

M62362P/FP

1280 RESOLUTION 3CH MULTIPLYING D-A CONVERTER

DESCRIPTION

The M62362P is an integrated circuit semiconductor of CMOS structure with 3 channels of built-in 1280 step resolution (equivalent 10.3-bit) multiplication type D-A converters.

is able to cascading serial use with Do terminal.
The device is suited for use in high accuracy automatic adjustment combination with microcomputer.

FEATURES

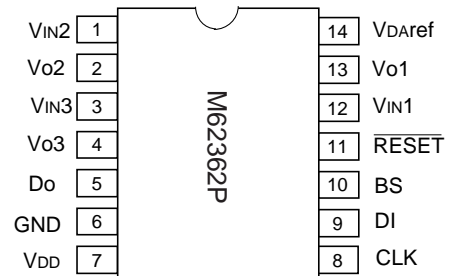
- Digital data transfer method
- 3-wire serial data transfer method
- High resolution
Resolution is more over 10-bit and error is less than ± 1 LSB
- Capable of 4 quadrant multiplication
- Short setting time
- With reset terminal

$$DD=5V\pm 10\%$$

APPLICATION

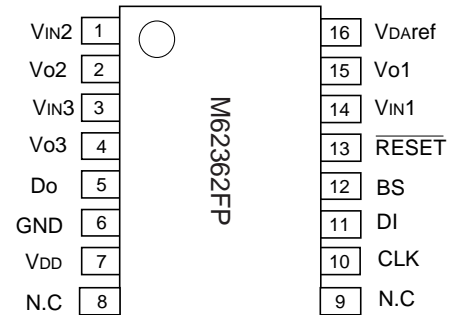
Signal gain control of DISPLAY-MONITOR or CTV.
Conversion from digital control data to analog control data for home-use and industrial equipment.
Automatic adjustment by combination with EEPROM and microcomputer. (replacement of conventional half-fixed

PIN CONFIGURATION (TOP VIEW)



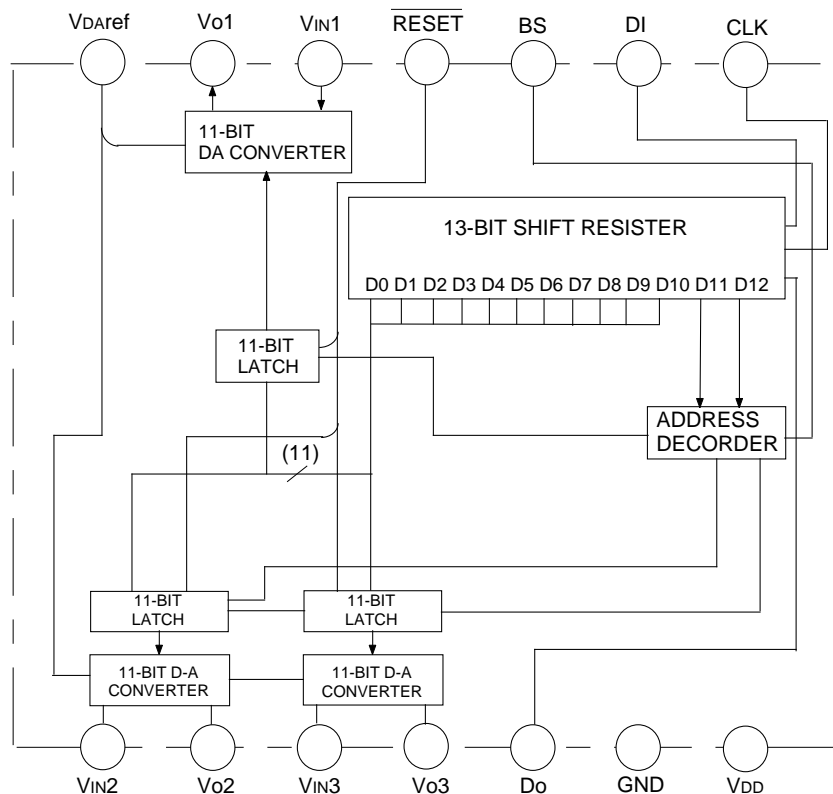
Outline 14P4

PIN CONFIGURATION (TOP VIEW)



Outline 16P2N

BLOCK DIAGRAM



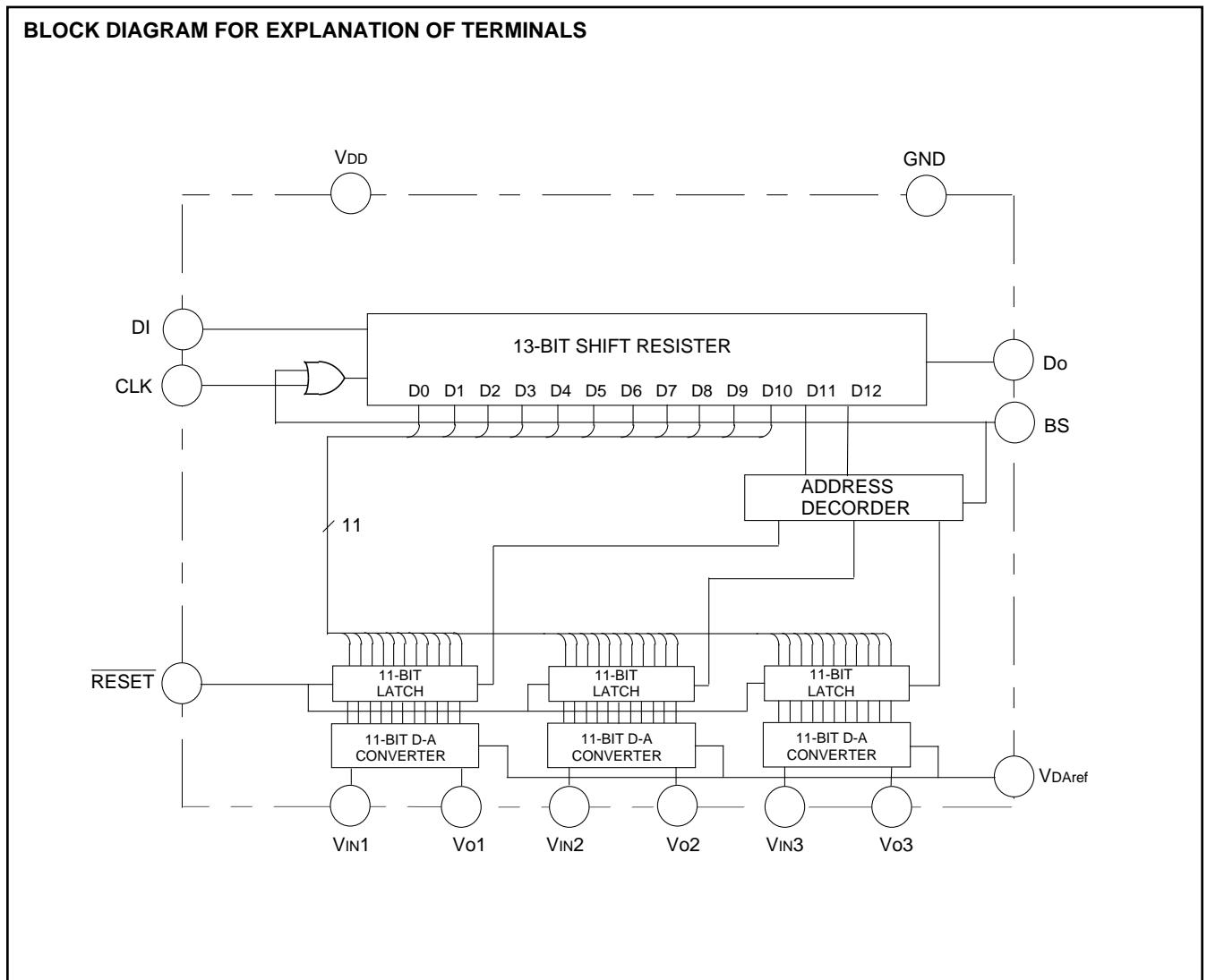
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EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
⑨ ⑪	DI	Serial data input terminal
⑤	Do	Serial data output terminal
⑧ ⑩	CLK	Serial clock input terminal
⑩ ⑫	BS	When BS terminal level is "H" latch circuit data is load
⑪ ⑬	RESET	When RESET terminal level is "L",all D-A output terminal became "L"
⑬ ⑮	Vo1	1280 resolution D-A output
②	Vo2	
④	Vo3	
⑦	V _{DD}	Power supply terminal
⑥	GND	GND terminal
①	V _{IN2}	D-A converter input terminal
③	V _{IN3}	
⑫ ⑭	V _{IN1}	
⑭ ⑯	V _{Dref}	D-A converter reference voltage input terminal

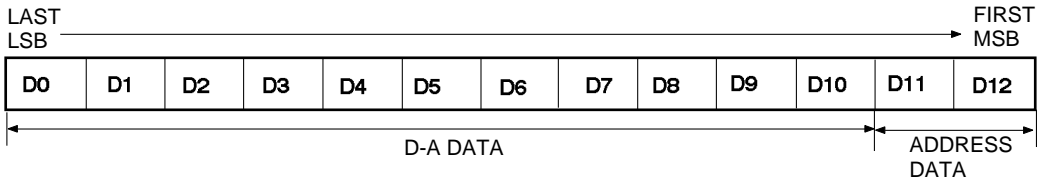
BLOCK DIAGRAM FOR EXPLANATION OF TERMINALS



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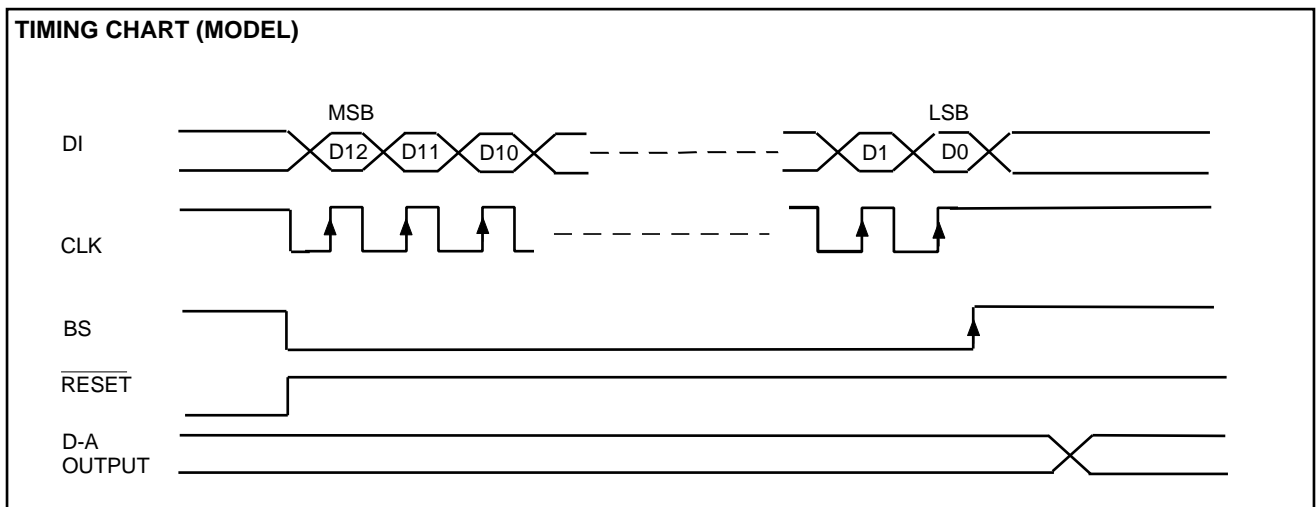
DIGITAL DATA FORMAT



D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D-A output
0	0	0	0	0	0	0	0	0	0	0	V_{Dref}
1	0	0	0	0	0	0	0	0	0	0	$(V_{IN}-V_{Dref}) / 1280 \times 1 + V_{Dref}$
0	1	0	0	0	0	0	0	0	0	0	$(V_{IN}-V_{Dref}) / 1280 \times 2 + V_{Dref}$
1	1	0	0	0	0	0	0	0	0	0	$(V_{IN}-V_{Dref}) / 1280 \times 3 + V_{Dref}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	1	0	0	1	$(V_{IN}-V_{Dref}) / 1280 \times 1279 + V_{Dref}$
0	0	0	0	0	0	0	0	1	0	1	V_{IN}
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	1	1	1	1	V_{IN}

D11	D12	DAC SELECTION
0	0	Don't care
0	1	ch1
1	0	ch2
1	1	ch3

TIMING CHART (MODEL)



*Input data is carried out BS signal "L" besides CLK signal positive edge.
CLK,BS,is keep generally "H" level.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{DD}	Supply voltage		-0.3~+7.0	V
V _{IND}	Digital input voltage(DI,CLK,BS)		-0.3~+7.0	V
V _{IN}	Input voltage		-0.3~V _{DD} +0.3	V
V _O	Output voltage		-0.3~V _{DD} +0.3	V
V _{DAREF}	D-A reference voltage		-0.3~V _{DD} +0.3	V
T _{opr}	Operating temperature		-20~+85	°C
T _{stg}	Storage temperature		-40~+125	°C

ELECTRICAL CHARACTERISTICS

Digital part(V_{DD},V_{IN}=+5V±10%, V_{DD} V_{IN},GND=V_{DAREF}=0V,Ta=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{DD}	Supply voltage		4.5	5.0	5.5	V
I _{ILK}	Input leak current	V _{IN} =0~V _{DD}	-10		10	μA
I _{IL}	Input low voltage				0.2V _{DD}	V
I _{IH}	Input high voltage		0.8V _{DD}			V
V _{OL}	Output low voltage	I _{OL} =2.5mA			0.4	V
V _{OH}	Output high voltage	I _{OH} =-400μA	V _{DD} -0.4			V

Analog part(V_{DD},V_{IN}=+5V±10%, V_{DD} V_{IN},GND=V_{DAREF}=0V,Ta=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{IN}	Input voltage		0		V _{DD}	V
V _O	Output voltage	V _{IN} =0~V _{DD}	0		V _{DD}	V
I _{IN}	Input current	V _{IN} =5V,V _{DAREF} =0V, Proportional to (V _{IN} -V _{DAREF})		0.75	1.5	mA
I _{DAREF}	D-A reference source current	V _{IN1} =V _{IN2} =V _{IN3} =5V, V _{DAREF} =0V, Proportional to (V _{IN} -V _{DAREF})	-4.5	-2.25		mA
I _O	D-A output sink or source current		-1.0		1.0	μA/LSB
R _O	Output impedance	Constant for all D-A output mode		1.8	3.6	k
RES	Resolution			1280		STEP
DNL	ACCURACY Differential nonlinearity		-1		1	LSB
NL		Nonlinearity	-0.6		0.6	%FS
NL		Nonlinearity for channels	-0.4		0.4	%FS

*Polarity of current, (+) is sink into IC and (-) is source from IC.

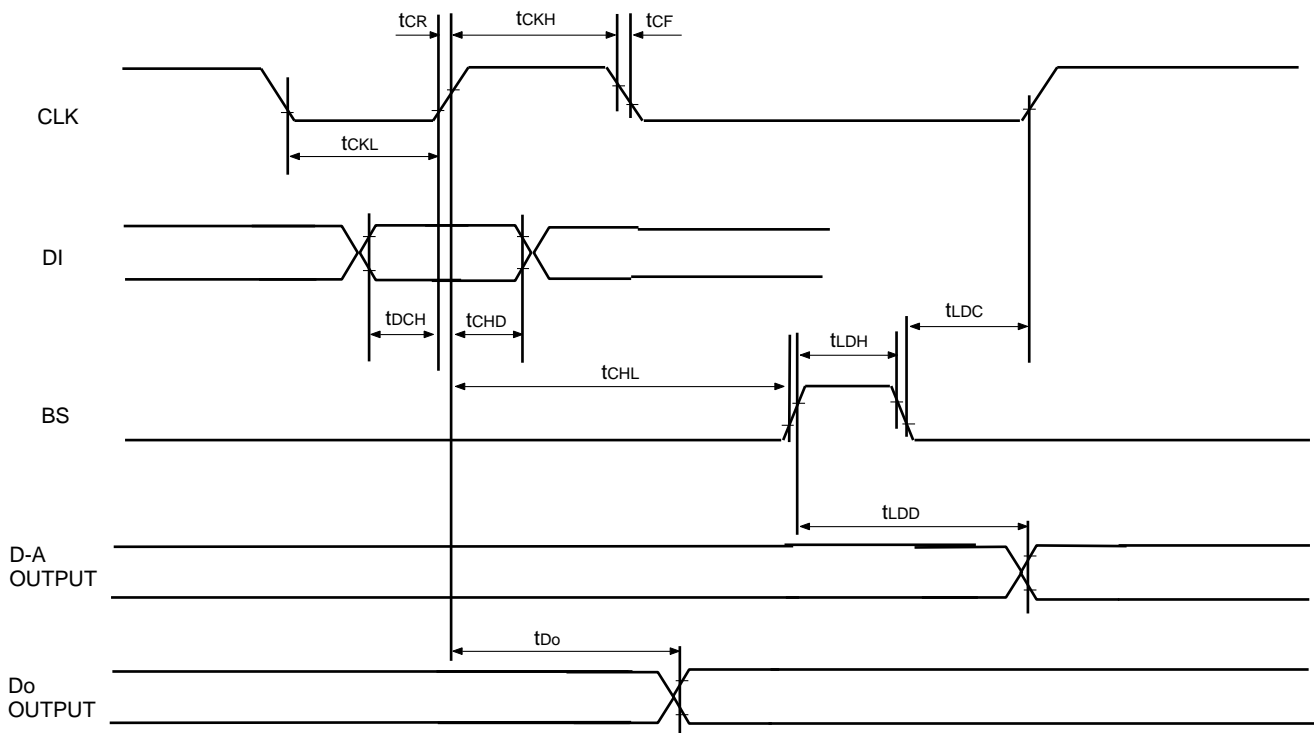
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AC CHARACTERISTICS ($V_{DD}, V_{IN} = +5V \pm 10\%$, $V_{DD}, V_{IN}, GND = V_{DAREF} = 0V$, $T_a = -20 \sim +85^\circ C$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
tCKL	Clock "L" pulse width		200			ns
tCKH	Clock "H" pulse width		200			ns
tCR	Clock rise time				200	ns
tCF	Clock fall time				200	ns
tDCH	Data set up time		60			ns
tCHD	Data hold time		100			ns
tCHL	LD set up time		200			ns
tLDC	LD hold time		100			ns
tLDH	LD "H" pulse width		100			ns
tDo	Data output delay time	CL 100pF	70		350	ns
tLDD	Data output setting time	No Load			20	μs
	Input-Output response time	f=10kHz			5	

TIMING CHART

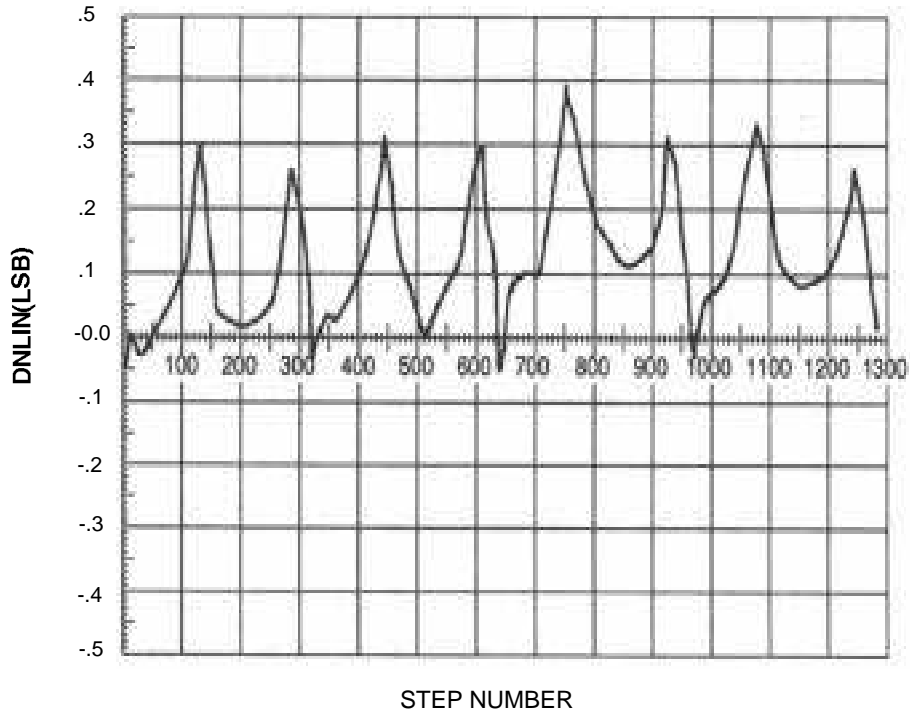


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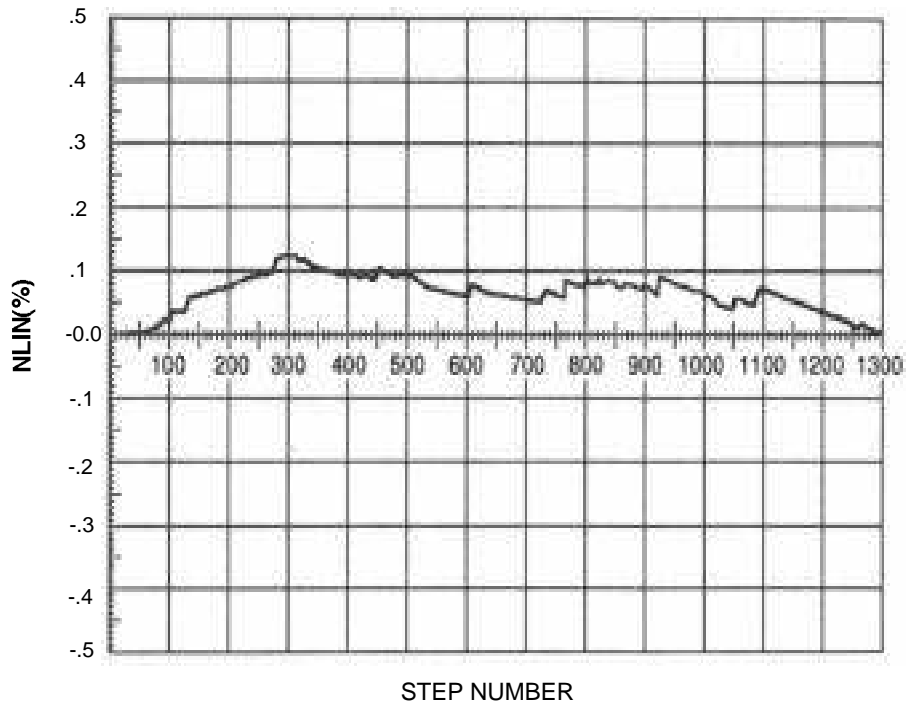
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TYPICAL CHARACTERISTICS

M62362P DIFFERENTIAL NONLINEARITY



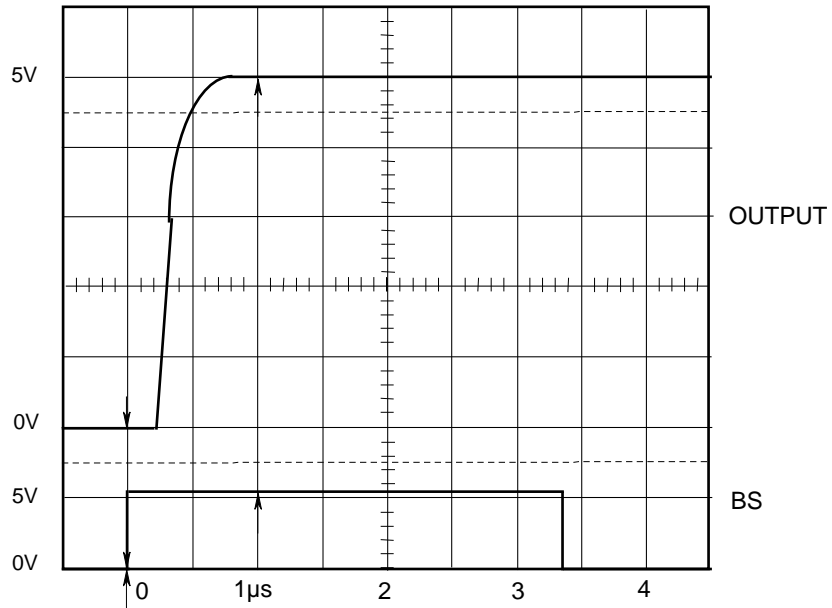
M62362P NONLINEARITY



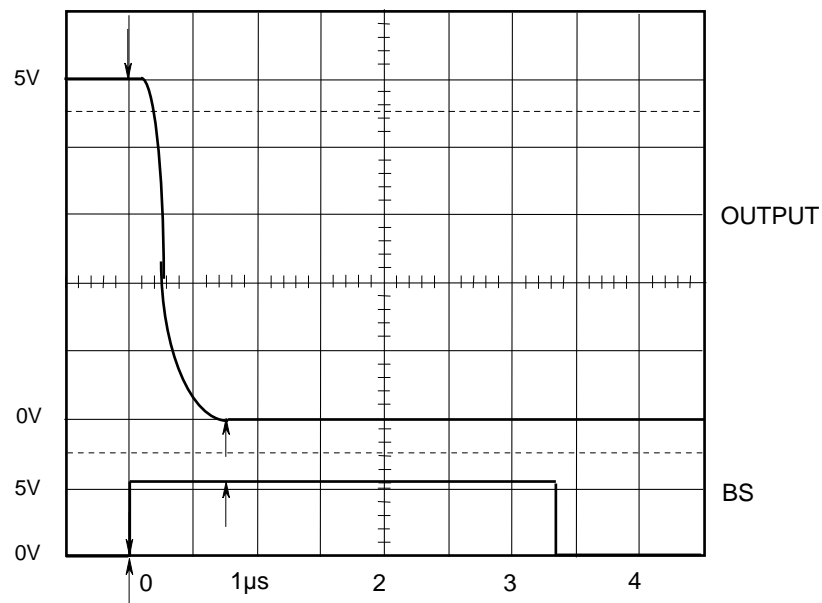
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1280 RESOLUTION 3CH MULTIPLYING D-A CONVERTER

M62362P OUTPUT RISE CHARACTERISTICS(SETTING TIME)



M62362P OUTPUT FALL CHARACTERISTICS(SETTING TIME)



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NOTICE

M62362 have 5 terminals these are input free voltage at use.(VDD, VIN1,VIN2,VIN3,VDaref)If Ripple and Spike is input to these terminals,accuracy of conversion is down .So,When use this device, please connect capacitor among to each terminals and GND for stable operation.

APPLICATION EXAMPLE

