

# M62381FP

## 8-BIT 8CH MULTIPLYING D-A CONVERTER WITH BUFFER AMPLIFIERS

### DESCRIPTION

The M62381FP is an integrated circuit semiconductor of CMOS structure with 8 channels of built-in 8-bit resolution multiplication type D-A converters.

The input data is a easy-to-use 3-wire serial transfer method and it is able to cascading serial use with Do terminal.

This device is capable of 4 quadrant multiplication because of built-in inverting type amplifier.

### FEATURES

- Digital data transfer method  
3-wire 12-bit serial data transfer method(DI,CLK,LD)
- High pressure proof( $V_{DD} \pm 5V$ )
- Short setting time
- Built-in reset terminal,all the buffer amplifier outputs forces zero volts.

### APPLICATION

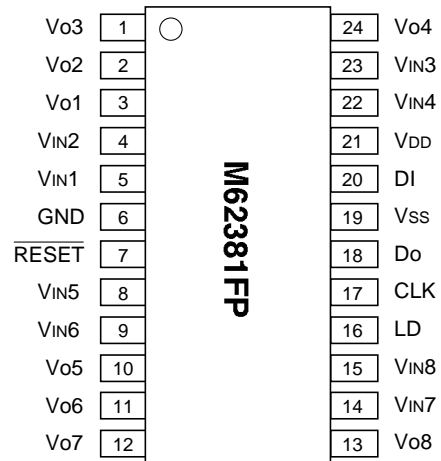
Signal gain control of DISPLAY-MONITOR or CTV.

Conversion from digital control data analog control data for form-use and industrial equipment.

Automatic adjustment by combination with EEPROM and micro-computer.

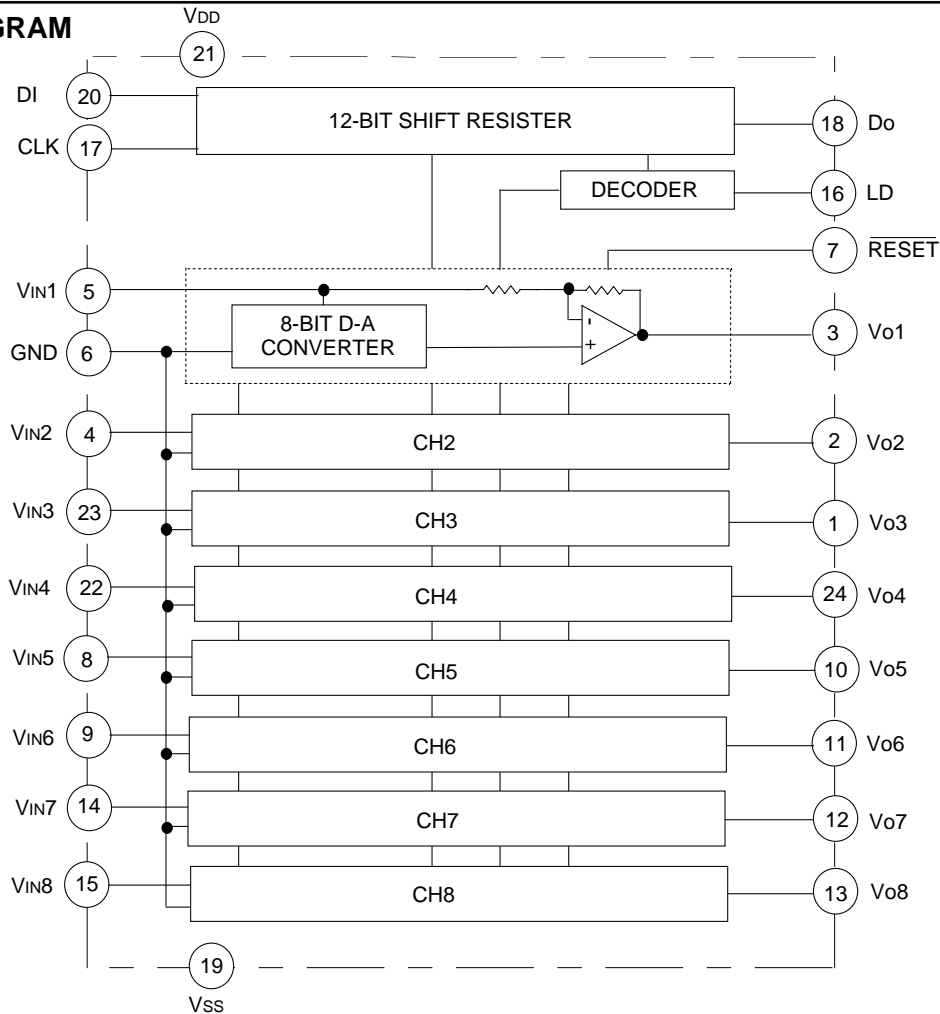
(replacement of conventional half-fixed resistor.)

### PIN CONFIGURATION (TOP VIEW)



Outline 24P2V-A

### BLOCK DIAGRAM



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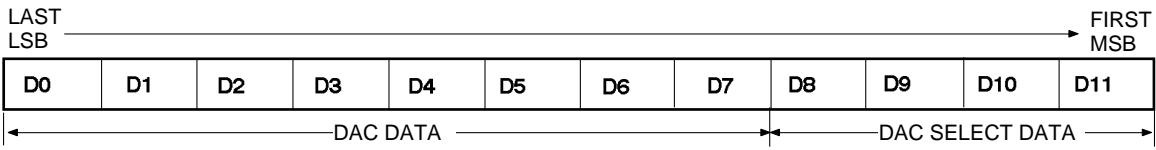
### EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
⑳	DI	Serial data input terminal
⑱	Do	Serial data output terminal
⑰	CLK	Serial clock input terminal
⑰	LD	When LD terminal level is "H",latch circuit data is load
③	Vo1	8-bit resolution D-A converter output terminal
②	Vo2	
①	Vo3	
㉔	Vo4	
⑩	Vo5	
⑪	Vo6	
⑫	Vo7	
⑬	Vo8	
㉑	V <sub>DD</sub>	Analog and digital common power supply terminal
⑲	V <sub>SS</sub>	Analog negative power supply terminal
⑥	GND	GND terminal
⑤	V <sub>IN1</sub>	D-A converter reference input terminal
④	V <sub>IN2</sub>	
㉓	V <sub>IN3</sub>	
㉒	V <sub>IN4</sub>	
⑧	V <sub>IN5</sub>	
⑨	V <sub>IN6</sub>	
⑭	V <sub>IN7</sub>	
⑮	V <sub>IN8</sub>	
⑦	RESET	When RESET terminal level is "H",all D-A output terminal became "0V"

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### DIGITAL DATA FORMAT



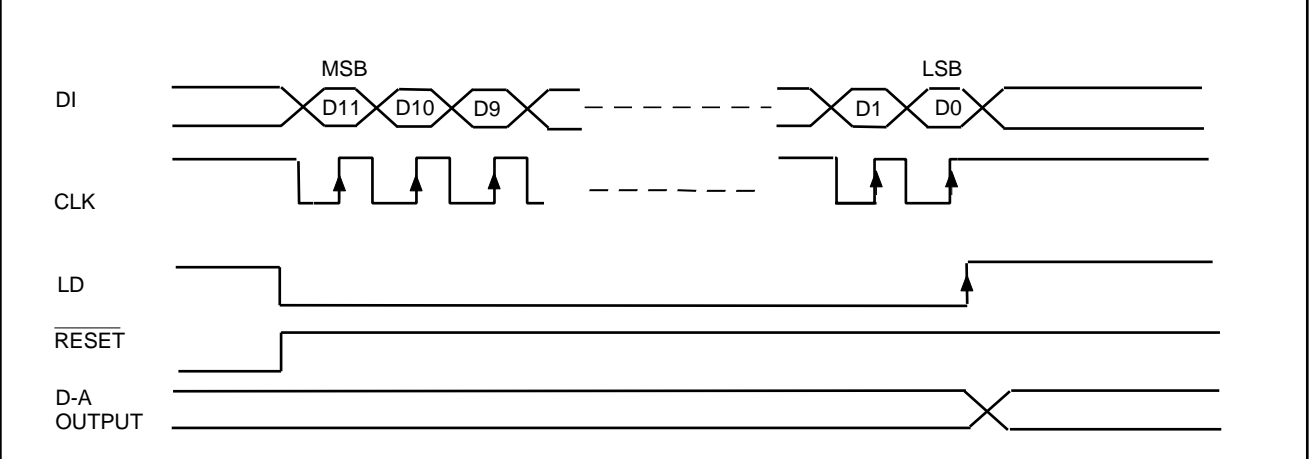
(1)DAC set up data

MSB							LSB	D-A output
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	-V <sub>IN</sub>
0	0	0	0	0	0	0	1	(1/128-1) X V <sub>IN</sub>
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	(127/128-1) X V <sub>IN</sub>
1	0	0	0	0	0	0	0	(128/128-1) X V <sub>IN</sub>
1	0	0	0	0	0	0	1	(129/128-1) X V <sub>IN</sub>
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	(254/128-1) X V <sub>IN</sub>
1	1	1	1	1	1	1	1	(255/128-1) X V <sub>IN</sub>

(2)DAC select data

MSB				LSB	DAC selection
D11	D10	D9	D8		
0	0	0	0	Don't care	
0	0	0	1	ch1 selection	
0	0	1	0	ch2 selection	
⋮	⋮	⋮	⋮	⋮	
0	1	1	1	ch7 selection	
1	0	0	0	ch8 selection	
1	0	0	1	Don't care	
⋮	⋮	⋮	⋮	⋮	
1	1	1	1	Don't care	

### TIMING CHART (MODEL)



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### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>DD</sub>	Supply voltage		-0.3 to +6.0	V
V <sub>IN</sub>	Digital input voltage		-0.3 to +6.0	V
V <sub>SS</sub>	Analog negative supply voltage		-6.0 to +3.0	V
V <sub>IN</sub>	Input voltage		V <sub>SS</sub> +0.3 to V <sub>DD</sub> -0.3	V
V <sub>o</sub>	Output voltage		V <sub>SS</sub> +0.3 to V <sub>DD</sub> -0.3	V
T <sub>opr</sub>	Operating temperature		-20 to +85	°C
T <sub>stg</sub>	Storage temperature		-40 to +125	°C

### ELECTRICAL CHARACTERISTICS

**Digital part**(V<sub>DD</sub>=+5V, V<sub>SS</sub>=-5V, V<sub>DD</sub> V<sub>IN</sub> V<sub>SS</sub>, GND=0V, T<sub>a</sub>=-20 to +85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V <sub>DD</sub>	Supply voltage		4.5	5.0	5.5	V
I <sub>ILK</sub>	Input leak current	V <sub>IN</sub> =0 to V <sub>CC</sub>	-10		10	μA
V <sub>IL</sub>	Input low voltage				0.2V <sub>DD</sub>	V
V <sub>IH</sub>	Input high voltage		0.8V <sub>DD</sub>			V
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> =2.5mA			0.4	V
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> =-400μA	V <sub>DD</sub> -0.4			V

**Analog part**(V<sub>DD</sub>=+5V, V<sub>SS</sub>=-5V, V<sub>DD</sub> V<sub>IN</sub> V<sub>SS</sub>, GND=0V, T<sub>a</sub>=-20 to +85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I <sub>IN</sub>	D-A converter reference input current			0.2	0.4	mA
V <sub>AO</sub>	Buffer amplifier output voltage range	I <sub>AO</sub> =±500μA I <sub>AO</sub> =±1mA	V <sub>AOZERO</sub> +0.15 V <sub>AOZERO</sub> +0.3		V <sub>AOFULL</sub> -0.15 V <sub>AOFULL</sub> -0.3	V
I <sub>AO</sub>	Buffer amplifier output current range	V <sub>AO</sub> =V <sub>AOZERO</sub> +0.3 to V <sub>AOFULL</sub> -0.3	-1.0		1.0	mA
RES	Resolution		8			bit
DNL	Differential nonlinearity		-1.0		1.0	LSB
NL	Nonlinearity	V <sub>DD</sub> -0.5 V <sub>IN</sub> V <sub>SS</sub> +0.5	-1.5		1.5	LSB
EG	Gain error		-3		3	%FS

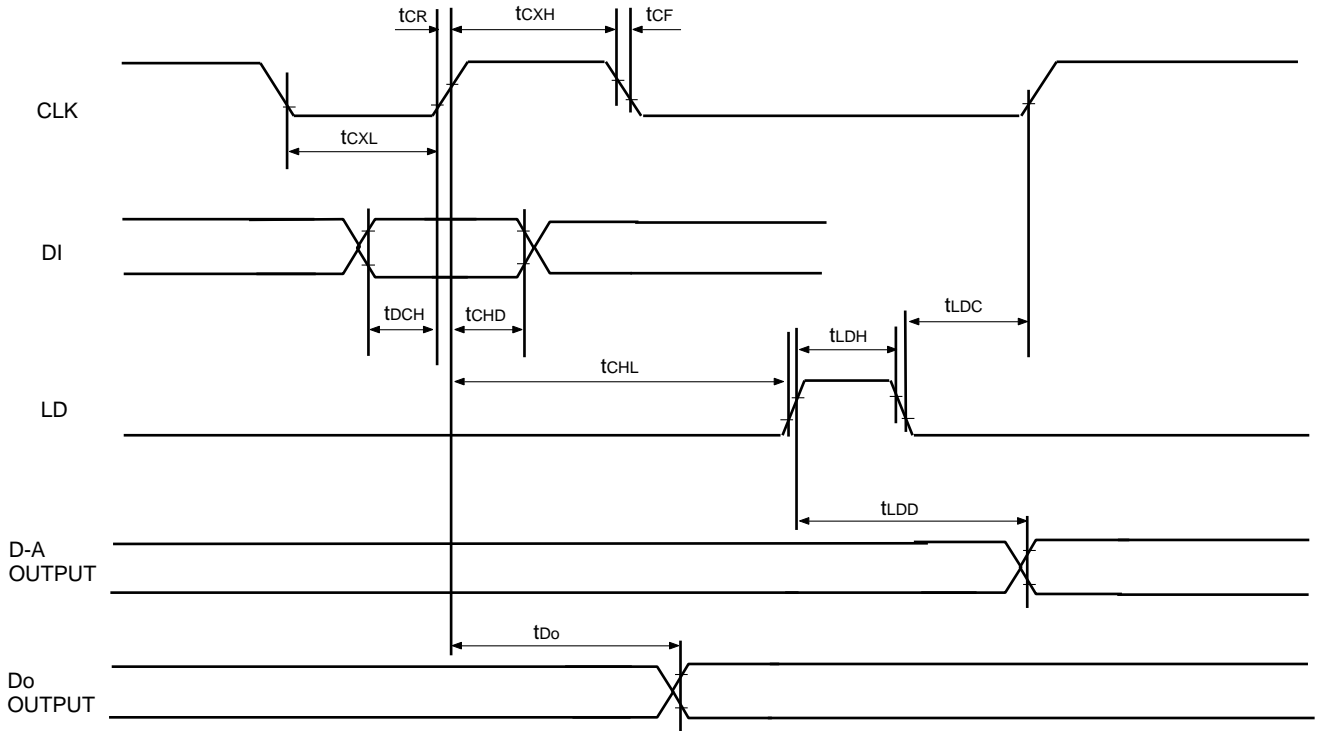
### AC CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t <sub>CXL</sub>	Clock "L" pulse width		200			ns
t <sub>CXH</sub>	Clock "H" pulse width		200			ns
t <sub>CR</sub>	Clock rise time				200	ns
t <sub>CF</sub>	Clock fall time				200	ns
t <sub>DCH</sub>	Data set up time		30			ns
t <sub>CHD</sub>	Data hold time		60			ns
t <sub>CHL</sub>	LD set up time		200			ns
t <sub>LDH</sub>	LD hold time		100			ns
t <sub>LDC</sub>	LD "H" pulse width		100			ns
t <sub>do</sub>	Data output delay time	C <sub>L</sub> =100pF	70		350	ns
t <sub>LDD</sub>	D-A output setting time	Without load				ns

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### TIMING CHART



### APPLICATION EXAMPLE

