

96-Bit AC-PDP DRIVER

The μ PD16335 is a high-voltage CMOS driver designed for flat display panels such as PDPs, VFDs and ELs. It consists of a 96-bit bi-directional shift register, 96-bit latch and high-voltage CMOS driver. The logic block is designed to operate using a 5-V power supply enabling direct connection to a gate array or a microcontroller. In addition, the μ PD16335 achieves low power dissipation by employing CMOS structure while having a high withstand voltage output (80 V, +50/-75 mA).

FEATURES

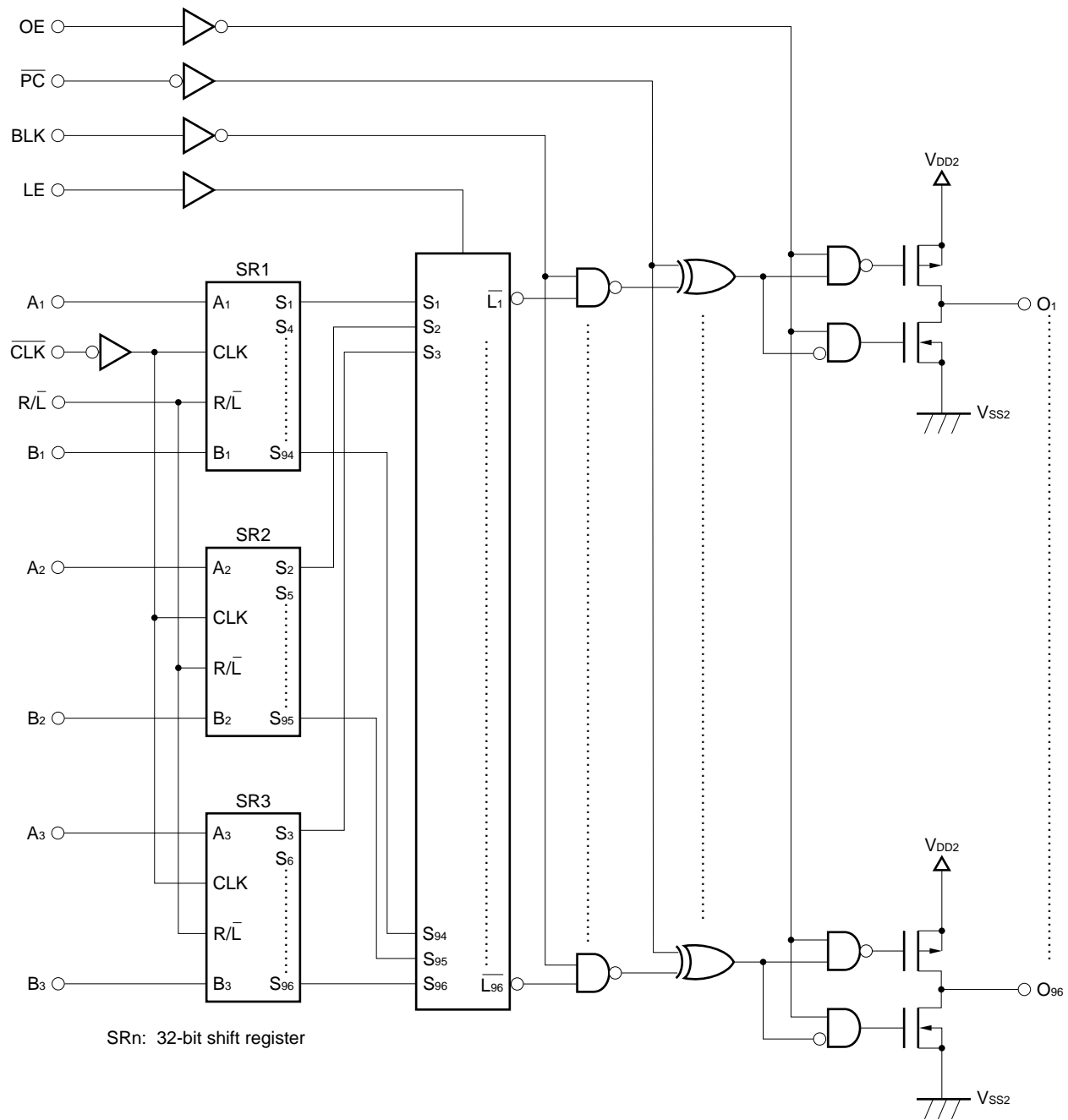
- Selectable by IBS pin; three 32-bit bi-directional shift register circuits configuration or six 16-bit bi-directional shift register circuits configuration
- Data control with transfer clock (external) and latch
- High-speed data transfer ($f_{\max.} = 25$ MHz min. at data fetch)
($f_{\max.} = 16$ MHz min. at cascade connection)
- High withstand output voltage (80 V, +50/-75 mA_{MAX.})
- 5 V CMOS input interface
- High withstand voltage CMOS structure
- Capable of reversing all driver outputs by \overline{PC} pin

ORDERING INFORMATION

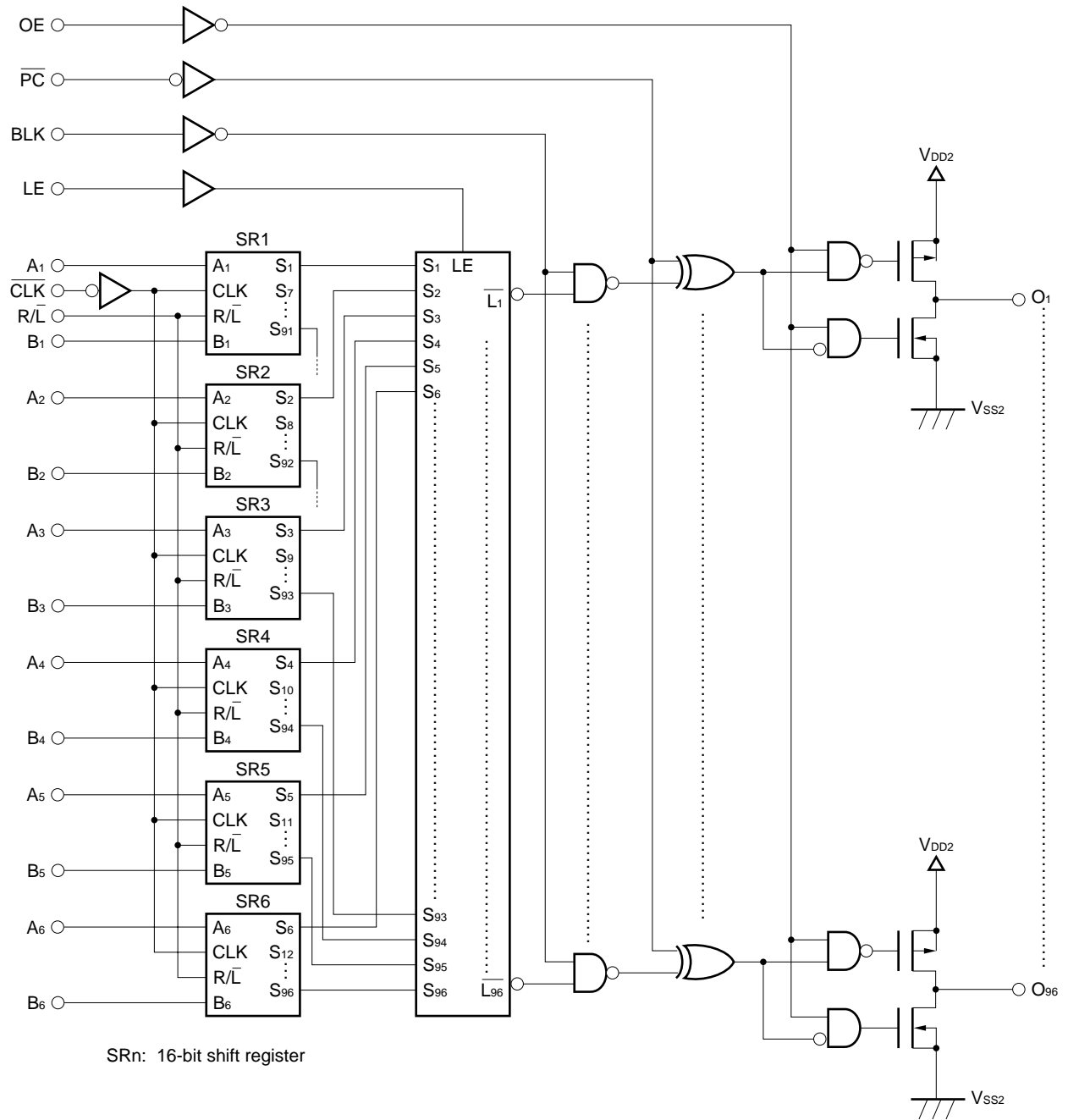
| Part Number | Package |
|---------------|---------------------|
| μ PD16335 | COB ^{Note} |

Note Please consult with an NEC sales representative about COB.

BLOCK DIAGRAM (IBS = H, 3-BIT INPUT, 32-BIT LENGTH SHIFT REGISTER)



BLOCK DIAGRAM (IBS = L, 6-BIT INPUT, 16-BIT LENGTH SHIFT REGISTER)



PIN DESCRIPTION

| Symbol | Pin Name | Description |
|--------------------------------------|---|---|
| \overline{PC} | Polarity change input | $\overline{PC} = L$: All driver output invert |
| BLK | Blank input | BLK = H: All output = H or L |
| LE | Latch enable input | Data latch by rising edge of this signal. |
| OE | Output enable | Make output high impedance by input H |
| A ₁ to A _{3 (6)} | RIGHT data input/output ^{Note} | When $R/\overline{L} = H$ (values in parentheses are for 6-bit input) A ₁ to A _{3 (6)} : Input B ₁ to B _{3 (6)} : Output |
| B ₁ to B _{3 (6)} | LEFT data input/output ^{Note} | When $R/\overline{L} = L$ (values in parentheses are for 6-bit input) A ₁ to A _{3 (6)} : Output B ₁ to B _{3 (6)} : Input |
| \overline{CLK} | Clock input | Shift executed on fall |
| R/\overline{L} | Shift control input | Right shift mode when $R/L = H$ SR ₁ : A ₁ → S ₁ ... S ₉₄ → B ₁ (Same direction for SR ₂ to SR ₆) Left shift mode when $R/L = L$ SR ₁ : B ₁ → S ₉₄ ... S ₁ → A ₁ (Same direction for SR ₂ to SR ₆) |
| IBS | Input mode switch | H: 32-bit length shift register, 3-bit input L: 16-bit length shift register, 6-bit input |
| O ₁ to O ₉₆ | High withstand voltage output | 80 V, +50/-75 mA _{MAX.} |
| V _{DD1} | Power supply for logic block | 5 V ±10% |
| V _{DD2} | Power supply for driver block | 10 to 70 V |
| V _{SS1} | Logic GND | Connect to system GND |
| V _{SS2} | Driver GND | Connect to system GND |

Note When input mode is 3-bit, set unused input and output pins “L” level.

TRUTH TABLE 1 (Shift Register Block)

| Input | | Output | | Shift Register |
|------------------|------------------|--------------------------|--------------------------|-----------------------|
| R/\overline{L} | \overline{CLK} | A | B | |
| H | ↓ | Input | Output ^{Note 1} | Right shift execution |
| H | H or L | | Output | Hold |
| L | ↓ | Output ^{Note 2} | Input | Left shift execution |
| L | H or L | Output | | Hold |

Notes 1. The data of S₉₁ to S₉₃ (S₈₅ to S₉₀) shifts to S₉₄ to S₉₆ (S₉₁ to S₉₆) and is output from B₁ to B₃ (B₁ to B₆) at the falling edge of the clock, respectively. (Values in parentheses are for 6-bit input)

2. The data of S₄ to S₆ (S₇ to S₁₂) shifts to S₁ to S₃ (S₁ to S₆) and is output from A₁ to A₃ (A₁ to A₆) at the falling edge of the clock, respectively (Values in parentheses are for 6-bit input)

TRUTH TABLE 2 (Latch Block)

| LE | Output State of Latch Block (\overline{L}_n) |
|--------|--|
| ↑ | Latch S _n data |
| H or L | Hold latch data |

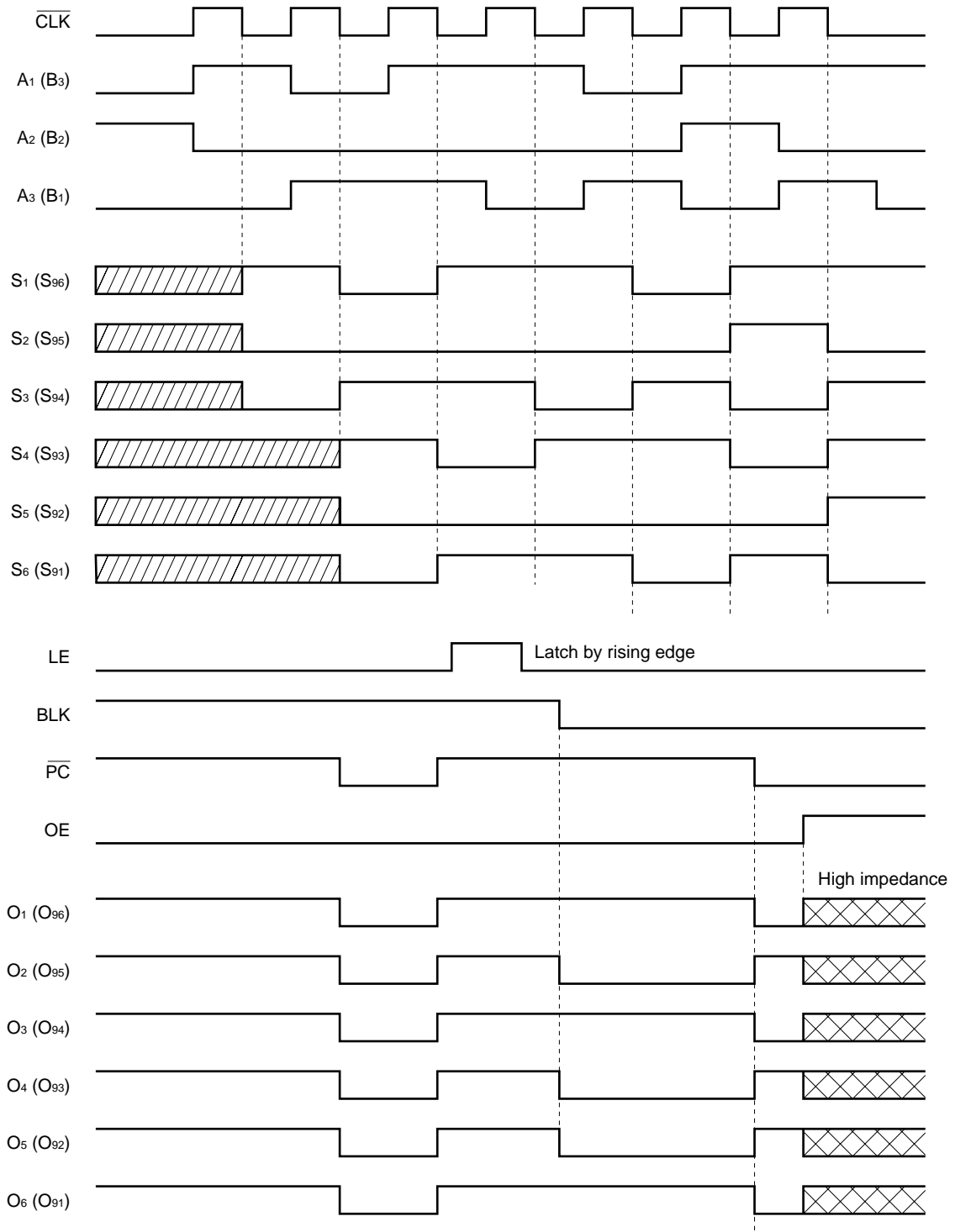
TRUTH TABLE 3 (Driver Block)

| \overline{L}_n | BLK | \overline{PC} | OE | Output State of Driver Block |
|------------------|-----|-----------------|----|--|
| X | H | H | L | H (All driver outputs: H) |
| X | H | L | L | L (All driver outputs: L) |
| X | L | H | L | Output latch data (\overline{L}_n) |
| X | L | L | L | Output inverted latch data ($\overline{\overline{L}_n}$) |
| X | X | X | H | Set output impedance high |

X: H or L, H: High level, L: Low level

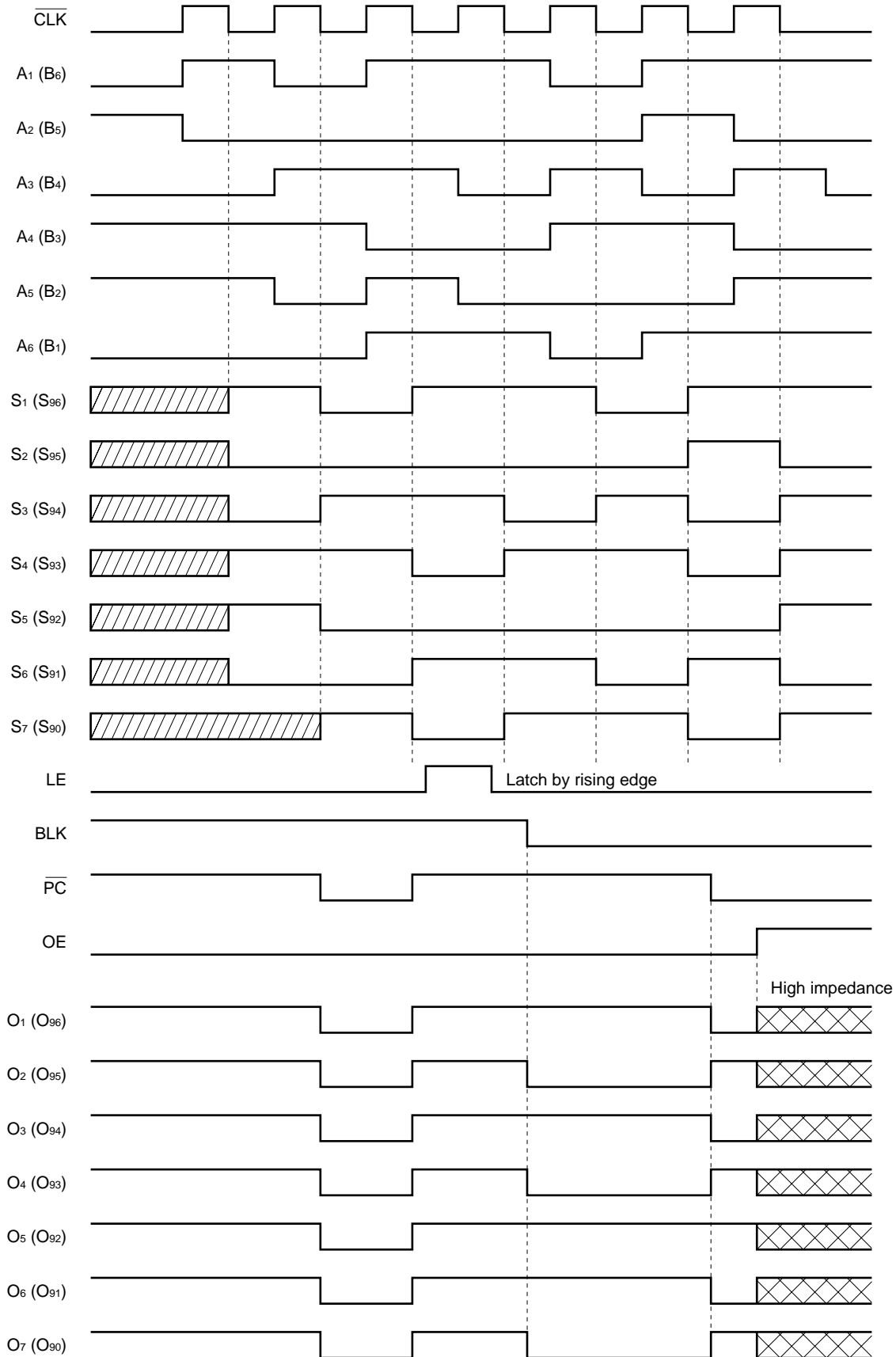
TIMING CHART (WHEN IBS = "H": 3-BIT INPUT, RIGHT SHIFT)

Values in parentheses in the following chart are when R/L = L.



TIMING CHART (WHEN IBS = "L": 6-BIT INPUT, RIGHT SHIFT)

Values in parentheses in the following chart are when $R/\bar{L} = L$.



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

| Parameter | Symbol | Ratings | Unit |
|-----------------------------|-------------------|-------------------------------|------|
| Logic Block Supply Voltage | V _{DD1} | -0.5 to +7.0 | V |
| Driver Block Supply Voltage | V _{DD2} | -0.5 to +80 | V |
| Logic Block Input Voltage | V _I | -0.5 to V _{DD1} +0.5 | V |
| Driver Block Output Current | I _{O2} | +50/-75 | mA |
| Junction Temperature | T _J | ±125 | °C |
| Storage Temperature | T _{stg.} | -65 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to +85°C, V_{SS1} = V_{SS2} = 0 V)

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit |
|-----------------------------|------------------|----------------------|------|----------------------|------|
| Logic Block Supply Voltage | V _{DD1} | 4.5 | 5.0 | 5.5 | V |
| Driver Block Supply Voltage | V _{DD2} | 10 | | 70 | V |
| High-Level Input Voltage | V _{IH} | 0.7 V _{DD1} | | V _{DD1} | V |
| Low-Level Input Voltage | V _{IL} | 0 | | 0.2 V _{DD1} | V |
| Driver Output Current | I _{OH2} | | | -60 | mA |
| | I _{OL2} | | | +40 | mA |

Caution In order to prevent latch-up breakage, be sure to enter the power to V_{DD1}, logic signal and V_{DD2} in that order, and turn off the power in the reverse order, keep this order also during a transition period.

ELECTRICAL SPECIFICATIONS (T_A = 25°C, V_{DD1} = 5.0 V, V_{DD2} = 70 V, V_{SS1} = V_{SS2} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|----------------------------|-------------------|--|----------------------|------|----------------------|------|
| High-Level Output Voltage | V _{OH1} | Logic, I _{OH1} = -1.0 mA | 0.9 V _{DD1} | | V _{DD1} | V |
| Low-Level Output Voltage | V _{OL1} | Logic, I _{OL1} = 1.0 mA | 0 | | 0.1 V _{DD1} | V |
| High-Level Output Voltage | V _{OH21} | O ₁ to O ₉₆ , I _{OH2} = -1.3 mA | 69 | | | V |
| | V _{OH22} | O ₁ to O ₉₆ , I _{OH2} = -13 mA | 65 | | | V |
| Low-Level Output Voltage | V _{OL21} | O ₁ to O ₉₆ , I _{OL2} = 5 mA | | | 1.0 | V |
| | V _{OL22} | O ₁ to O ₉₆ , I _{OL2} = 40 mA | | | 10 | V |
| Input Leakage Current | I _{IL} | V _I = V _{DD1} or V _{SS1} | | | ±1.0 | μA |
| High-Level Input Voltage | V _{IH} | | 0.7 V _{DD1} | | | V |
| Low-Level Input Voltage | V _{IL} | | | | 0.2 V _{DD1} | V |
| Static Current Dissipation | I _{DD1} | Logic, T _A = -40 to +85° | | | 100 | μA |
| | I _{DD1} | Logic, T _A = 25°C | | | 10 | μA |
| | I _{DD2} | Driver, T _A = -40 to +85° | | | 1000 | μA |
| | I _{DD2} | Driver, T _A = 25°C | | | 100 | μA |

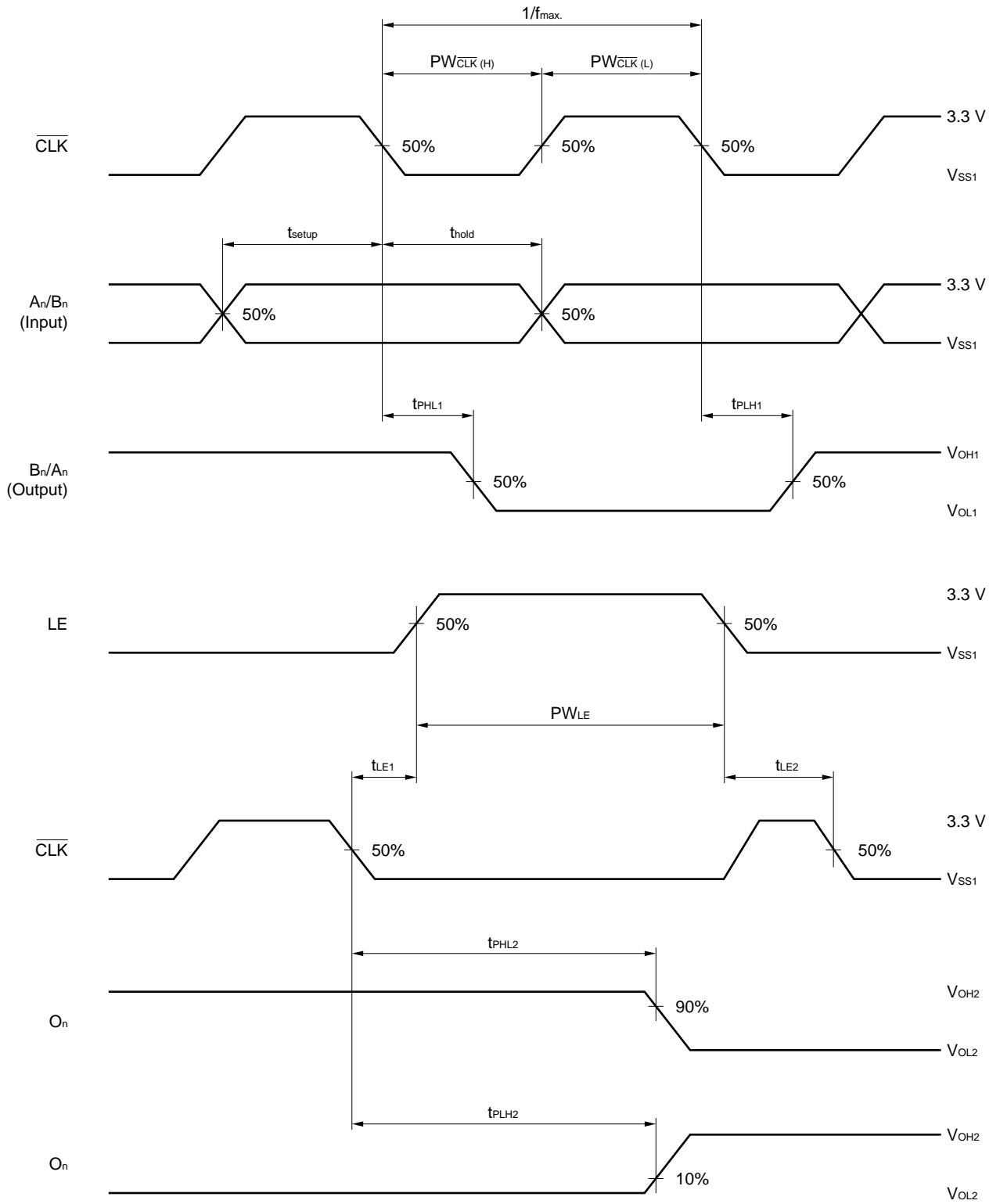
SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{DD1} = 5.0\text{ V}$, $V_{DD2} = 130\text{ V}$, $V_{SS1} = V_{SS2} = 0\text{ V}$, logic $C_L = 15\text{ pF}$, driver $C_L = 50\text{ pF}$, $t_r = t_f = 6.0\text{ ns}$)

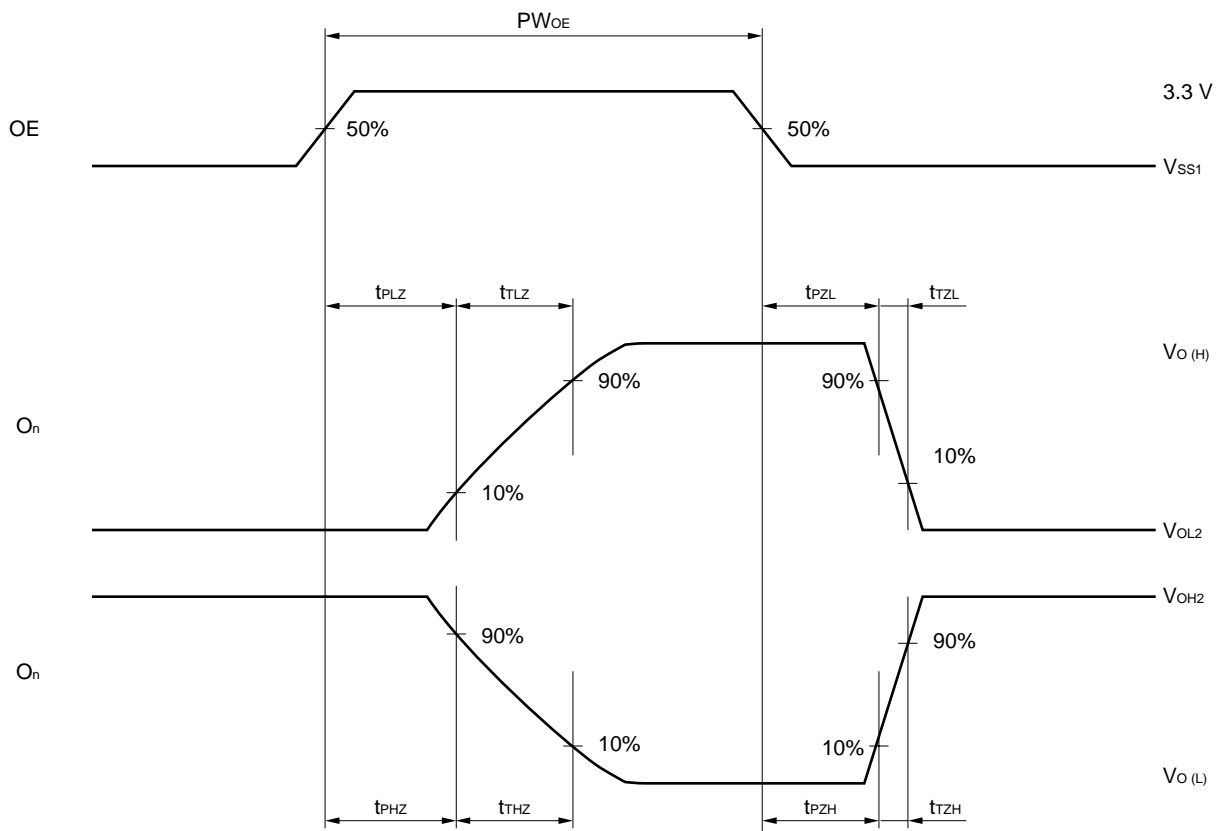
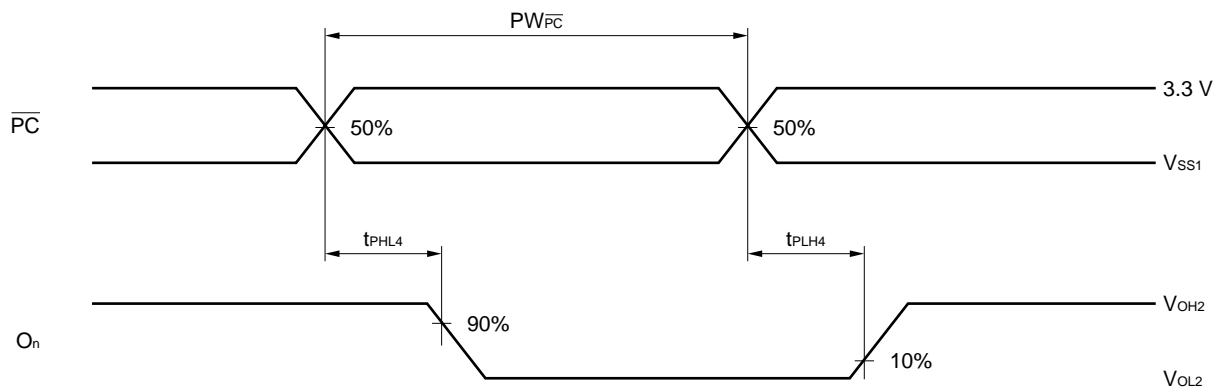
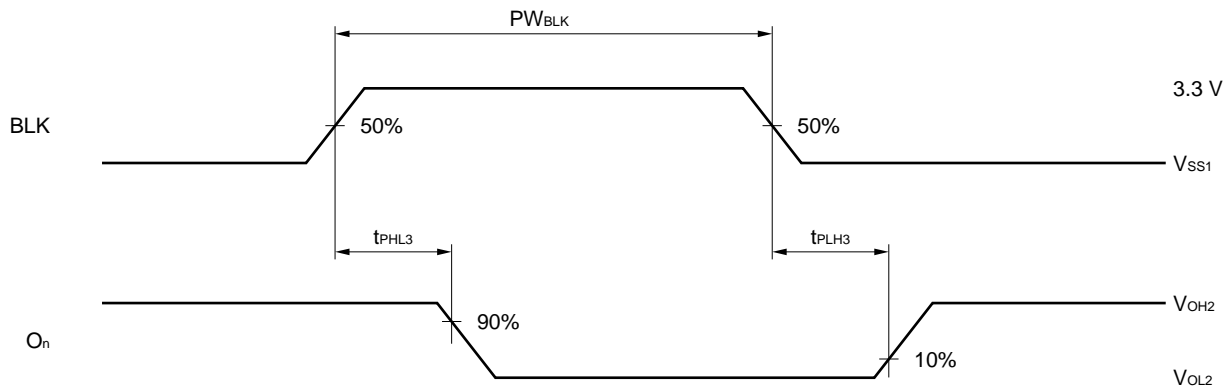
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------|------------------|--|------|------|------|---------------|
| Transmission Delay Time | t_{PHL1} | $\overline{\text{CLK}} \downarrow \rightarrow \text{A/B}$ | | | 55 | ns |
| | t_{PLH1} | | | | 55 | ns |
| | t_{PHL2} | $\overline{\text{CLK}} \uparrow (\text{LE} = \text{H}) \rightarrow \text{O}_1 \text{ to } \text{O}_{96}$ | | | 180 | ns |
| | t_{PLH2} | | | | 180 | ns |
| | t_{PHL3} | $\text{BLK} \rightarrow \text{O}_1 \text{ to } \text{O}_{96}$ | | | 165 | ns |
| | t_{PLH3} | | | | 165 | ns |
| | t_{PHL4} | $\overline{\text{PC}} \rightarrow \text{O}_1 \text{ to } \text{O}_{96}$ | | | 160 | ns |
| | t_{PLH4} | | | | 160 | ns |
| | t_{PHZ} | $\text{OE} \rightarrow \text{O}_1 \text{ to } \text{O}_{96}$ | | | 300 | ns |
| | t_{PZH} | $\text{RL} = 10\text{ k}\Omega$ | | | 180 | ns |
| | t_{PLZ} | | | | 300 | ns |
| | t_{PZL} | | | | 180 | ns |
| Rise Time | t_{TLH} | $\text{O}_1 \text{ to } \text{O}_{96}$ | | | 120 | ns |
| | t_{TLZ} | $\text{RL} = 10\text{ k}\Omega$ | | | 3 | μs |
| | t_{TZH} | $\text{O}_1 \text{ to } \text{O}_{96}$ | | | 120 | ns |
| Fall Time | t_{THL} | $\text{O}_1 \text{ to } \text{O}_{96}$ | | | 150 | ns |
| | t_{THZ} | $\text{RL} = 10\text{ k}\Omega$ | | | 3 | μs |
| | t_{TZL} | $\text{O}_1 \text{ to } \text{O}_{96}$ | | | 150 | ns |
| Maximum Clock Frequency | f_{max} | When data is read, duty 50% | 25 | | | MHz |
| | | cascade connection, Duty 50% | 16 | | | MHz |
| Input Capacitance | C_i | | | | 15 | pF |

TIMING REQUIREMENT ($T_A = -40 \text{ to } +85^\circ\text{C}$, $V_{DD1} = 4.5 \text{ to } 5.5\text{ V}$, $V_{SS1, 2} = 0\text{ V}$, $t_r = t_f = 6.0\text{ ns}$)

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|------------------------------------|------------------------------|---------------------------------|------|------|------|---------------|
| Clock Pulse Width | $PW_{\overline{\text{CLK}}}$ | | 20 | | | ns |
| Latch Enable Pulse Width | PW_{LE} | | 20 | | | ns |
| Blank Pulse Width | PW_{BLK} | | 200 | | | ns |
| $\overline{\text{PC}}$ Pulse Width | $PW_{\overline{\text{PC}}}$ | | 200 | | | ns |
| OE Pulse Width | PW_{OE} | $\text{RL} = 10\text{ k}\Omega$ | 3.3 | | | μs |
| Data Setup Time | t_{setup} | | 7 | | | ns |
| Data Hold Time | t_{hold} | | 10 | | | ns |
| Latch Enable Time 1 | t_{LE1} | | 20 | | | ns |
| Latch Enable Time 2 | t_{LE2} | | 20 | | | ns |

SWITCHING CHARACTERISTICS WAVEFORM





[MEMO]

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