NEC

MOS INTEGRATED CIRCUIT
μPD16340

96-BIT AC-PDP DRIVER

DESCRIPTION

The μPD16340 is a high withstand voltage CMOS driver designed for use with a flat display panel such as a PDP, VFD, or EL panel. It consists of a 96-bit bi-directional shift register, 96-bit latch and high withstand voltage CMOS driver. The logic block operates with a 5-V power supply interface (CMOS level input) so that it can be directly connected to a gate array and microcontroller. The driver block provides a high withstand voltage output: 80 V, +50/–75 mA MAX. The logic and driver blocks are made of CMOS circuits, consuming lower power.

FEATURES

- Circuit configuration switched by the IBS pin between three 32-bit bi-directional shift registers and six 16-bit bidirectional shift registers.
- Data control with transfer clock (external) and latch
- High-speed data transfer ($f_{MAX.}$ = 40 MHz MIN. at data latch)
  ($f_{MAX.}$ = 25 MHz MIN. at cascade connection)
- High withstand output voltage (80 V, +50/–75 mA MAX.)
- 5-V CMOS input interface
- High withstand voltage CMOS structure

★ ORDERING INFORMATION

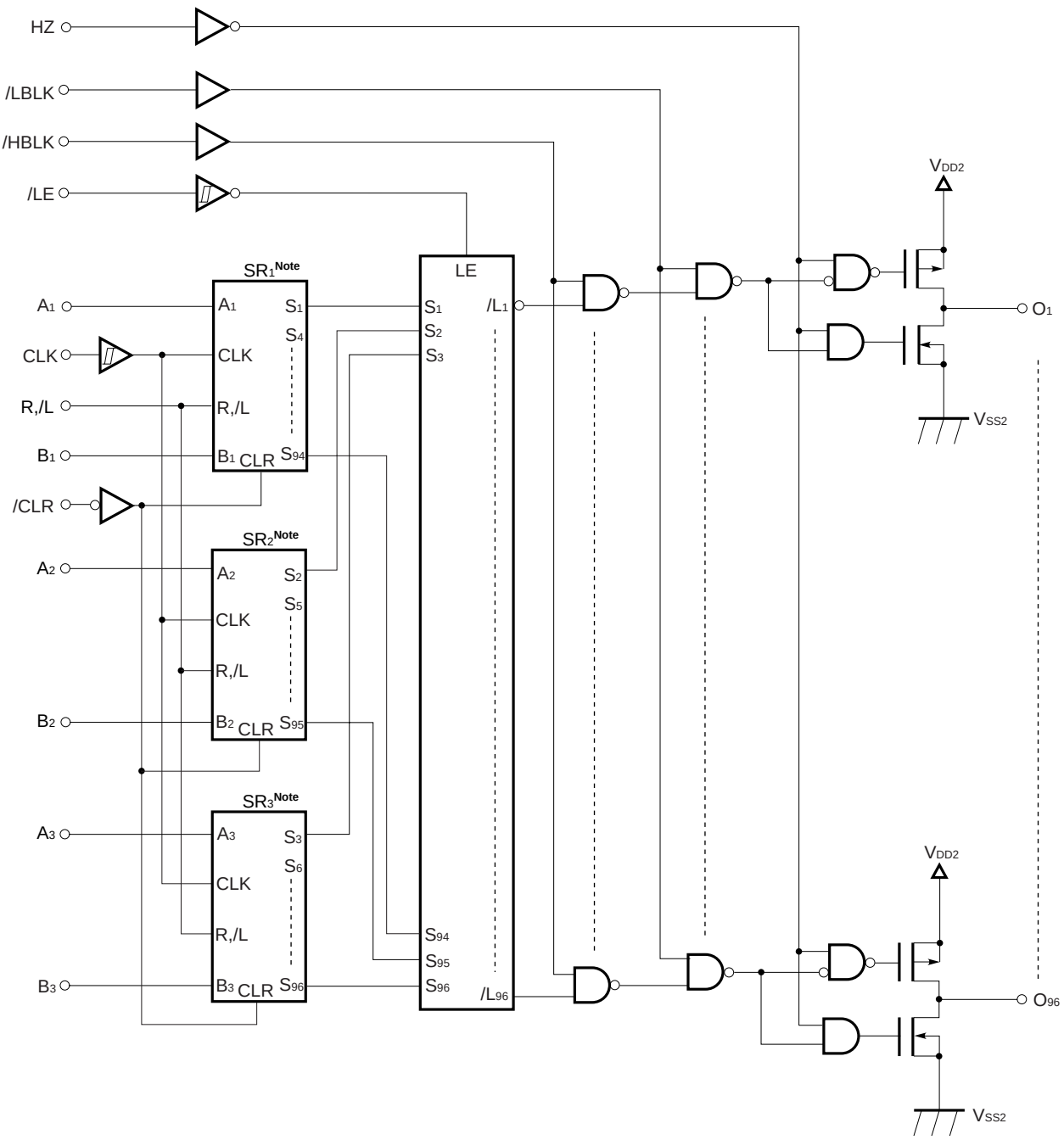
Part Number	Package
μPD16340	Module

Caution Consult an NEC sales representative regarding the module. Since the module characteristics is based on the module specifications, there may be differences between the contents written in this document and real characteristics.

Document No. S13685EJ1V0DS00 (1st edition)
Date Published December 1999 NS CP (K)
Printed in Japan

The mark ★ shows major revised points.

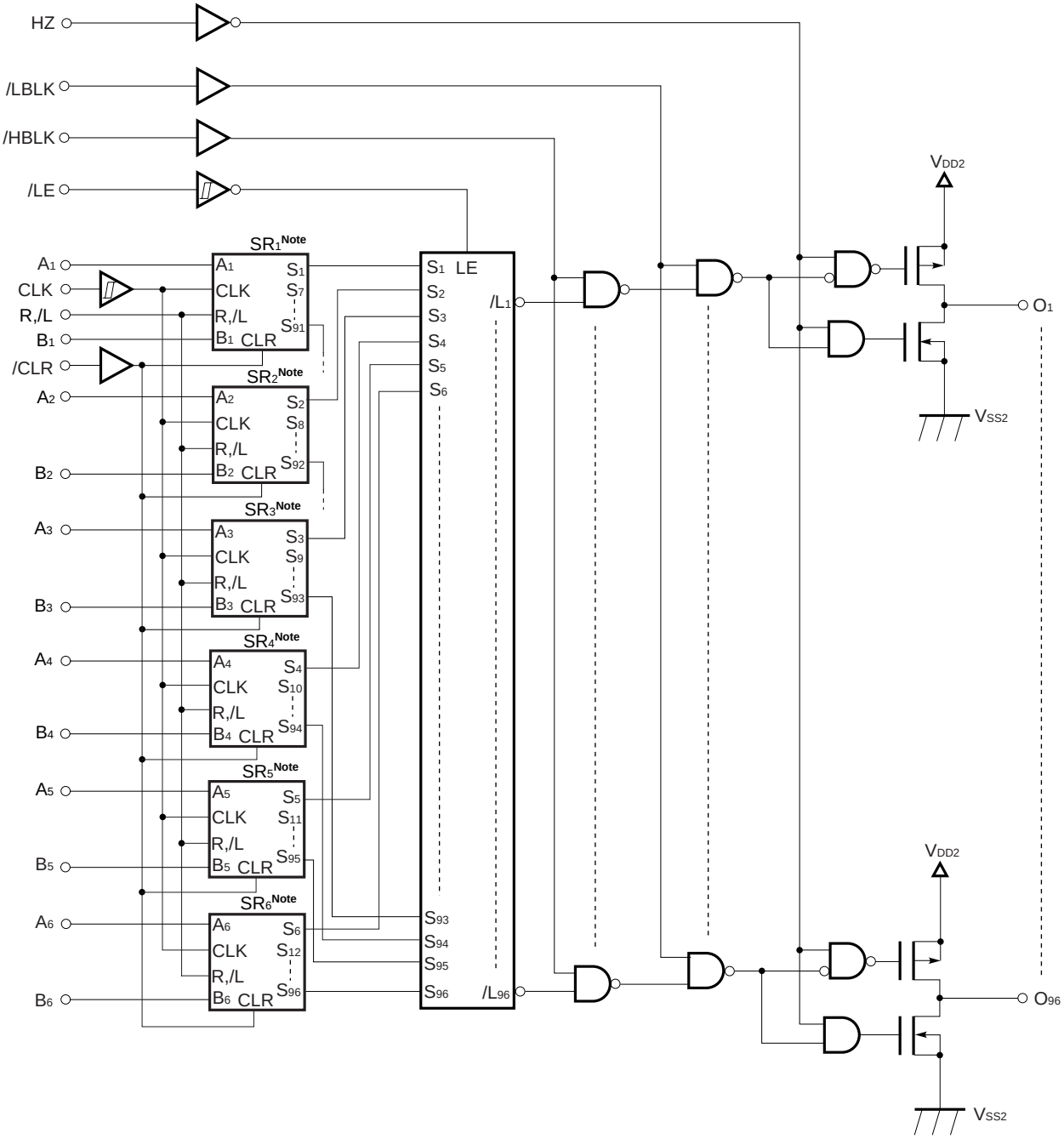
BLOCK DIAGRAM 1 (IBS = H, 3-BIT INPUT, 32-BIT LENGTH SHIFT REGISTER)



Note SR_n: 32-bit shift register

Remark /xxx indicates active low signal.

BLOCK DIAGRAM 2 (IBS = L, 6-BIT INPUT, 16-BIT LENGTH SHIFT REGISTER)



Note SRn: 16-bit shift register

PIN FUNCTIONS

Symbol	Pin Name	Description
/LBLK	Low blanking input	/LBLK = L : All output = L
/HBLK	High blanking input	/HBLK = L : All output = H
/LE	Latch enable input	Latch on a falling edge
HZ	Output high impedance	H: All output set to the high-impedance state
/CLR	Register clear input	L: All shift register data cleared to the L level
A_1-$A_{3(6)}$	RIGHT data input/output [Note]	R,/L = H, the parenthesized pins are used in 6-bit input mode. A_1-$A_{3(6)}$: Input, B_1-$B_{3(6)}$: Output
B_1-$B_{3(6)}$	LEFT data input/output [Note]	R,/L = L, the parenthesized pins are used in 6-bit input mode. A_1-$A_{3(6)}$: Output, B_1-$B_{3(6)}$: Input
CLK	Clock input	Shift on a rising edge
R,/L	Shift control input	H: Right shift mode SR_1 : $A_1 \rightarrow S_1$.....$S_{94} \rightarrow B_1$ (SR_2 and SR_3 also shift in the same direction.) Left shift mode SR_1 : $B_1 \rightarrow S_{94}$.....$S_1 \rightarrow A_1$ (SR_2 and SR_6 also shift in the same direction.)
IBS	Input mode switch	H: 32-bit shift registers, 3-bit input mode L: 16-bit shift registers, 6-bit input mode
O_1 to O_{96}	High withstand voltage output	80 V, +50/–75 mA MAX.
V_{DD1}	Logic power supply	5 V ± 10 %
V_{DD2}	Driver power supply	10 to 70 V
V_{SS1}	Logic ground	Connect to system ground
V_{SS2}	Driver ground	Connect to system ground

Note In 3-bit input mode, unused I/O pins must be held at the L level.

To use for module, the back side of IC chip must be held at the V_{SS} (GND) level.

TRUTH TABLE

Shift Register Block

Input		Output		Shift Register
R,/L	CLK	A	B	
H	↑	Input	Output [Note1]	Right shift operation performed
H	H or L		Output	Hold
L	↑	Output [Note2]	Input	Left shift operation performed
L	H or L	Output		Hold

Notes 1. On the rising edge of the clock, the data of S_{91}-S_{93} (S_{85}-S_{90}) is shifted to S_{94}-S_{96} (S_{91}-S_{96}), and is output from B_1-B_3 (B_1-B_6) (The parenthesized pins are used in 6-bit input mode.).

2. On the rising edge of the clock, the data of S_4-S_6 (S_7-S_{12}) is shifted to S_1-S_3 (S_1-S_6), and is output from A_1-A_3 (A_1-A_6) (The parenthesized pins are used in 6-bit input mode.).

Latch Block

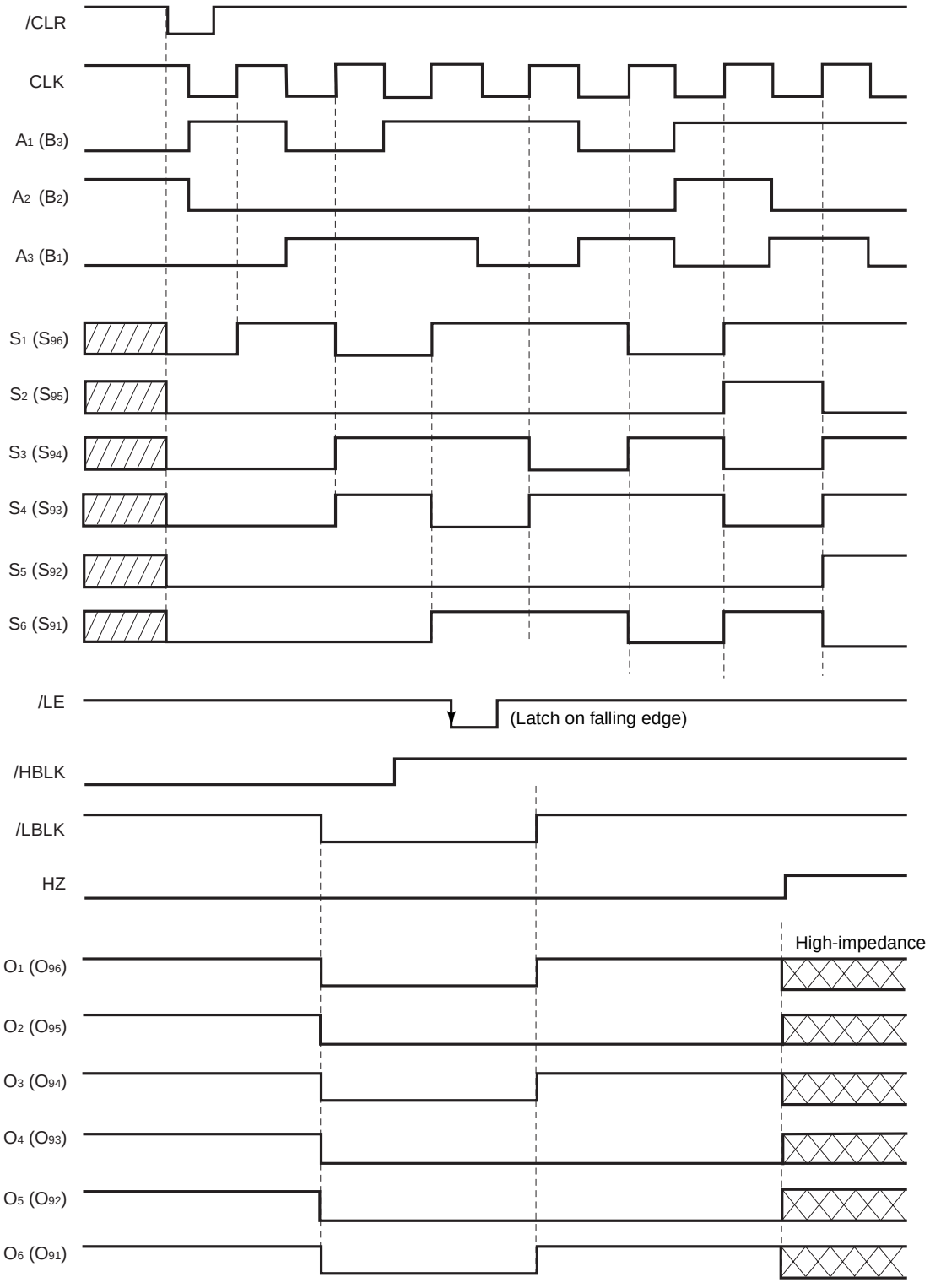
/LE	Output State of Latch Section (/L_n)
↓	Latch S_n data
H or L	Hold latch (output) data

Driver Block

A (B)	/HBLK	/LBLK	HZ	Output State of Driver Block
x	L	H	L	All driver output : H
x	x	L	L	All driver output : L
x	x	x	H	All driver output : High Impedance
L	H	H	L	L
H	H	H	L	H

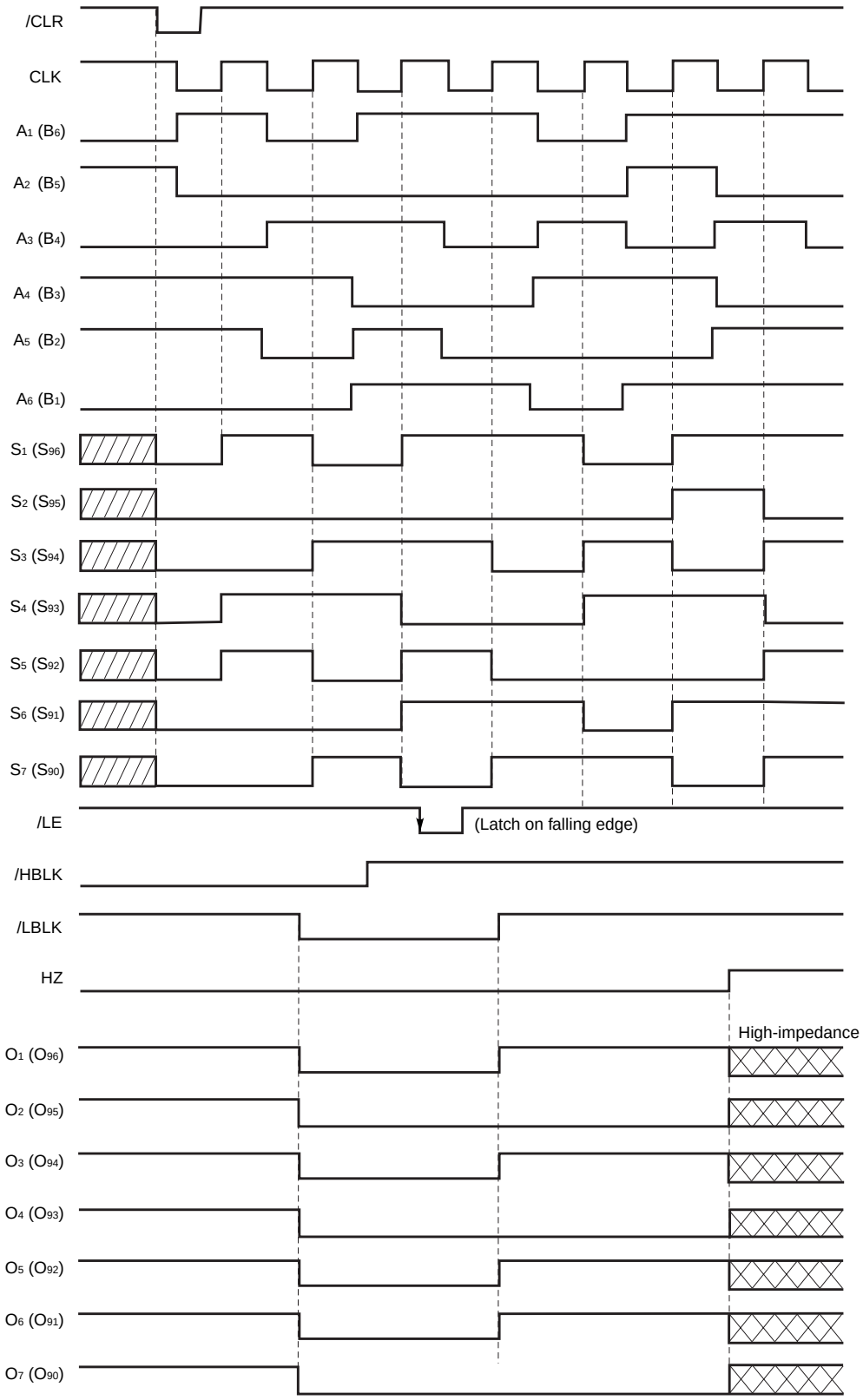
Remark x : H or L, H : High level, L : Low level

TIMING CHART 1 (IBS = H, 3-BIT INPUT, RIGHT SHIFT)



Remark Values in parentheses are when R,/L = L.

TIMING CHART 2 (IBS = L, 6-BIT INPUT, RIGHT SHIFT)



Remark Values in parentheses are when R,/L = L.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	V_{DD1}	–0.5 to +6.0	V
Driver Supply Voltage	V_{DD2}	–0.5 to +80	V
Logic Input Voltage	V_I	–0.5 to V_{DD1} + 0.5	V
Driver Output Current	I_{O2}	+50 / –75	mA
Operating Junction Temperature	T_J	+125	°C
Storage Temperature	T_{stg}	–65 to +150	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range (T_A = –40 to +85 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V_{DD1}		4.5	5.0	5.5	V
Driver Supply Voltage	V_{DD2}		15		70	V
High-Level Input Voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}		0		0.2 V_{DD1}	V
Driver Output Current	I_{OH2}				–60	mA
	I_{OL2}				+40	mA

Electrical Characteristics (T_A = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 70 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-Level Output Voltage	V_{OH1}	Logic, I_{OH1} = –1.0 mA	0.9 V_{DD1}		V_{DD1}	V
Low-Level Output Voltage	V_{OL1}	Logic, I_{OL1} = 1.0 mA	0		0.1 V_{DD1}	V
High-Level Output Voltage	V_{OH21}	O_1 to O_{96}, I_{OH2} = –1.3 mA	69			V
	V_{OH22}	O_1 to O_{96}, I_{OH2} = –13 mA	65			V
Low-Level Output Voltage	V_{OL21}	O_1 to O_{96}, I_{OL2} = 5 mA			1.0	V
	V_{OL22}	O_1 to O_{96}, I_{OL2} = 40 mA			10	V
Input Leakage Current	I_{IL}	V_1 = V_{DD1} or V_{SS1}			±1.0	μA
High-Level Intput Voltage	V_{IH}		0.7 V_{DD1}			V
Low-Level Input Voltage	V_{IL}				0.2 V_{DD1}	V
★ Static Current Dissipation	I_{DD1}	Logic, T_A = –40 to +85 °C			500	μA
★		Logic, T_A = 25 °C			300	μA
	I_{DD2}	Driver, T_A = –40 to +85 °C			1000	μA
		Driver, T_A = 25 °C			100	μA

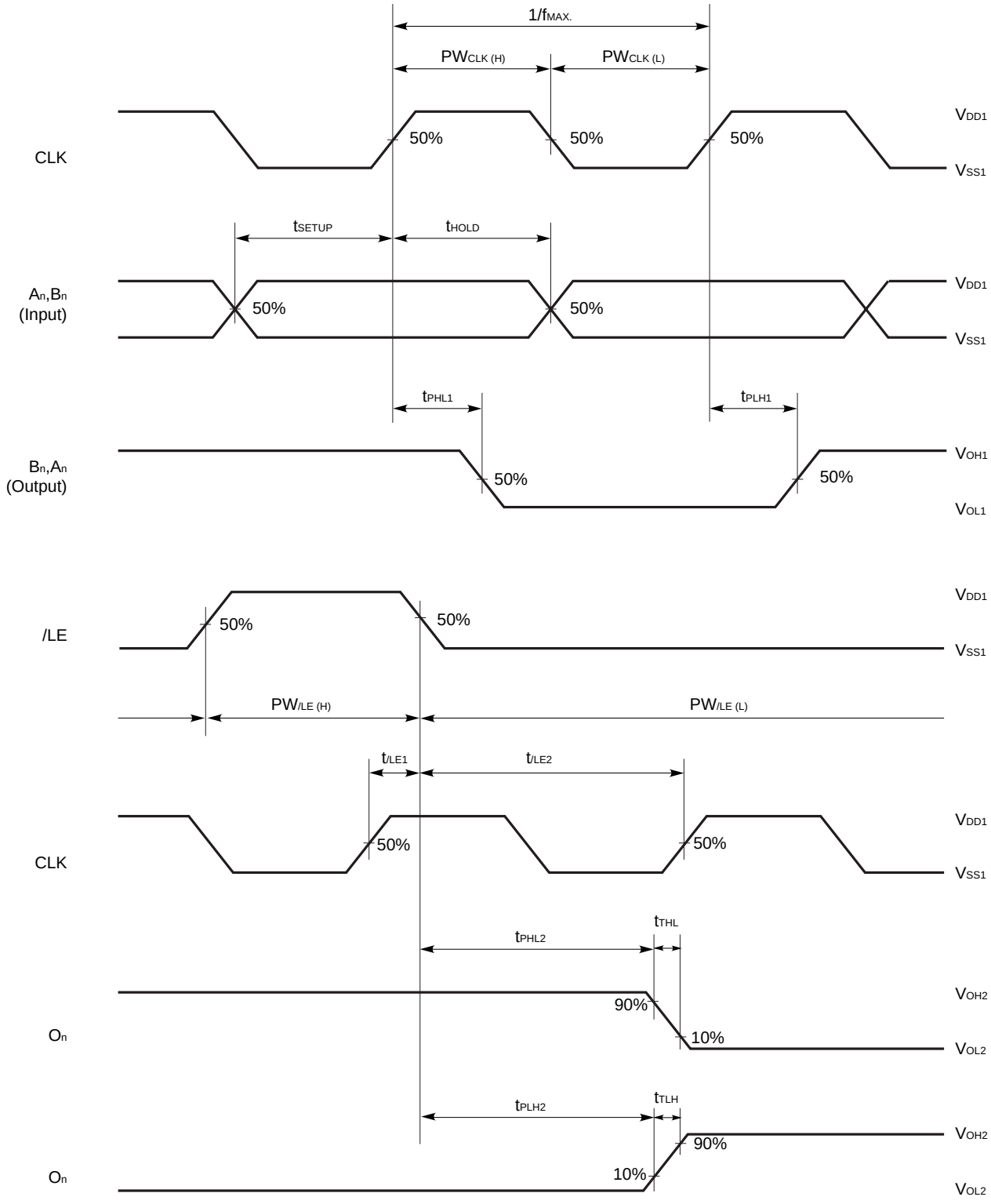
Switching Characteristics (T_A = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 70 V, V_{SS1} = V_{SS2} = 0 V, Logic C_L = 15 pF, Driver C_L = 50 pF, t_r = t_f = 6.0 ns)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Propagation Delay Time	t_{PHL1}	CLK ↑ → A/B			34	ns
	t_{PLH1}				34	ns
	t_{PHL2}	/LE ↓ → O_1 to O_{96}			180	ns
	t_{PLH2}				180	ns
	t_{PHL3}	/HBLK → O_1 to O_{96}			165	ns
	t_{PLH3}				165	ns
	t_{PHL4}	/LBLK → O_1 to O_{96}			160	ns
	t_{PLH4}				160	ns
	t_{PHZ}	HZ → O_1 to O_{96}, R_L = 10 kΩ			300	ns
	t_{PZH}				180	ns
	t_{PLZ}				300	ns
	t_{PZL}				180	ns
Rise Time	t_{TLH}	O_1 to O_{96}			120	ns
	t_{TLZ}	O_1 to O_{96}, R_L = 10 kΩ			3	μs
	t_{TZH}				120	ns
Fall Time	t_{THL}	O_1 to O_{96}			150	ns
	t_{THZ}	O_1 to O_{96}, R_L = 10 kΩ			3	μs
	t_{TZL}				150	ns
Maximum Clock Frequency	$f_{MAX.}$	Data latch, duty = 50 %	40			MHz
		Cascade connection,Duty = 50 %	25			MHz
Input Capacitance	C_I				15	pF

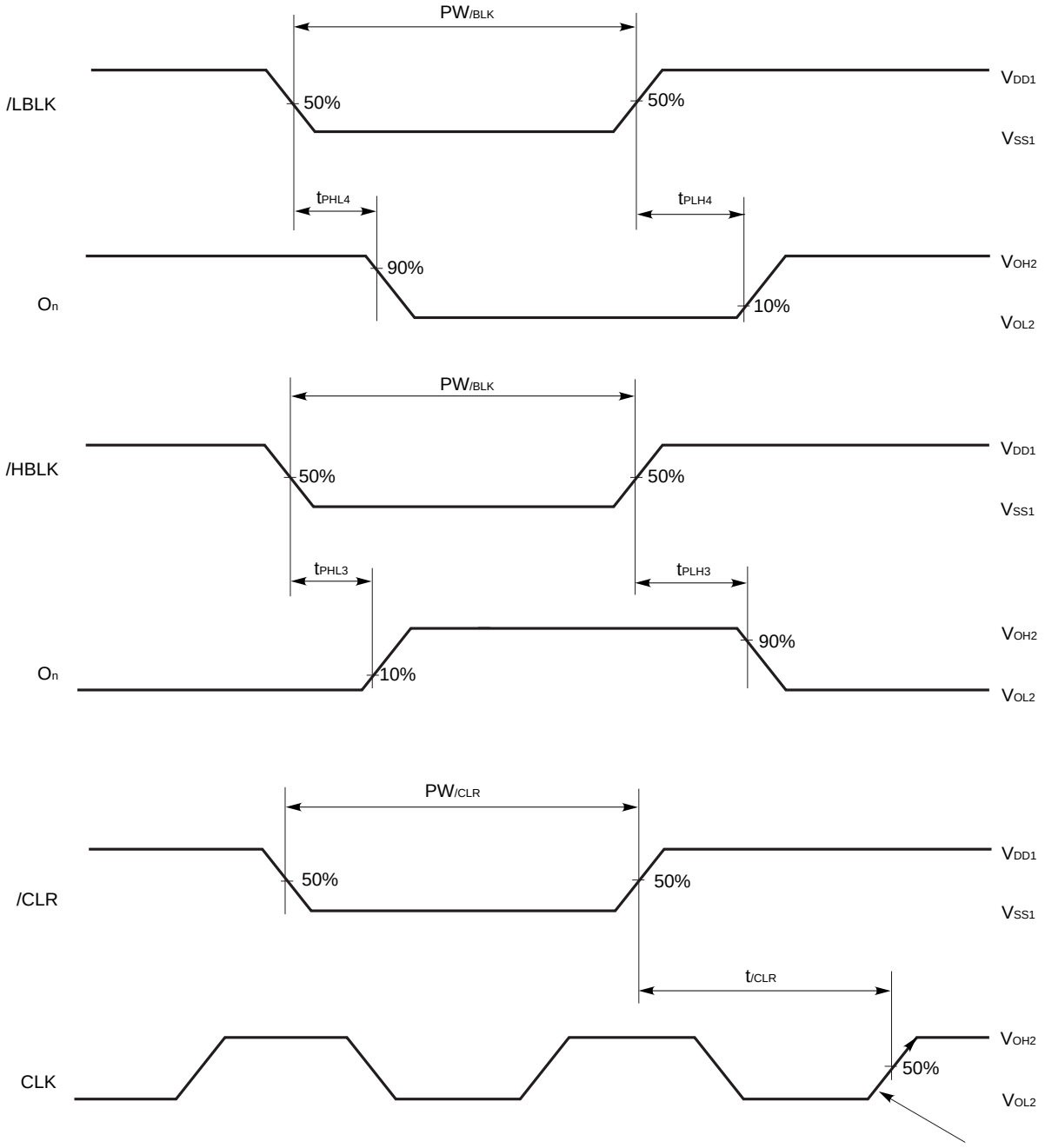
Timing Requirement (T_A = –40 to +85 °C, V_{DD1} = 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 6.0 ns)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	$PW_{CLK(H)}$ $PW_{CLK(L)}$		12			ns
Latch Enable Pulse Width	$PW_{/LE(H)}$ $PW_{/LE(L)}$		12			ns
Blank Pulse Width	$PW_{/BLK}$	/HBLK, /LBLK	200			ns
HZ Pulse Width	PW_{HZ}	R_L = 10 kΩ	3.3			μs
/CLR Pulse Width	$PW_{/CLR}$		12			ns
Data Setup Time	t_{SETUP}		4			ns
Data Hold Time	t_{HOLD}		6			ns
Latch Enable Time	$t_{/LE1}$		12			ns
	$t_{/LE2}$		12			ns
★ /CLR Timing	$t_{/CLR}$		6			ns

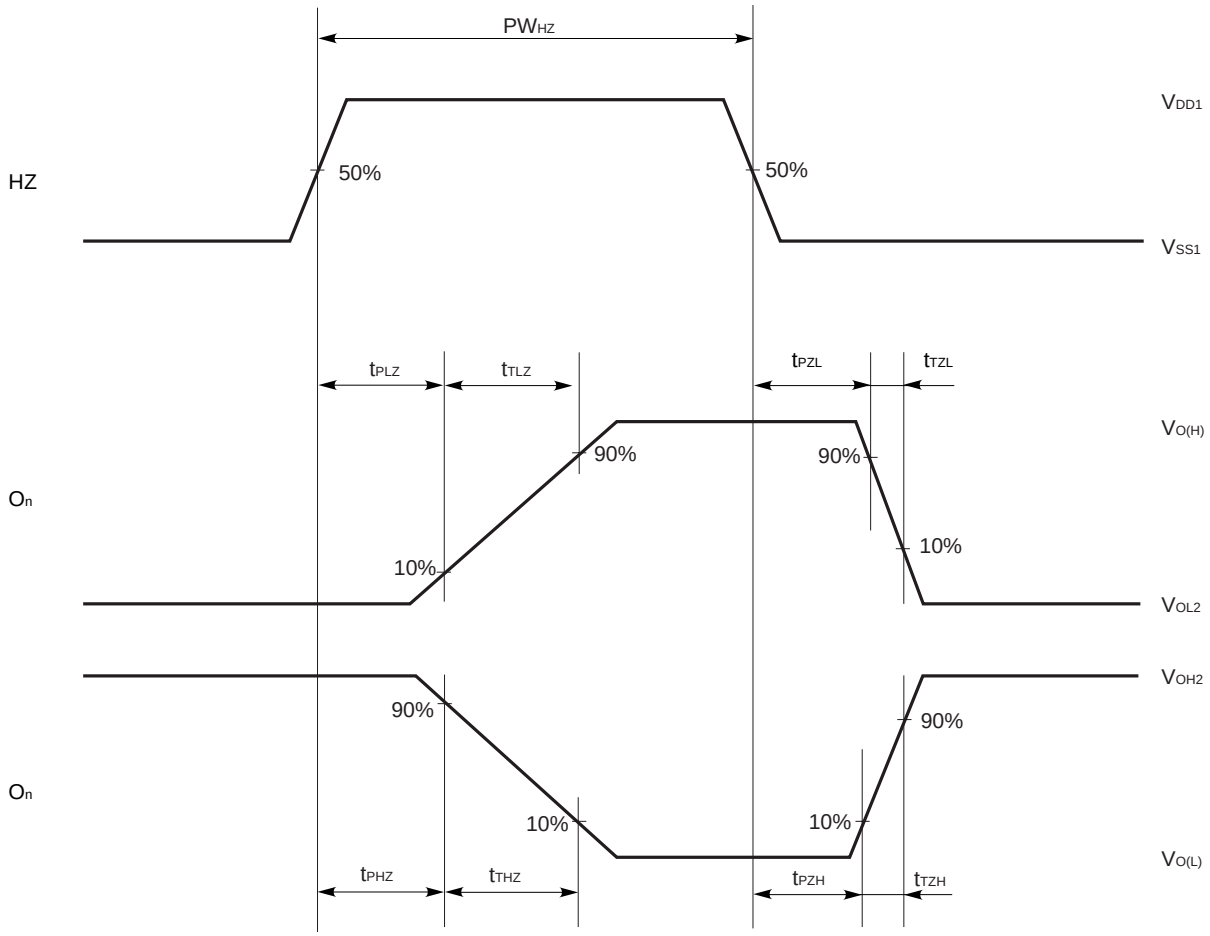
Switching Characteristics Waveform (1/3)



★ **Switching Characteristics Waveform (2/3)**



Switching Characteristics Waveform (3/3)



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System(C10983E)

Quality Grades to NEC's Semiconductor Devices(C11531E)

- **The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.**
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.
- NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.
- Descriptions of circuits, software, and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software, and information in the design of the customer's equipment shall be done under the full responsibility of the customer. NEC Corporation assumes no responsibility for any losses incurred by the customer or third parties arising from the use of these circuits, software, and information.
- While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.
- NEC devices are classified into the following three quality grades:
  "Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

  The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

M7 98.8