NEC

MOS INTEGRATED CIRCUIT
μPD16347

192-BIT AC-PDP DRIVER

DESCRIPTION

The μPD16347 is a high-withstanding-voltage CMOS driver designed for use with a flat display panel such as a PDP, VFD, or EL panel. It consists of a 192-bit bi-directional shift register, 192-bit latch and high-withstanding-voltage CMOS driver. The logic block operates with a 5.0 V power supply and 3.3 V interface so that it can be directly connected to a gate array and microcomputer. The driver block provides a high-withstanding-voltage output: 80 V.

The logic and driver blocks are made of CMOS circuits, consuming lower power.

FEATURES

- 3-ch, 4-ch, 6-ch and 6-ch (3-ch + 3-ch) input port switching is possible using the IBS1 and IBS2 pins
- Many outputs: 192-bit output
- Clock transfer is switchable via the SDS pin between single edge and double edge
- Data control with transfer clock (external) and latch
- High-speed data transfer: f_{CLK} = 60 MHz MAX. (at loading of data)
- On-chip chip temperature detection circuit
- High withstanding voltage and high drive output: 80 V MAX., +15/–30 mA MAX.
- 3.3 V input interface (V_{DD1} = 5.0 V)
- High-withstanding-voltage CMOS structure

ORDERING INFORMATION

Part Number	Package
μPD16347N-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, please contact one of our sales representatives.

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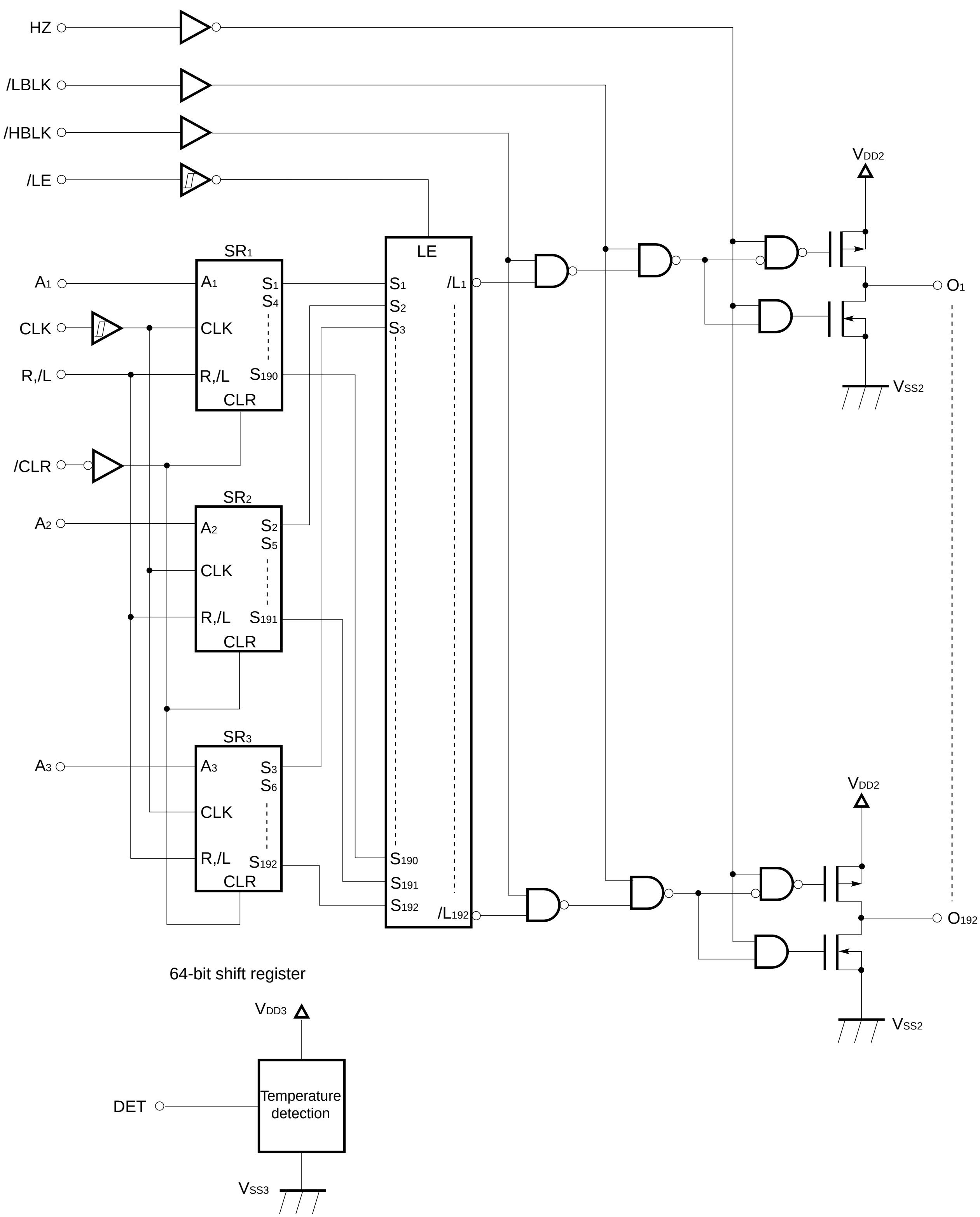
The mark ★ shows major revised points.

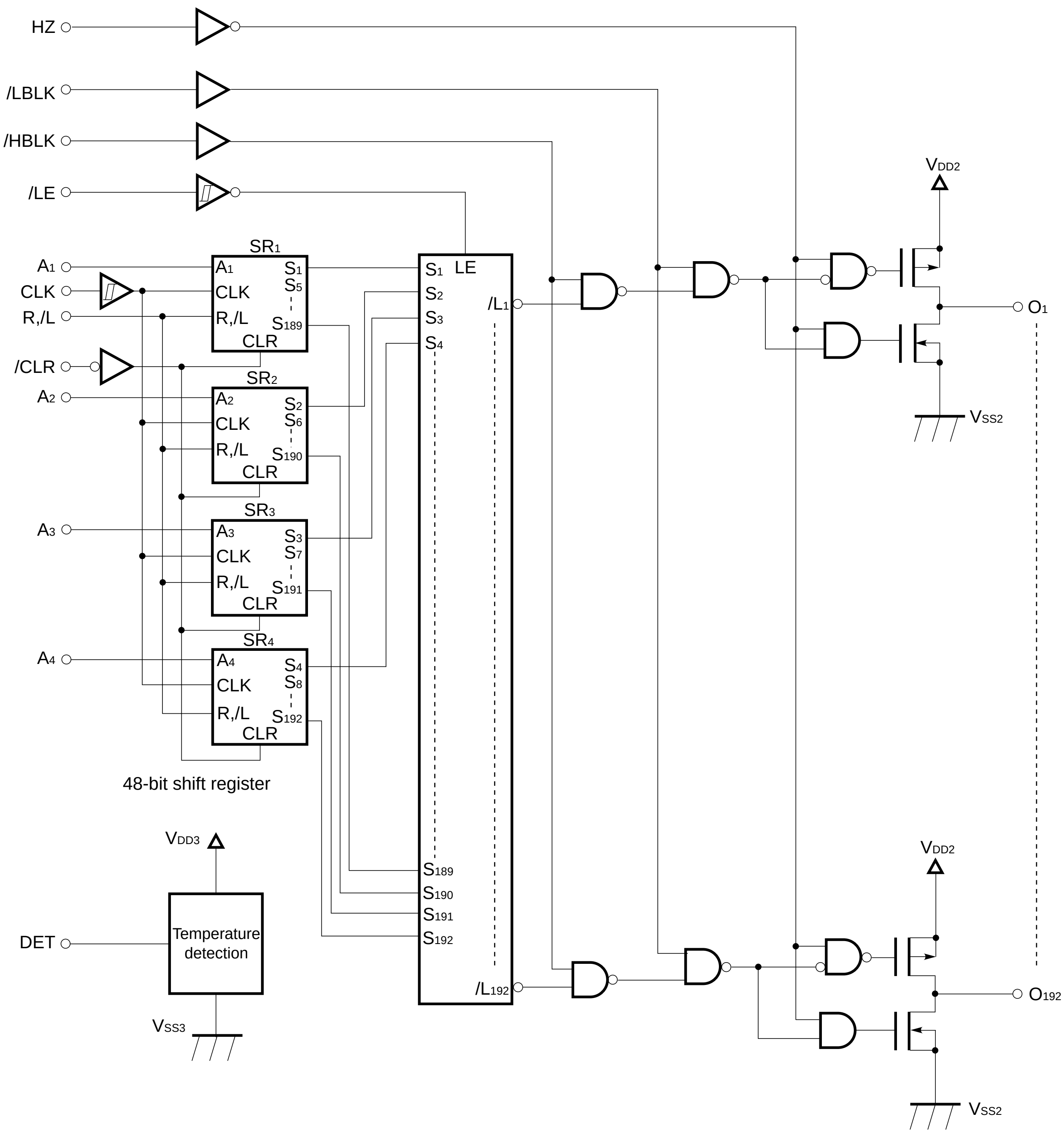
1. BLOCK DIAGRAM

(1) IBS1 = L, IBS2 = H: 3-bit input

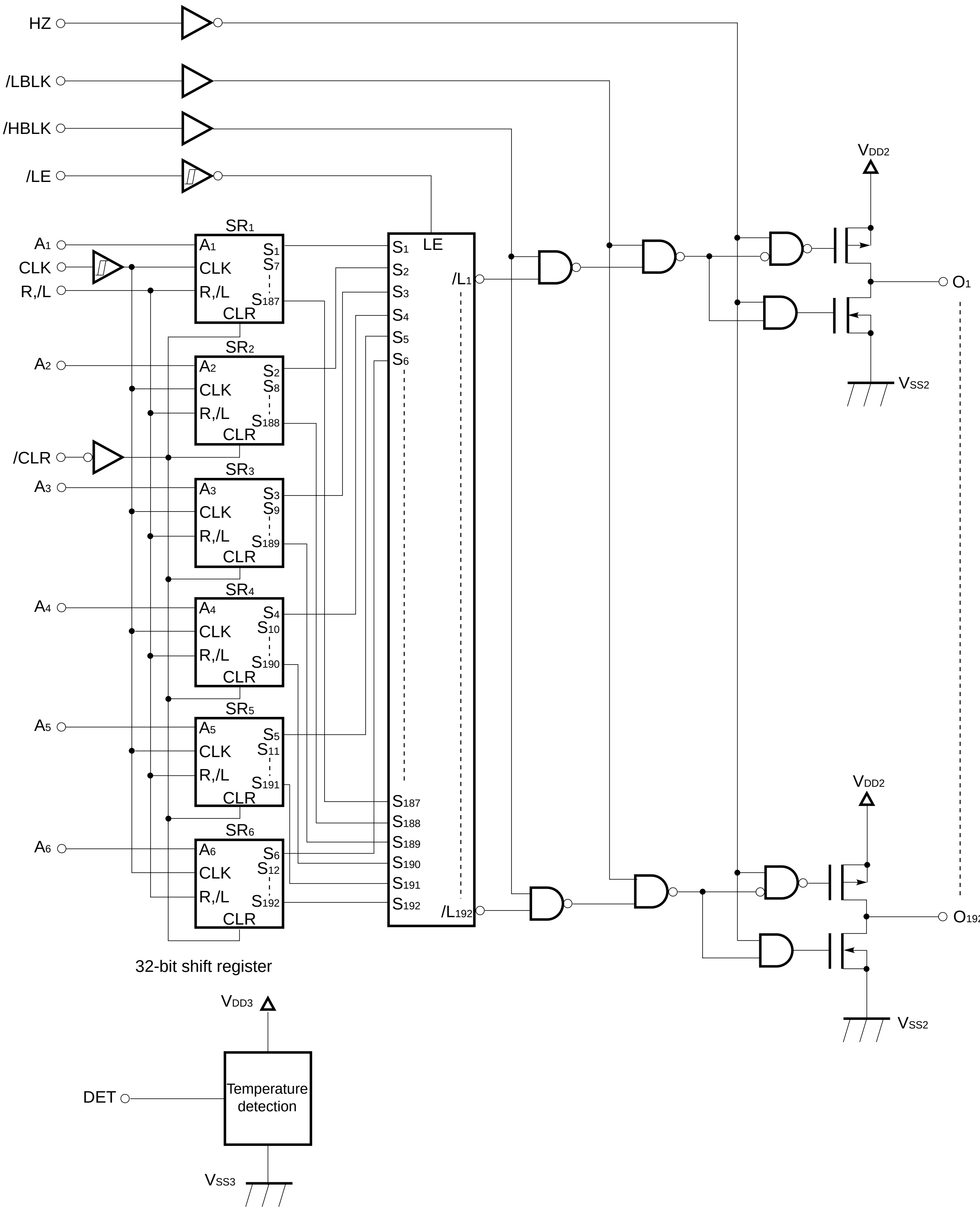


Remark /xxx indicates active low signal.

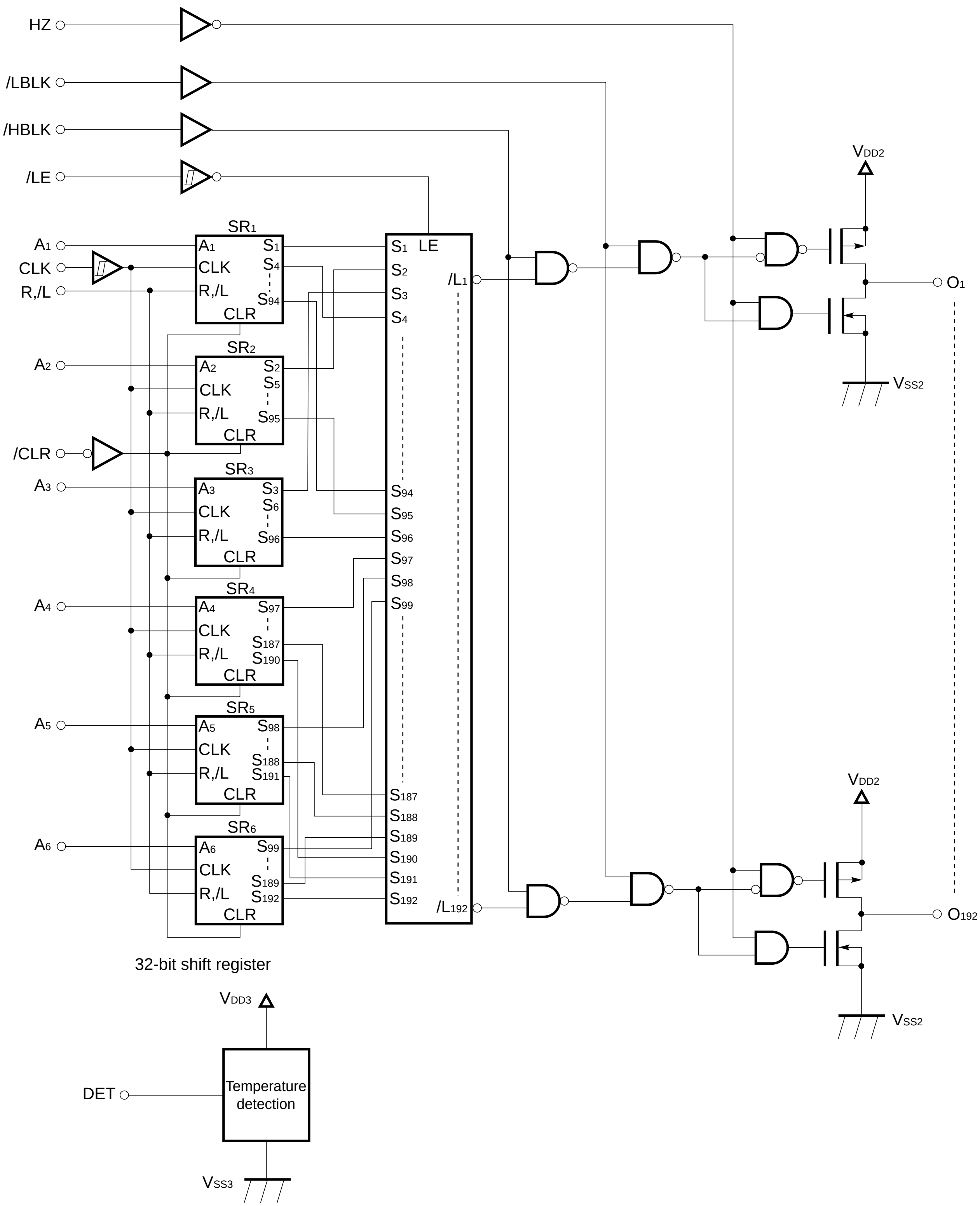
(2) IBS1 = L, IBS2 = L: 4-bit input



(3) IBS1 = H, IBS2 = L: 6-bit input

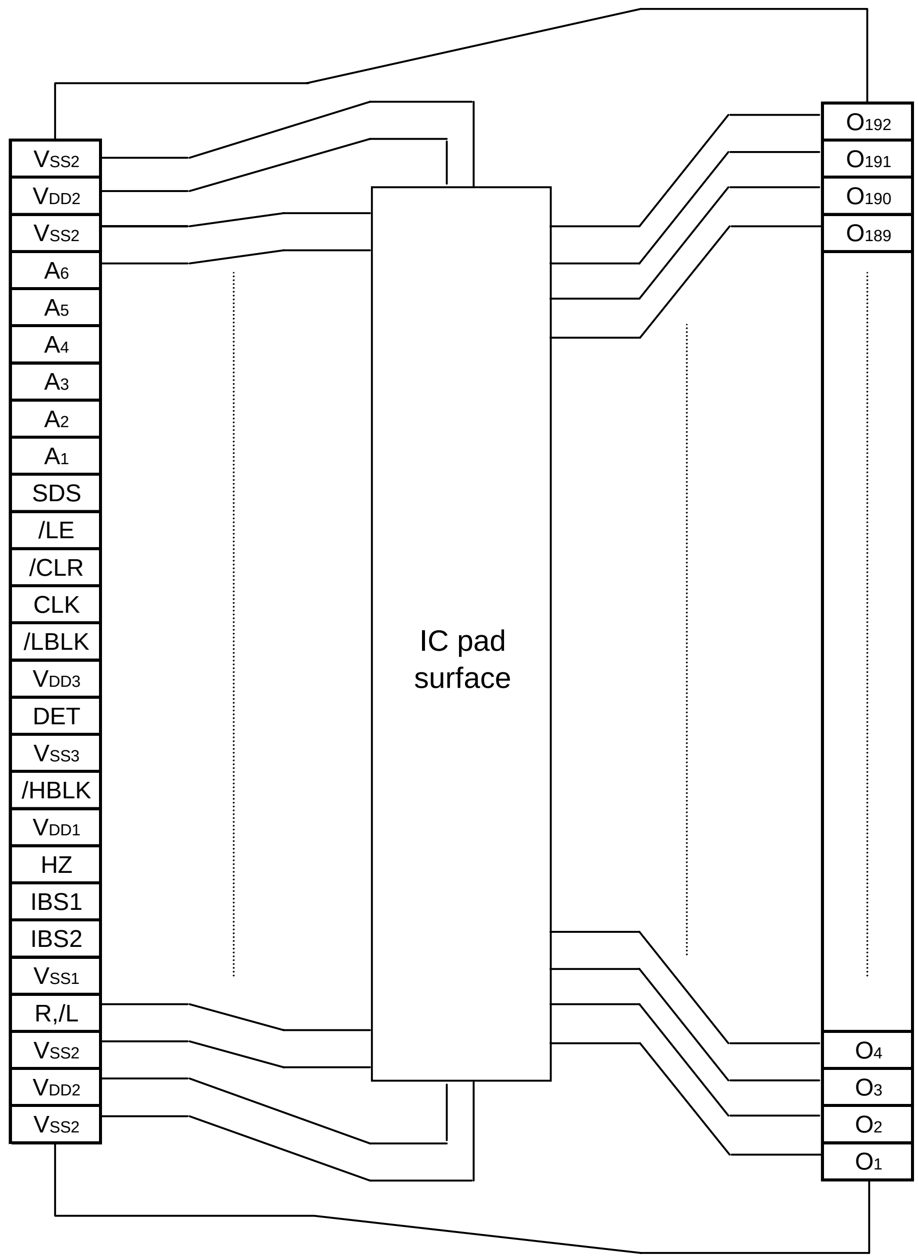


(4) IBS1 = H, IBS2 = H: 6-bit (3-bit + 3-bit) input



2. PIN CONFIGURATION (IC pad surface)

μPD16347N-xxx: TCP (TAB package)



Remark This figure does not specify the TCP package.

3. PIN FUNCTIONS

Symbol	Pin Name	I/O	Description
/LBLK	Low blanking	Input	/LBLK = L: All output = L
/HBLK	High blanking	Input	/HBLK = L: All output = H
/LE	Latch enable	Input	Latch operation performed at the falling edge.
HZ	Output high impedance	Input	HZ = H: All output set to the high-impedance state
/CLR	Register clear	Input	/CLR = L: All shift register data cleared to the low level
A_1 to $A_{3\ (6)}$	Data	Input	The A_1 to $A_{3\ (6)}$ are Data input pins. The data shift direction is switched inside the R,/L pin.
CLK	Clock	Input	SDS = H: Shift operation is executed at the rising and falling edges SDS = L: Shift operation is executed at the rising edge
R,/L	Shift direction control	Input	The shift direction control pin of shift register. The shift directions of the shift register are as follows. R,/L = H (right shift): SR_1: $A_1 \rightarrow S_1 ... S_{190}$ (SR_2 to SR_6 also shift in the same direction.) R,/L = L (left shift): SR_1: $A_1 \rightarrow S_{190} ... S_1$ (SR_2 to SR_6 also shift in the same direction.) Refer to **5. INTERNAL REGISTER.**
IBS1, IBS2	Input mode switch	Input	IBS1 = H, IBS2 = H: 6-bit (3-bit + 3-bit) input, Length of shift register: 32-bit IBS1 = H, IBS2 = L: 6-bit input, Length of shift register: 32-bit IBS1 = L, IBS2 = H: 3-bit input, Length of shift register: 64-bit IBS1 = L, IBS2 = L: 4-bit input, Length of shift register: 48-bit
DET	Temperature detection	Output	The DET is N-ch open-drain output. Low level is output (N-ch transistor: ON) via temperature detection.
SDS	Clock edge switch	Input	SDS = H: Shift operation is executed at the rising and falling edges of CLK (double edge) SDS = L: Shift operation is executed at the rising edge of CLK (single edge)
O_1 to O_{192}	High withstanding voltage	Output	70 V
V_{DD1}	Logic power supply	–	5 V ± 5%
V_{DD2}	Driver power supply	–	15 to 70 V
V_{DD3}	Temperature detection power supply	–	5 V ± 10%
V_{SS1}	Logic ground	–	Connect to system ground
V_{SS2}	Driver ground	–	Connect to system ground
V_{SS3}	Temperature detection ground	–	Connect to system ground

Caution In 3-bit and 4-bit input mode, unused input pins must be held at the low level or high level.

4. TRUTH TABLE

Shift Register Block

Input			Shift Register
R,/L	SDS	CLK	
H	H	↑ or ↓	Right shift operation is executed.
H	H	H or L	Hold
H	L	↑	Right shift operation is executed.
H	L	H or L	Hold
L	H	↑ or ↓	Left shift operation is executed.
L	H	H or L	Hold
L	L	↑	Left shift operation is executed.
L	L	H or L	Hold

Latch Block

/LE	Output State of Latch Section (/L_n)
↓	Latch S_n data
H or L	Hold latch (output) data

Driver Block

A	/HBLK	/LBLK	HZ	Output State of Driver Block
				O_1 to O_{192}
x	L	H	L	All driver output: H
x	x	L	L	All driver output: L
x	x	x	H	All driver output: High-impedance
L	H	H	L	L
H	H	H	L	H

Remark x: H or L

5. INTERNAL REGISTER

Shift Direction (R,/L = H, right shift)

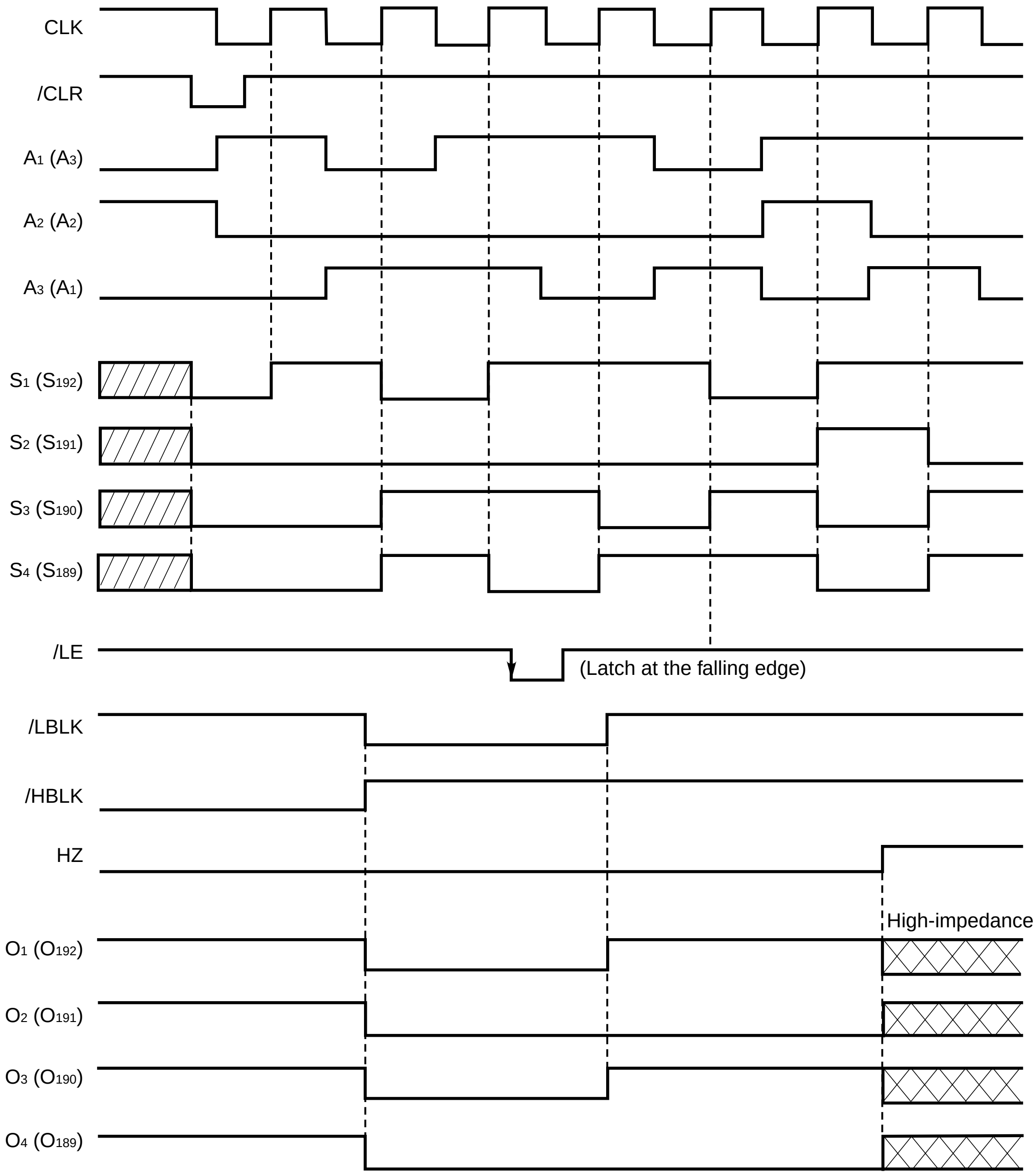
	3-bit input	4-bit input	6-bit input	6-bit (3-bit + 3-bit) input
SR_1 (A_1 input register)	$A_1 \rightarrow S_1, S_4 \dots S_{190}$	$A_1 \rightarrow S_1, S_5 \dots S_{189}$	$A_1 \rightarrow S_1, S_7 \dots S_{187}$	$A_1 \rightarrow S_1, S_4 \dots S_{94}$
SR_2 (A_2 input register)	$A_2 \rightarrow S_2, S_5 \dots S_{191}$	$A_2 \rightarrow S_2, S_6 \dots S_{190}$	$A_2 \rightarrow S_2, S_8 \dots S_{188}$	$A_2 \rightarrow S_2, S_5 \dots S_{95}$
SR_3 (A_3 input register)	$A_3 \rightarrow S_3, S_6 \dots S_{192}$	$A_3 \rightarrow S_3, S_7 \dots S_{191}$	$A_3 \rightarrow S_3, S_9 \dots S_{189}$	$A_3 \rightarrow S_3, S_6 \dots S_{96}$
SR_4 (A_4 input register)		$A_4 \rightarrow S_4, S_8 \dots S_{192}$	$A_4 \rightarrow S_4, S_{10} \dots S_{190}$	$A_4 \rightarrow S_{97}, S_{100} \dots S_{190}$
SR_5 (A_5 input register)			$A_5 \rightarrow S_5, S_{11} \dots S_{191}$	$A_5 \rightarrow S_{98}, S_{101} \dots S_{191}$
SR_6 (A_6 input register)			$A_6 \rightarrow S_6, S_{12} \dots S_{192}$	$A_6 \rightarrow S_{99}, S_{102} \dots S_{192}$

Shift Direction (R,/L = L, left shift)

	3-bit input	4-bit input	6-bit input	6-bit (3-bit + 3-bit) input
SR_1 (A_1 input register)	$A_1 \rightarrow S_{190}, S_{187} \dots S_1$	$A_1 \rightarrow S_{189}, S_{185} \dots S_1$	$A_1 \rightarrow S_{187}, S_{181} \dots S_1$	$A_1 \rightarrow S_{94}, S_{91} \dots S_1$
SR_2 (A_2 input register)	$A_2 \rightarrow S_{191}, S_{188} \dots S_2$	$A_2 \rightarrow S_{190}, S_{186} \dots S_2$	$A_2 \rightarrow S_{188}, S_{182} \dots S_2$	$A_2 \rightarrow S_{95}, S_{92} \dots S_2$
SR_3 (A_3 input register)	$A_3 \rightarrow S_{192}, S_{189} \dots S_3$	$A_3 \rightarrow S_{191}, S_{187} \dots S_3$	$A_3 \rightarrow S_{189}, S_{183} \dots S_3$	$A_3 \rightarrow S_{96}, S_{93} \dots S_3$
SR_4 (A_4 input register)		$A_4 \rightarrow S_{192}, S_{188} \dots S_4$	$A_4 \rightarrow S_{190}, S_{184} \dots S_4$	$A_4 \rightarrow S_{190}, S_{187} \dots S_{97}$
SR_5 (A_5 input register)			$A_5 \rightarrow S_{191}, S_{185} \dots S_5$	$A_5 \rightarrow S_{191}, S_{188} \dots S_{98}$
SR_6 (A_6 input register)			$A_6 \rightarrow S_{192}, S_{186} \dots S_6$	$A_6 \rightarrow S_{192}, S_{189} \dots S_{99}$

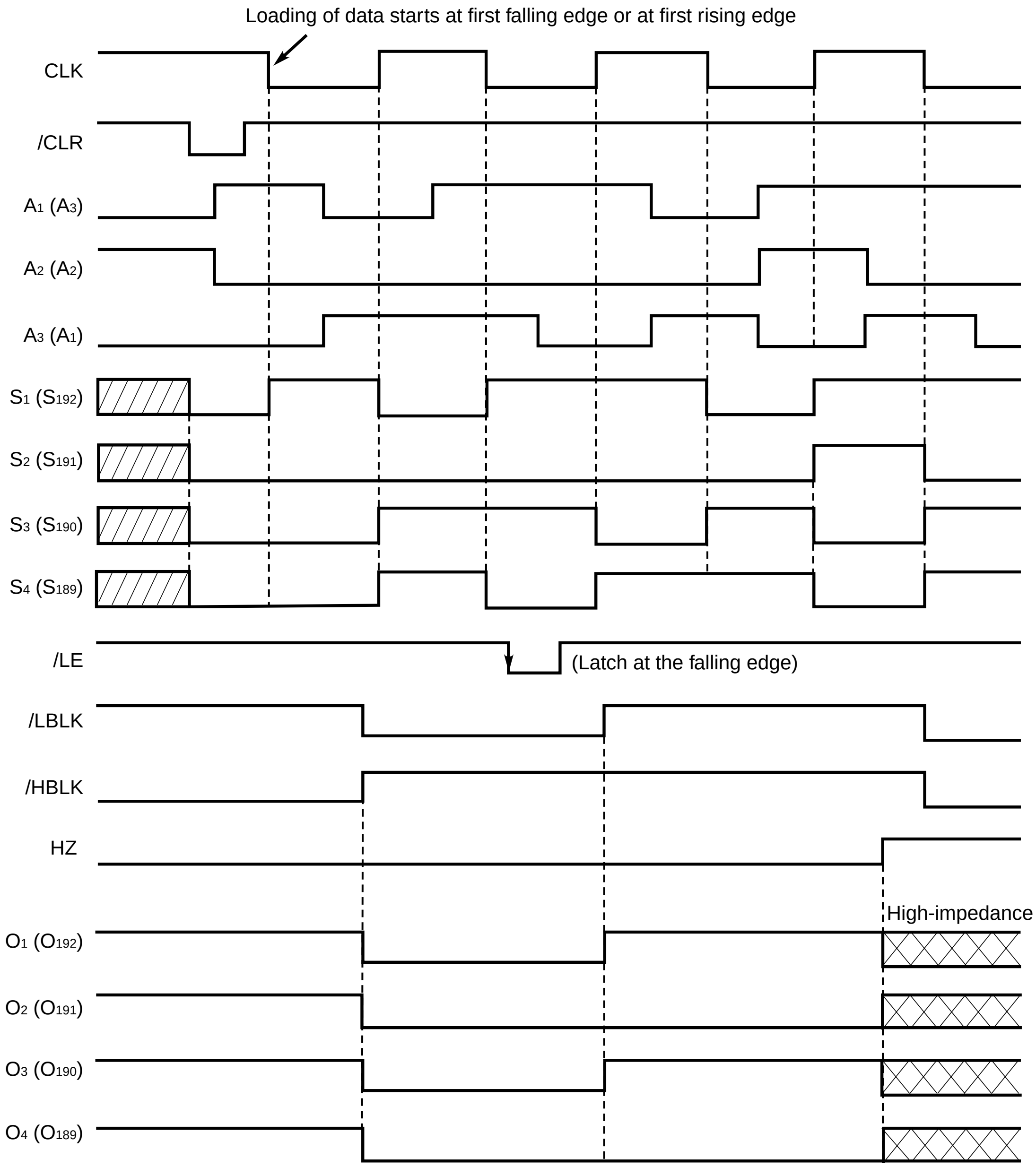
6. TIMING CHART

(1) IBS1 = L, IBS2 = H: 3-bit input, SDS = L: single edge



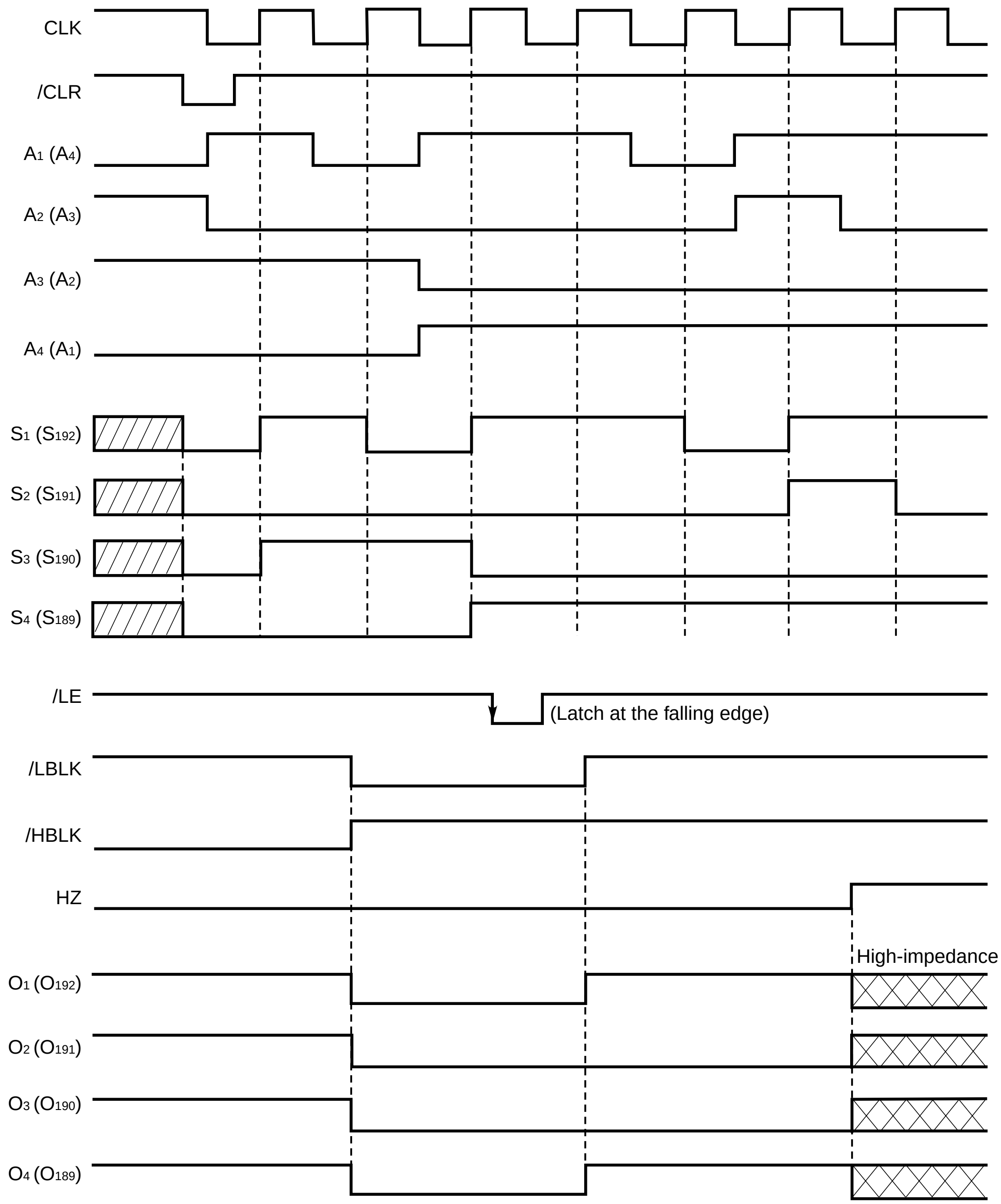
Remark Values in parentheses are when R,/L = L.

(2) IBS1 = L, IBS2 = H: 3-bit input, SDS = H: double edge



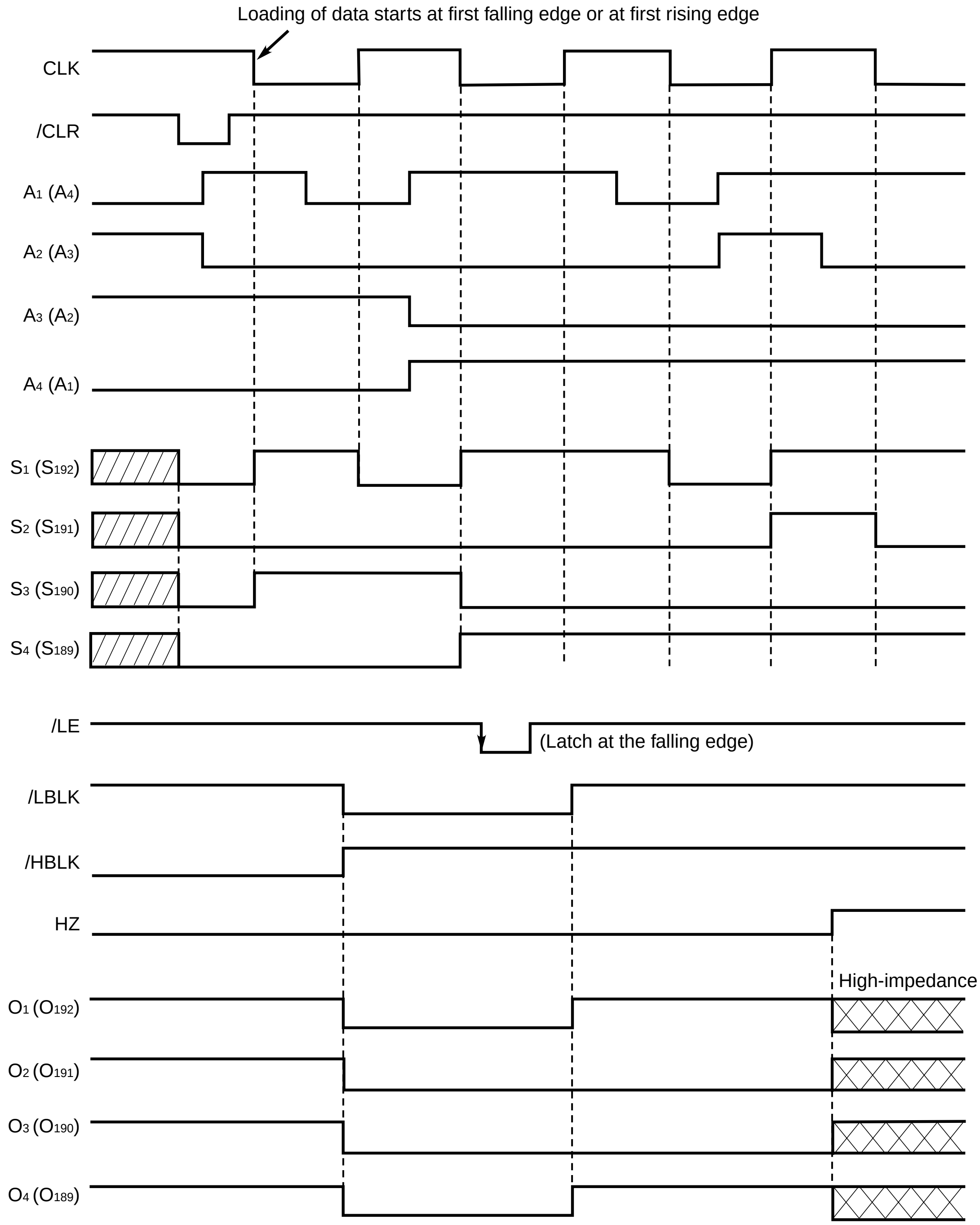
Remark Values in parentheses are when R,/L = L.

(3) IBS1 = L, IBS2 = L: 4-bit input, SDS = L: single edge



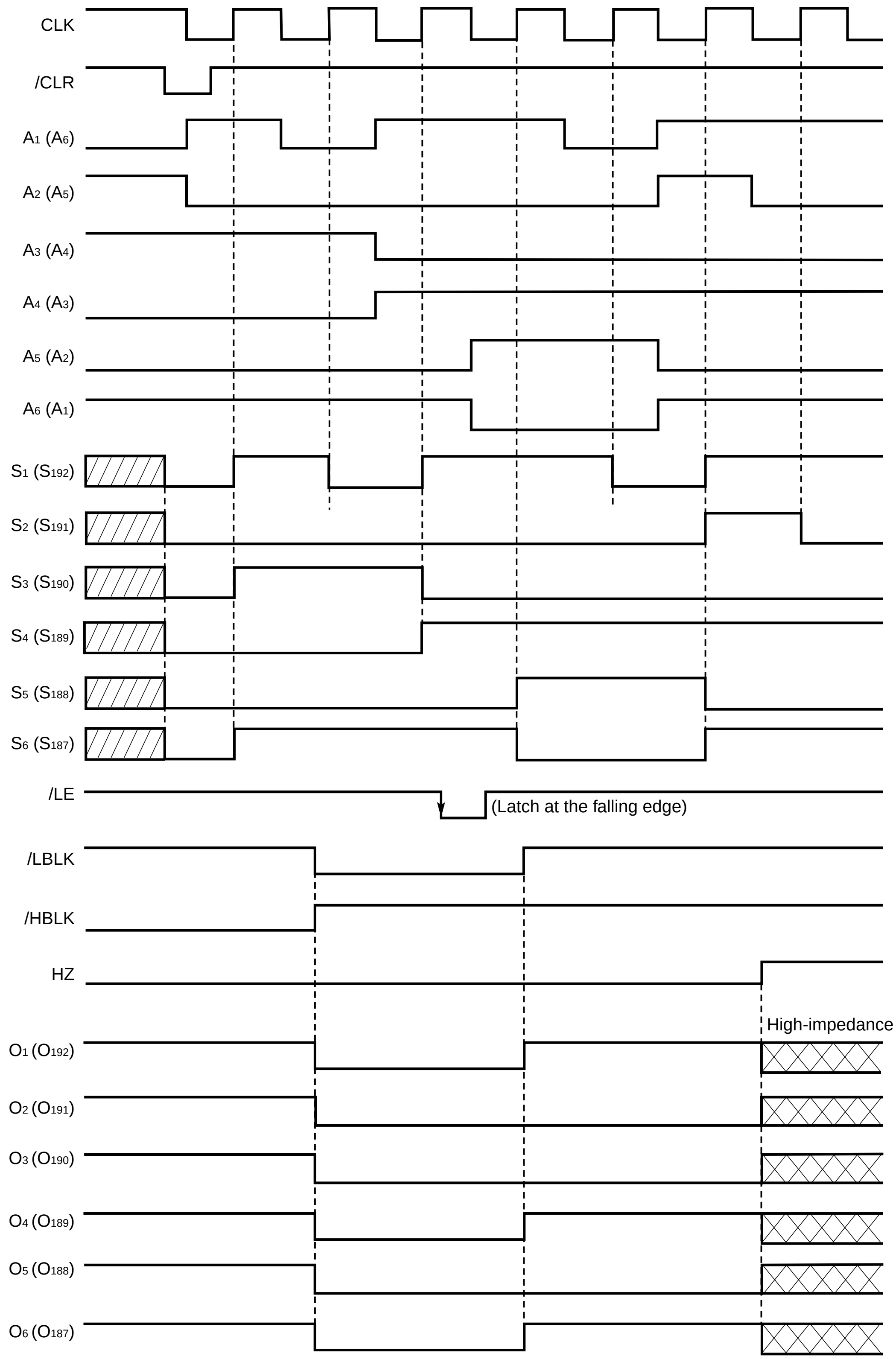
Remark Values in parentheses are when R,/L = L.

(4) IBS1 = L, IBS2 = L: 4-bit input, SDS = H: double edge



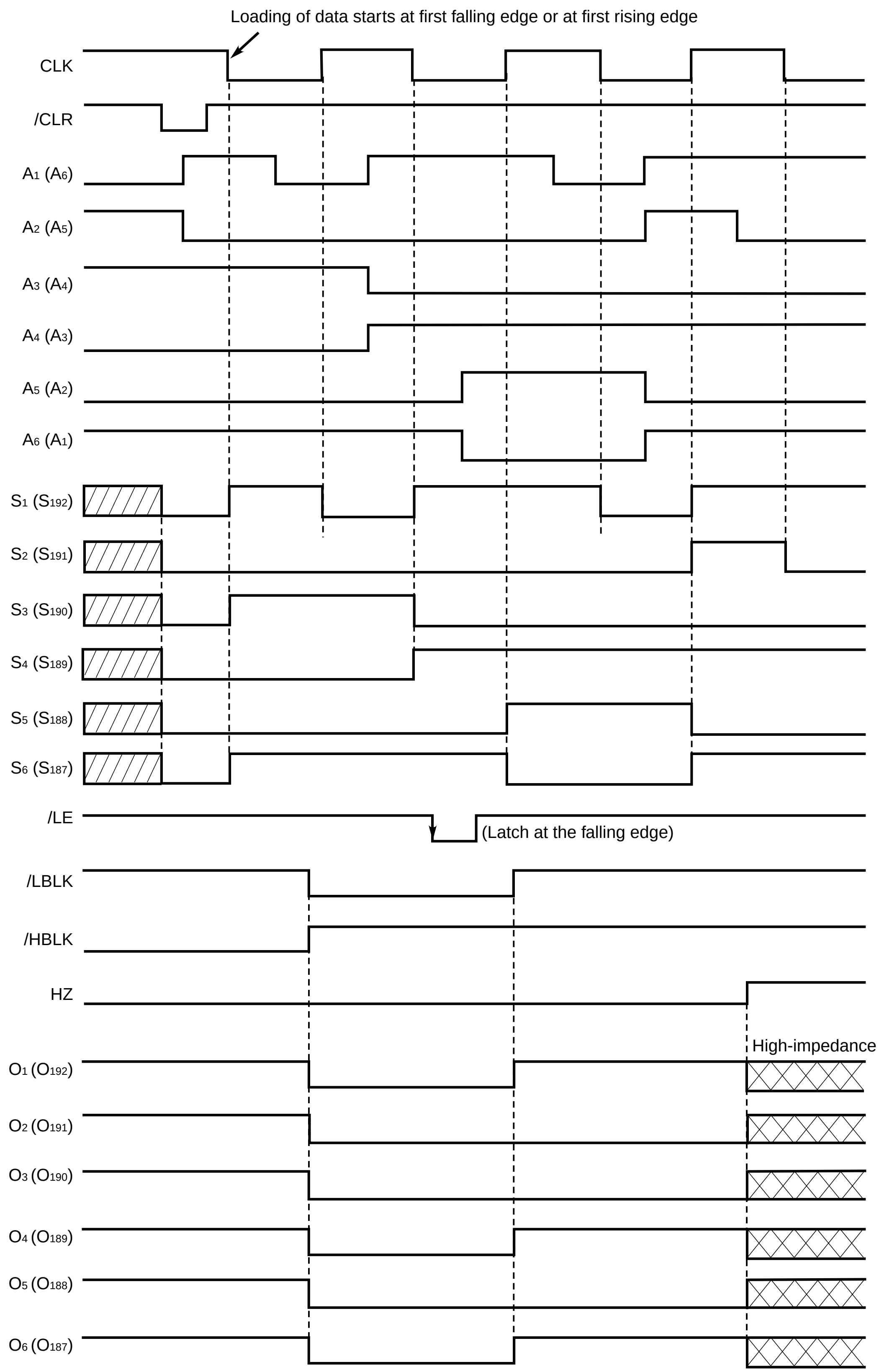
Remark Values in parentheses are when R,/L = L.

(5) IBS1 = H, IBS2 = L: 6-bit input, SDS = L: single edge



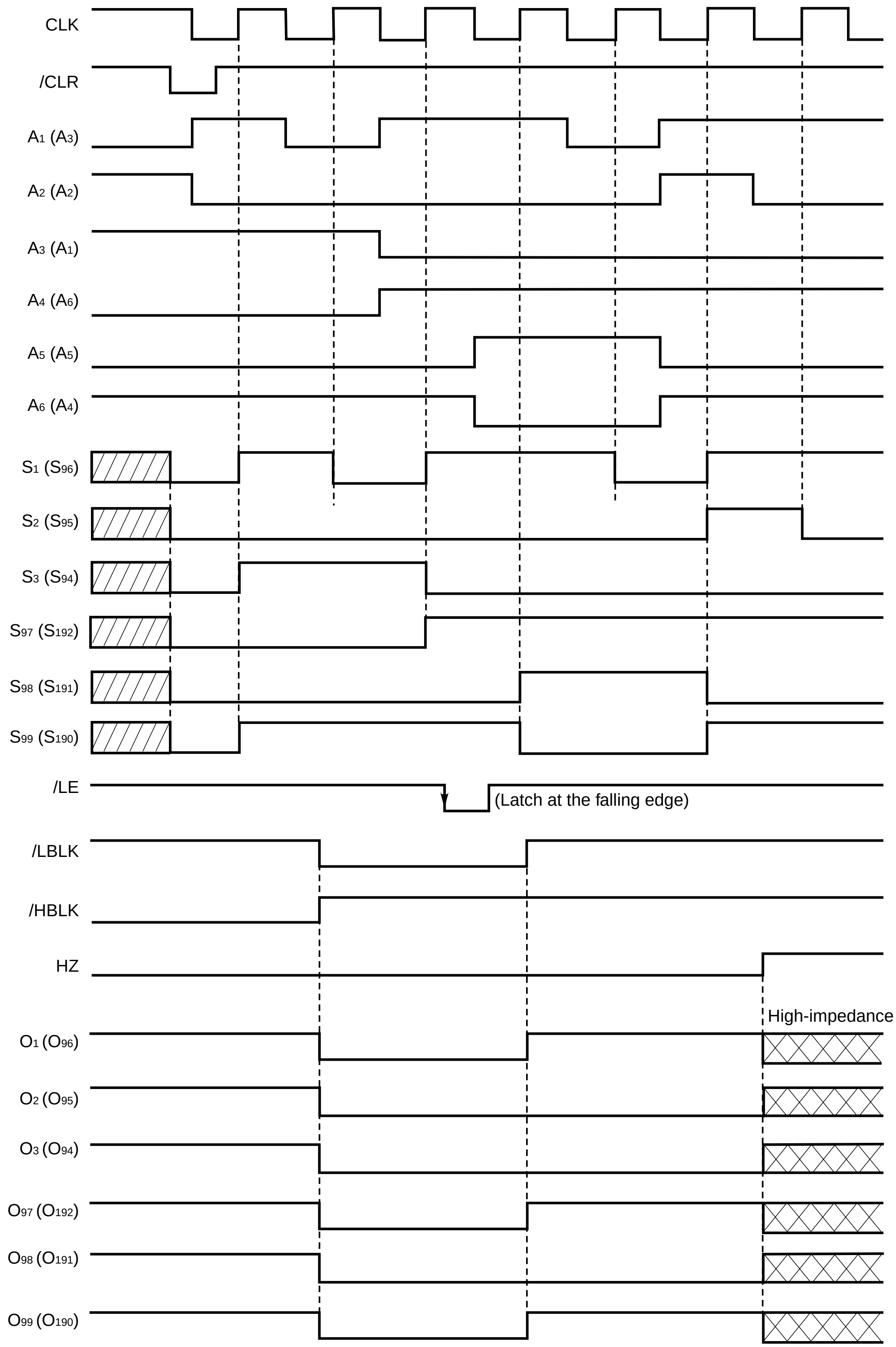
Remark Values in parentheses are when R,/L = L.

(6) IBS1 = H, IBS2 = L: 6-bit input, SDS = H: double edge



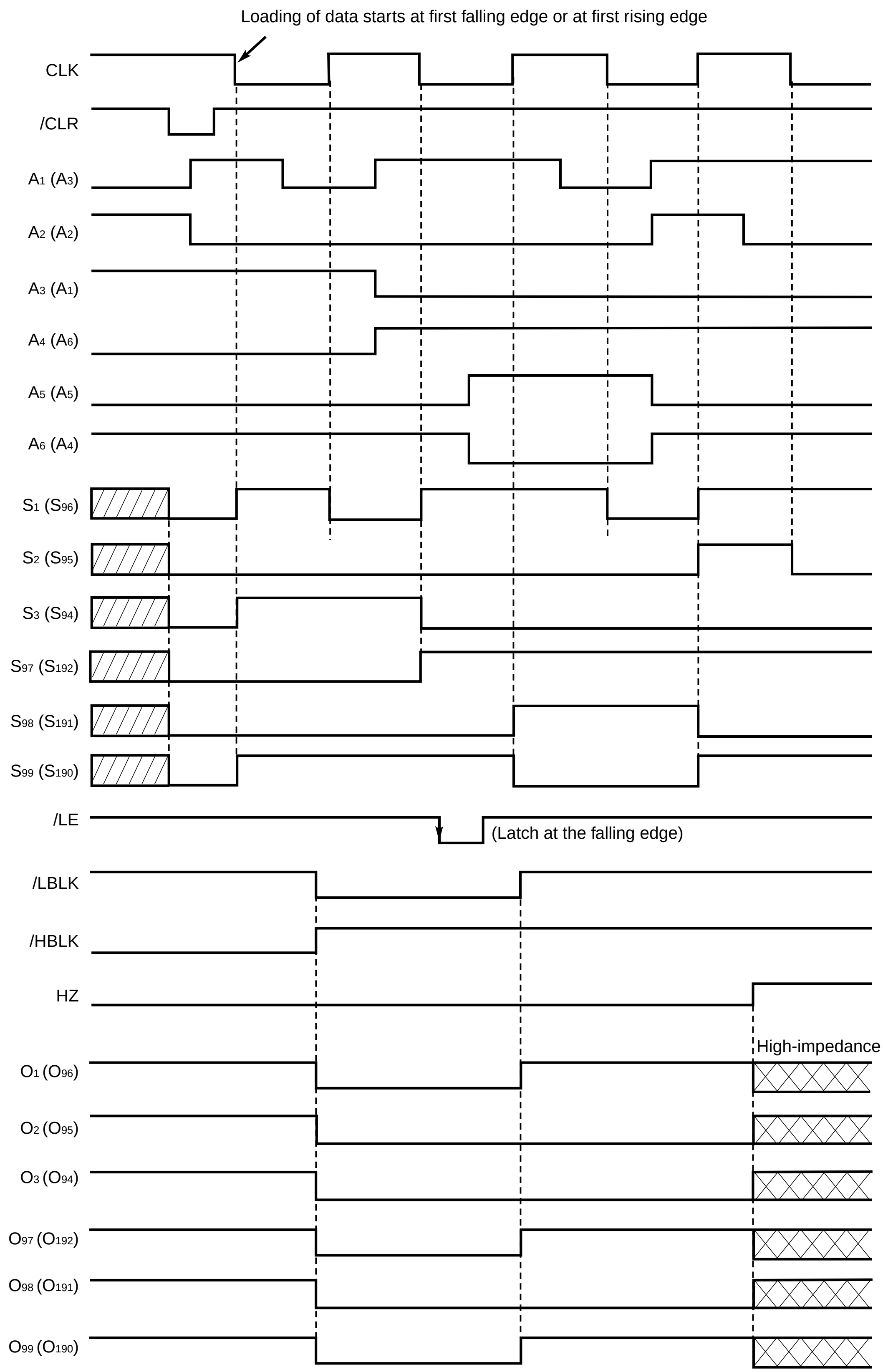
Remark Values in parentheses are when R,/L = L.

(7) IBS1 = H, IBS2 = H: 6-bit (3-bit + 3-bit) input, SDS = L: single edge



Remark Values in parentheses are when R,/L = L.

(8) IBS1 = H, IBS2 = H: 6-bit (3-bit + 3-bit) input, SDS = H: double edge



Remark Values in parentheses are when R,/L = L.

7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = V_{SS3} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic and temperature detection supply voltage	V_{DD1}, V_{DD3}	–0.5 to +6.0	V
Driver supply voltage	V_{DD2}	–0.5 to +80	V
Logic input voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Temperature detection input voltage	V_{I3}	–0.5 to V_{DD3} + 0.5	V
Operating junction temperature	T_j	+125	°C
Storage temperature	T_{stg}	–65 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –40 to +85°C, V_{SS1} = V_{SS2} = V_{SS3} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD1}	4.75	5.0	5.25	V
Driver supply voltage	V_{DD2}	15		70	V
Temperature detection supply voltage	V_{DD3}	4.5	5.0	5.5	V
Logic high level input voltage	V_{IH11}	2.7		V_{DD1}	V
Logic low level input voltage	V_{IL11}	0		0.6	V
IBS and R,/L high level input voltage	V_{IH12}	0.7 V_{DD1}		V_{DD1}	V
IBS and R,/L low level input voltage	V_{IL12}	0		0.2 V_{DD1}	V
Driver output current	I_{OH2}			–24	mA
	I_{OL2}			+13	mA

★ **Electrical Characteristics (T_A = 25°C, V_{DD1} = V_{DD3} = 5.0 V, V_{DD2} = 70 V, V_{SS1} = V_{SS2} = V_{SS3} = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High level output voltage	V_{OH21}	I_{OH2} = –0.52 mA	69			V
	V_{OH22}	I_{OH2} = –5.2 mA	65			V
Low level output voltage	V_{OL21}	I_{OL2} = 1.6 mA			1.0	V
	V_{OL22}	I_{OL2} = 13 mA			10	V
Input leakage current	I_I	V_{I1} = V_{DD1} or V_{SS1}, V_{I3} = V_{DD3} or V_{SS3}			±1.0	μA
Logic high level input voltage	V_{IH11}	V_{DD1} = 4.75 to 5.25 V	2.7		V_{DD1}	V
Logic low level input voltage	V_{IL11}	V_{DD1} = 4.75 to 5.25 V	0		0.6	V
IBS and R,/L high level input voltage	V_{IH12}		0.7 V_{DD1}		V_{DD1}	V
IBS and R,/L low level input voltage	V_{IL12}		0		0.2 V_{DD1}	V
Detection temperature	T_{DET}		110		135	°C
Detection temperature hysteresis width	T_{hys}		10		15	°C
Temperature detection output (N-ch) characteristic	R_{DET}	V_{SS3} to DET voltage, I_O = 1 mA			0.1 V_{DD3}	V
Static current dissipation	I_{DD11}	Logic, T_A = –40 to +85°C			1000	μA
		Logic, T_A = 25°C			600	μA
	I_{DD12}	Logic, T_A = –40 to +85°C			10 **Note**	mA
		Logic, T_A = 25°C			10 **Note**	mA
	I_{DD3}	Temperature detection, T_A = –40 to +85°C			1000	μA
		Temperature detection, T_A = 25°C			800	μA
	I_{DD2}	Driver, T_A = –40 to +85°C			1000	μA
		Driver, T_A = 25°C			100	μA

Note When input all input high level (V_{IH} = 2.7 V to V_{DD1}, but both the R,/L and IBS pins are fixed to V_I = V_{SS1} or V_{DD1})

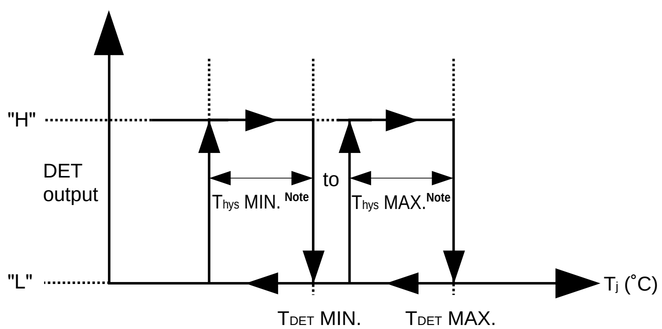
Switching Characteristics (T_A = 25°C, V_{DD1} = V_{DD3} = 5.0 V, V_{DD2} = 70 V, V_{SS1} = V_{SS2} = V_{SS3} = 0 V, Logic C_L = 15 pF, Driver C_L = 50 pF, t_r = t_f = 3.0 ns)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Propagation delay time	t_{PHL2}	/LE ↓ → O_1 to O_{192}			220	ns
	t_{PLH2}				220	ns
	t_{PHL3}	/HBLK → O_1 to O_{192}			205	ns
	t_{PLH3}				205	ns
	t_{PHL4}	/LBLK → O_1 to O_{192}			200	ns
	t_{PLH4}				200	ns
	t_{PHZ}	HZ → O_1 to O_{192},			340	ns
	t_{PZH}	R_L = 10 kΩ			220	ns
	t_{PLZ}				340	ns
	t_{PZL}				220	ns
Rise time	t_{TLH}	O_1 to O_{192}			220	ns
	t_{TLZ}	O_1 to O_{192},			3	μs
	t_{TZH}	R_L = 10 kΩ			220	ns
Fall time	t_{THL}	O_1 to O_{192}			350	ns
	t_{THZ}	O_1 to O_{192},			3	μs
	t_{TZL}	R_L = 10 kΩ			350	ns
Maximum clock frequency	$f_{MAX.}$	Loading of data, duty = 50%	60			MHz
Input capacitance	C_I				15	pF

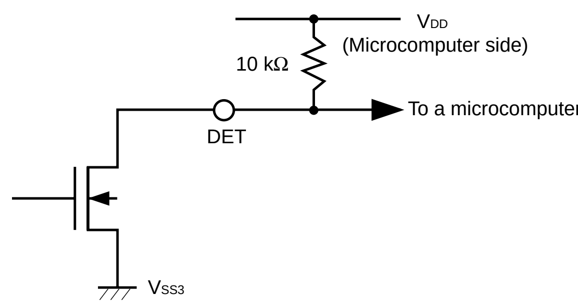
Timing Requirement (T_A = 25°C, V_{DD1} = 4.75 to 5.25 V, V_{SS1} = V_{SS2} = V_{SS3} = 0 V, t_r = t_f = 3.0 ns)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW_{CLK}		8			ns
Latch enable pulse width	$PW_{/LE}$		8			ns
Blank pulse width	$PW_{/BLK}$	/HBLK, /LBLK	600			ns
HZ pulse width	PW_{HZ}	R_L = 10 kΩ	3.3			μs
/CLR pulse width	$PW_{/CLR}$		12			ns
/CLR timing	$t_{/CLR}$		6			ns
Data setup time	t_{SETUP}		3			ns
Data hold time	t_{HOLD}		3			ns
Latch enable Time	$t_{/LE11}$, $t_{/LE21}$		8			ns
	$t_{/LE12}$, $t_{/LE22}$		8			ns

★ **Detection Temperature Hysteresis Width and Detection Output**

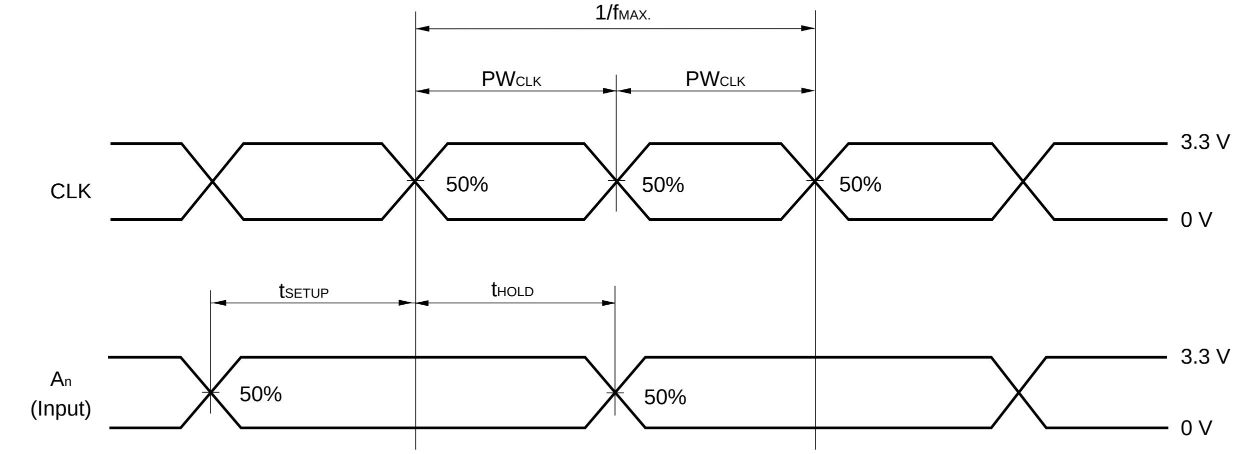


<Detection output circuit>

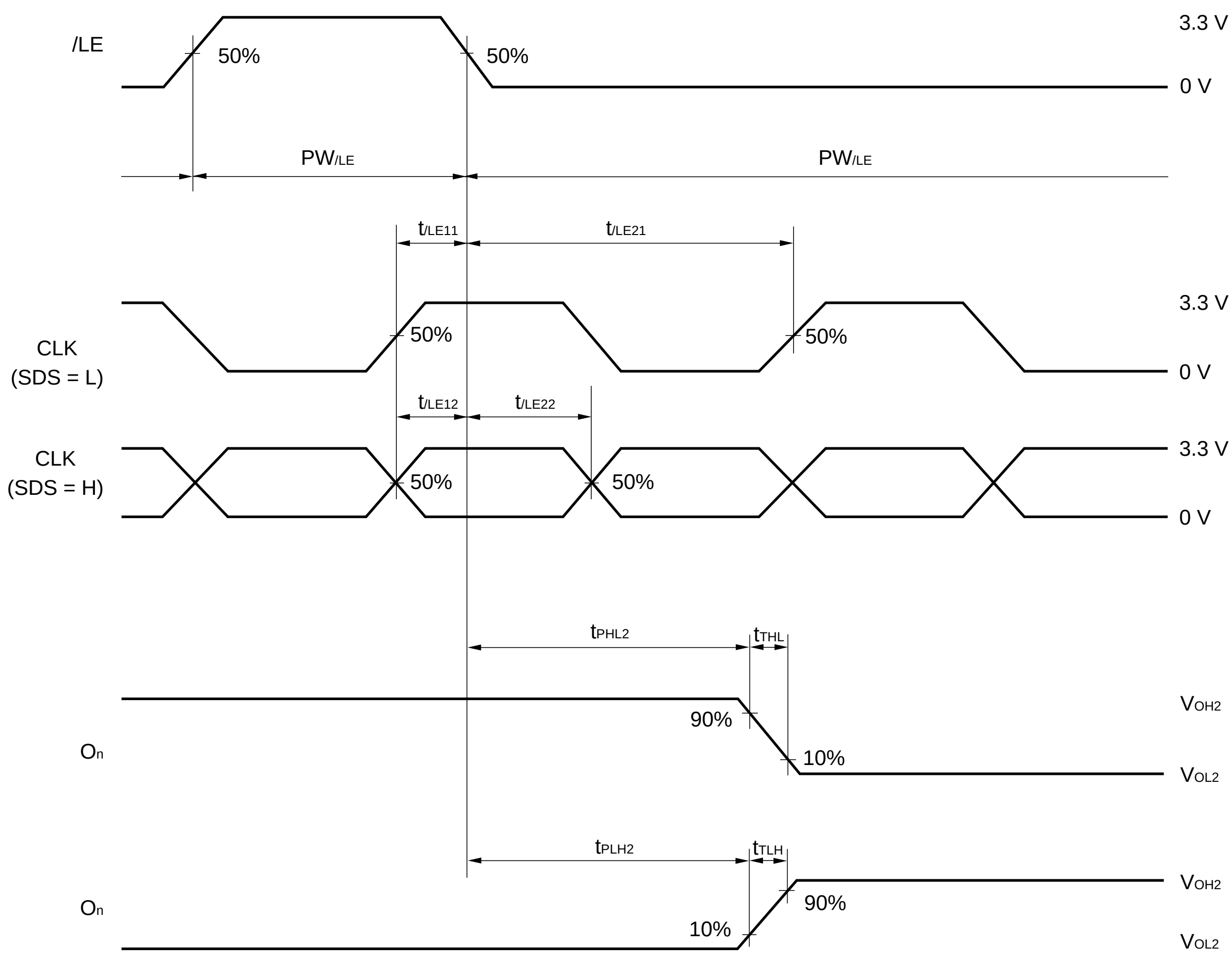


Note Change of T_{hys} linked with T_{DET}'s.

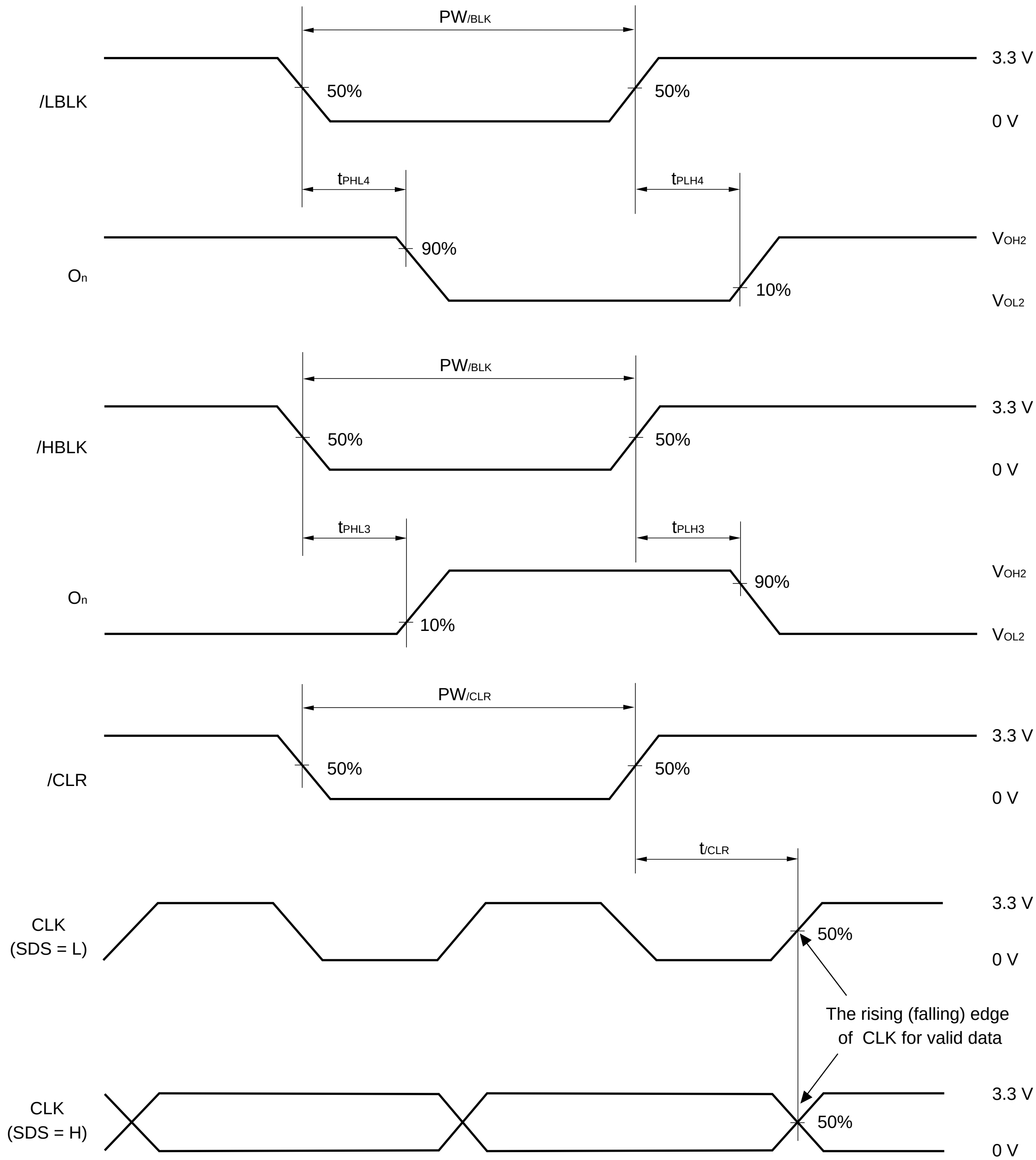
Switching Characteristics Waveform (1/3)



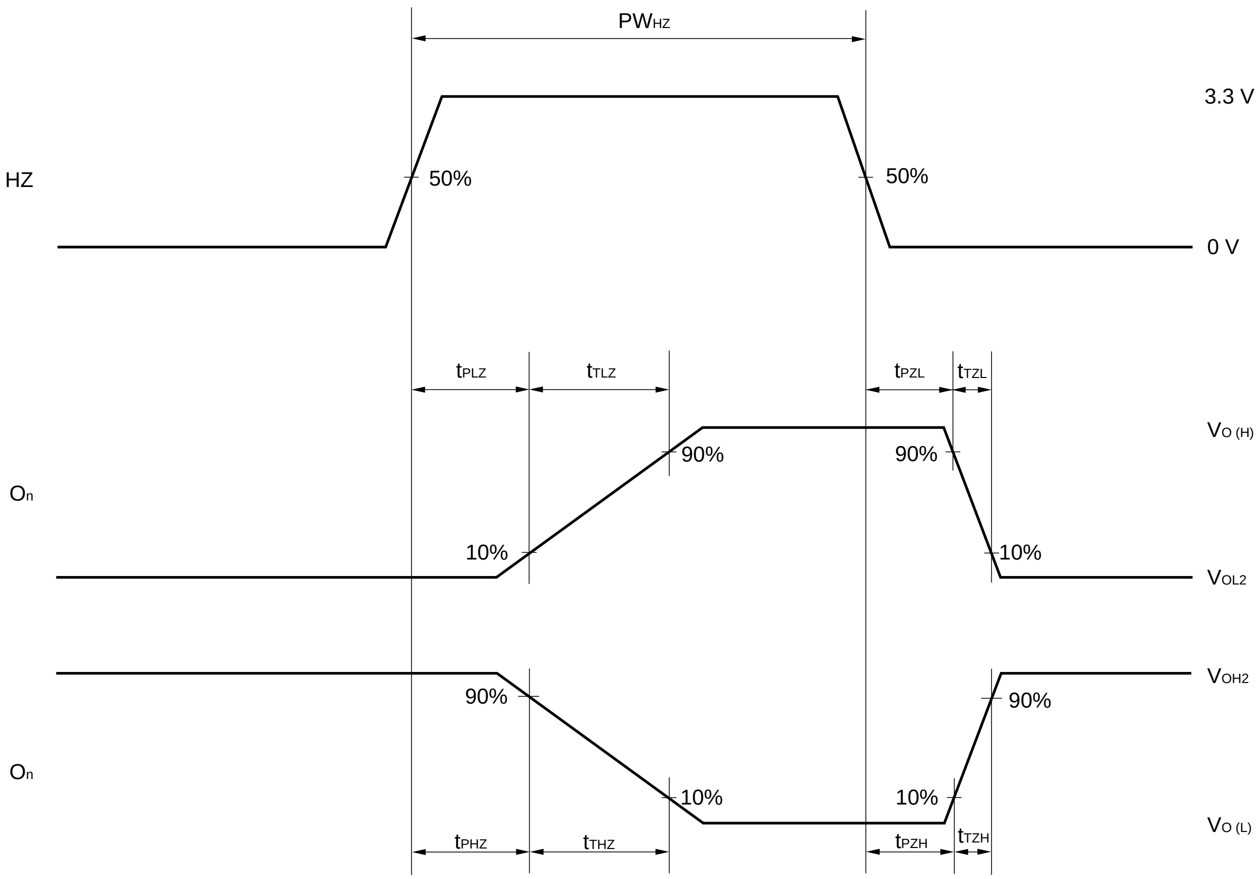
Remark The falling timing of CLK is at SDS = H (double edge).



Switching Characteristics Waveform (2/3)



Switching Characteristics Waveform (3/3)



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)