2SJ363

Silicon P-Channel MOS FET

HITACHI

Application

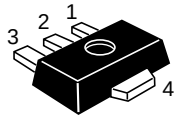
Low frequency power switching

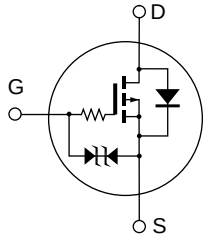
Features

- Low on-resistance
- Low drive current
- 4 V gate drive device can be driven from 5 V source

Outline

UPAK





1. Gate
2. Drain
3. Source
4. Drain

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Absolute Maximum Ratings (Ta = 25°C)

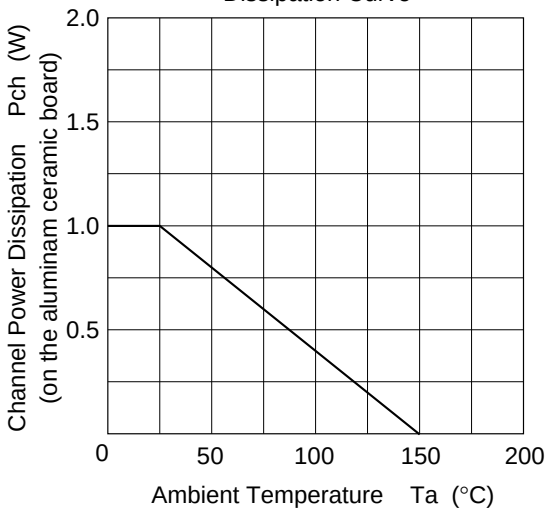
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–2	A
Drain peak current	$I_{D(pulse)}$*[1]	–4	A
Body to drain diode reverse drain current	I_{DR}	–2	A
Channel dissipation	Pch*[2]	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 100 µs, duty cycle ≤ 10%
2. Value on the alumina ceramic board (12.5×20×0.7 mm)
3. Marking is “PY”.

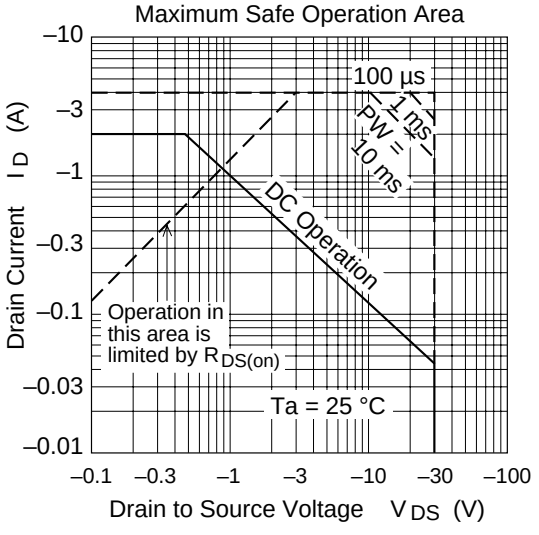
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±10 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±5	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1	µA	V_{DS} = –24 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	I_D = –100 µA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.6	0.75	Ω	I_D = –1 A, V_{GS} = –4 V*[1]
		—	0.35	0.45	Ω	I_D = –1 A, V_{GS} = –10 V*[1]
Forward transfer admittance	$\|y_{fs}\|$	1.4	2.0	—	S	I_D = –1 A, V_{DS} = –10 V*[1]
Input capacitance	Ciss	—	2.1	—	pF	V_{DS} = –10 V, V_{GS} = 0,
Output capacitance	Coss	—	100	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	0.25	—	pF	
Turn-on delay time	$t_{d(on)}$	—	1.65	—	µs	I_D = –1 A, V_{GS} = –10 V,
Rise time	t_r	—	8	—	µs	R_L = 30 Ω
Turn-off delay time	$t_{d(off)}$	—	25.9	—	µs	
Fall time	t_f	—	14.9	—	µs	

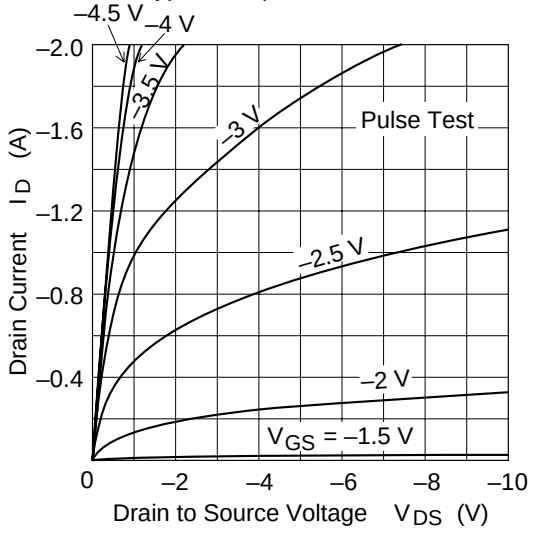
Maximum Channel Power Dissipation Curve



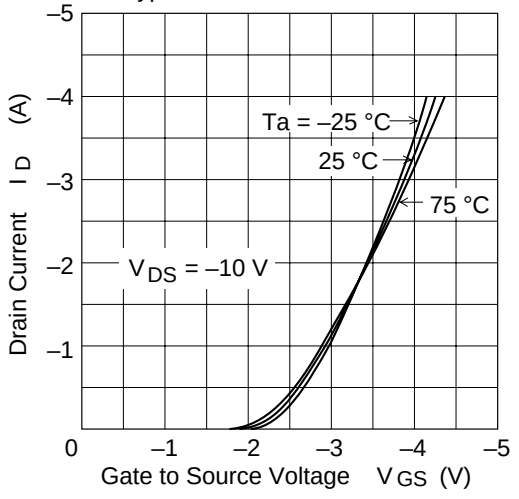
Maximum Safe Operation Area



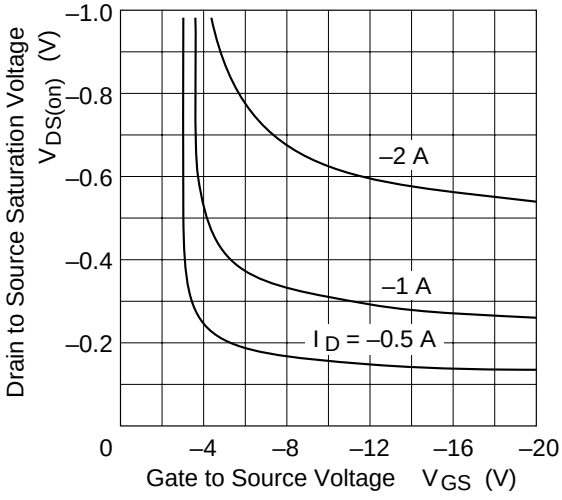
Typical Output Characteristics



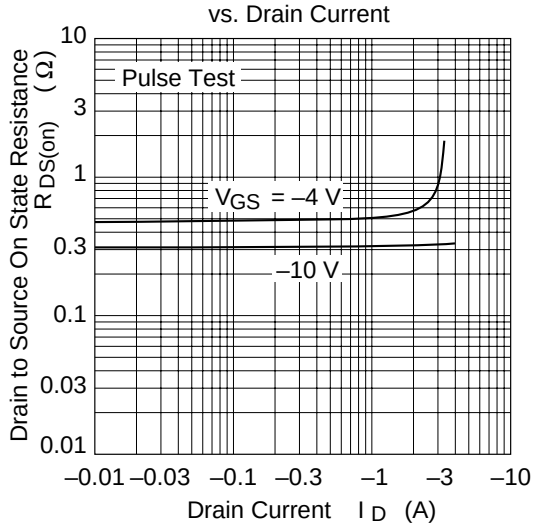
Typical Transfer Characteristics



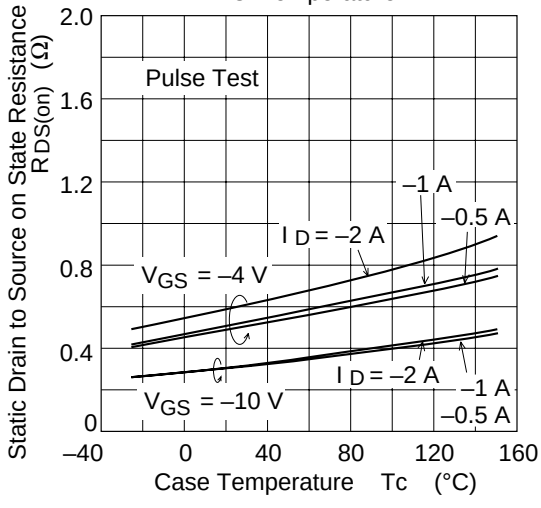
Drain to Source Saturation Voltage vs. Gate to Source Voltage



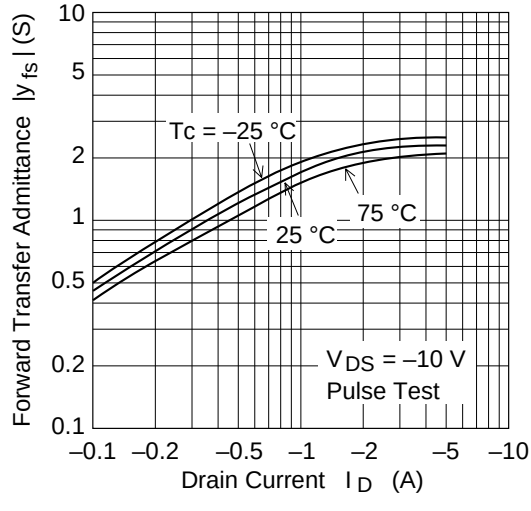
Static Drain to Source on State Resistance vs. Drain Current



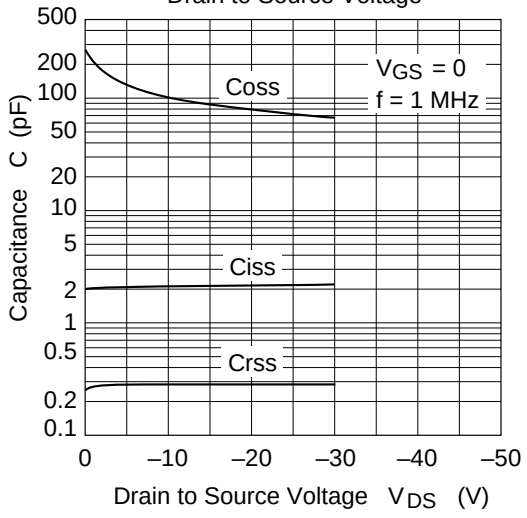
Static Drain to Source on State Resistance vs. Temperature



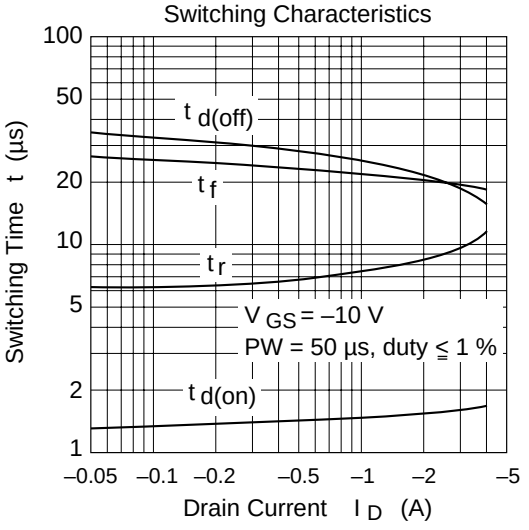
Forward Transfer Admittance vs. Drain Current



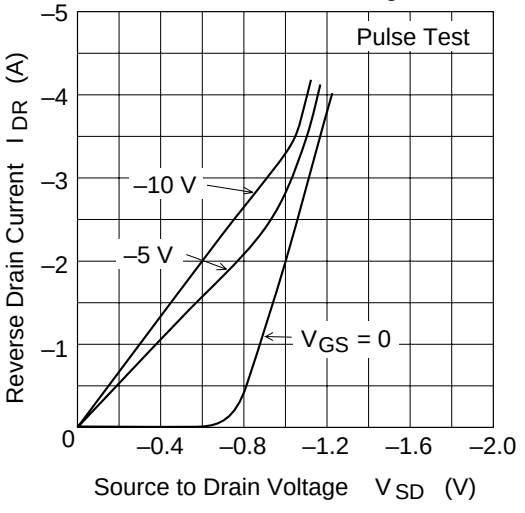
Typical Capacitance vs.
Drain to Source Voltage



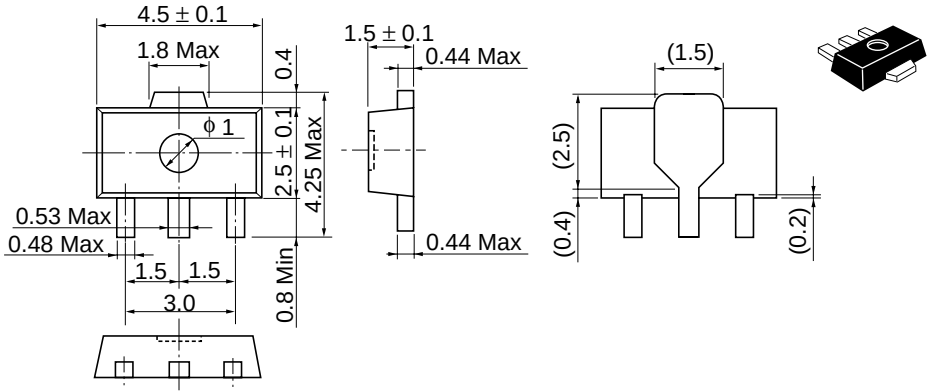
Switching Characteristics



Reverse Drain Current vs.
Source to Drain Voltage



Unit: mm



Hitachi Code	UPAK
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.050 g

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