MN662747RPH

Signal Processing LSI for CD Players

■ Overview

The MN662747RPH is a CD signal processing LSI that, on a single chip, combines optics servos for the CD player (focus, tracking, and traverse servos), digital signal processing (EFM demodulation and error correction), digital servo processing for the spindle motor, digital filter, and D/A converter, so thus covers all signal processing functions from the head's RF amplifier onward.

■ Features

(Optics servo)

- Focus, tracking, and traverse servos
- Automatic adjustment functions for FO/TR gain, FO/TR offset, and FO/TR balance
- Built-in D/A converter for drive voltage output
- Built-in dropout countermeasures
- Anti-shock functions
- Built-in track cross counter
- Traverse speed detection function

(Digital Signal Processing)

- Built-in DSL and PLL
- Frame synchronization detection, holding, and insertion
- Subcode data processing
  - Subcode Q data CRC check
  - Built-in subcode Q data register
- CIRC error detection and correction
  - C1 decoder: duplex error correction
  - C2 decoder: triplex error correction
  - Built-in 16-K bits of RAM for use in de-interleaving
- Audio data interpolation
  - Averaging or retention of previous values
  - Digital attenuation (–12 dB)
- Audio data peak level detection function
- Digital audio interface (EIAJ format)
- Audio data serial interface for input and output

(Spindle Motor Servo)

- CLV digital servo
- Switchable servo gain

(Audio circuits)

- Digital filter using 8-fold oversampling
- Built-in D/A converter (1-bit D/A converter)
- Built-in differential operational amplifier (secondary low pass filter)

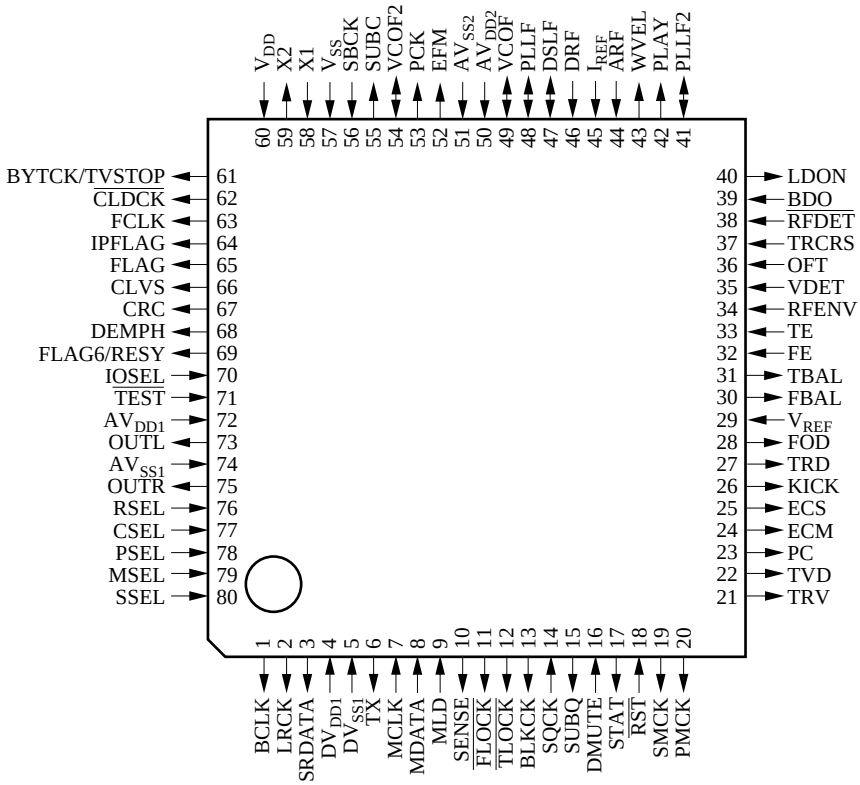
(Other)

- Built-in playback pitch control function (normal speed only) (±13%)
- Support for quadruple-speed playback (digital servo and signal processing block only)
- Built-in support for jitter-free disc rotation synchronization playback
- Oscillator shutdown mode
- Power management mode
- Operating voltage 4.5 to 5.5 V

■ Applications

- CD players

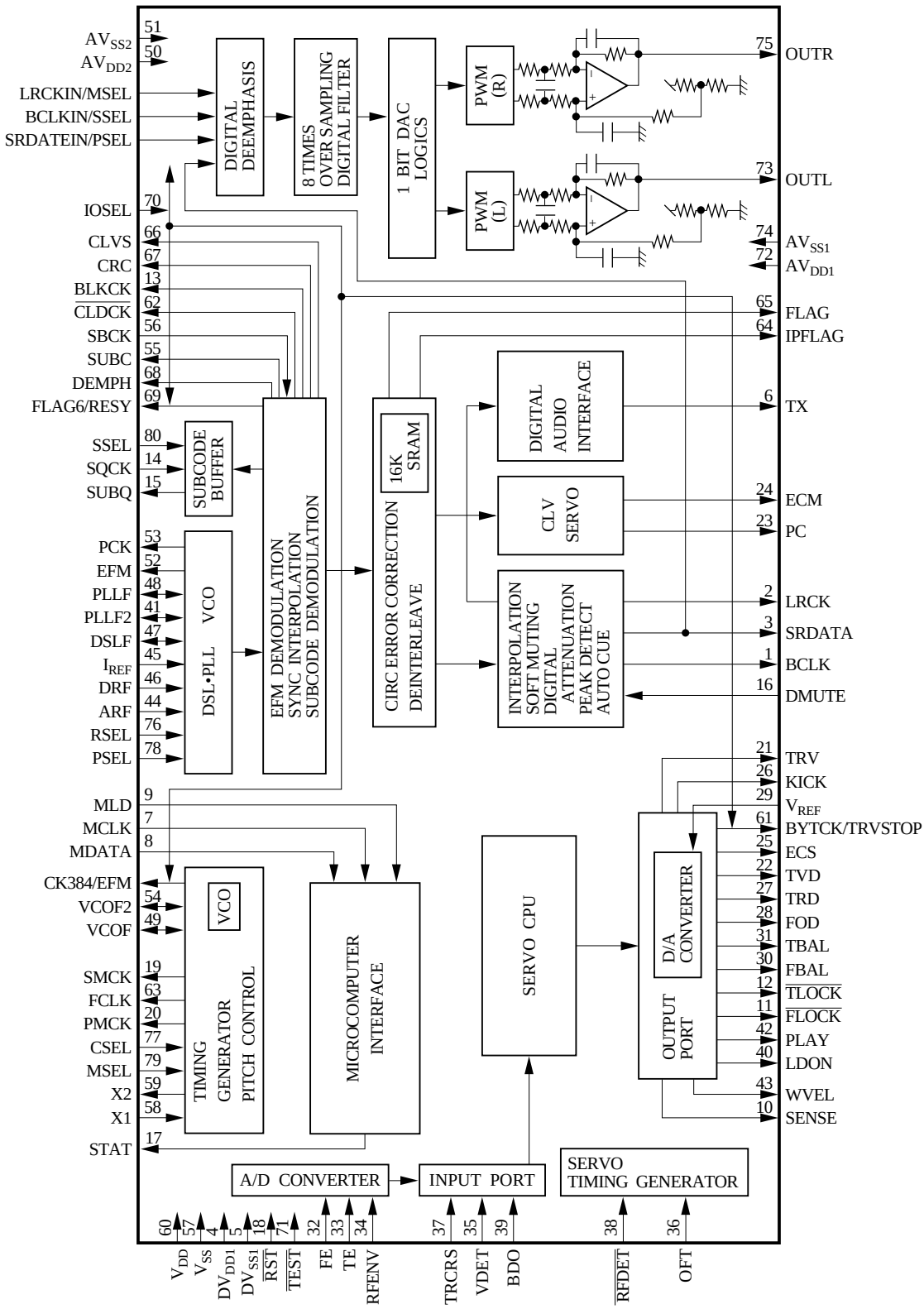
■ Pin Assignment



(TOP VIEW)

QFS080-P-1414

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	I/O	Function Description
1	BCLK	O	SRDATA bit clock output.
2	LRCK	O	Left/right channel discrimination signal output.
3	SRDATA	O	Serial data output.
4	DV_{DD1}	I	Power supply for digital circuits.
5	DV_{SS1}	I	Ground for digital circuits.
6	TX	O	Digital audio interface output signal.
7	MCLK	I	Microcomputer command clock input. (Data is latched at rising edge.)
8	MDATA	I	Microcomputer command data input.
9	MLD	I	Microcomputer command load signal input. "L" level: load.
10	SENSE	O	Sense signal output. (OFT, FESL, NACEND, NAJEND, SFG, and NWTEND)
11	$\overline{\text{FLOCK}}$ or DIRBK	O	During default operation, focus servo convergence signal. "L" level: convergence. During command execution, direction detection output for external track counter.
12	$\overline{\text{TLOCK}}$ or OTCFR	O	During default operation, tracking servo convergence signal. "L" level: convergence. During command execution, traverse speed control output.
13	BLKCK	O	Subcode block clock signal (f_{BLKCK}=75 Hz)
14	SQCK	I	External clock input for subcode Q register
15	SUBQ	O	Subcode Q data output
16	DMUTE	I	Muting input. (Effective only for an output bit rate of 64 f_s) "H" level: muting.
17	STAT	O	Status signal. (CRC, CLVS, TTSTOP, JCLVS, SQOK, FLAG6, SENSE, $\overline{\text{FLOCK}}$, $\overline{\text{TLOCK}}$, rpm data, and FCLV)
18	$\overline{\text{RST}}$	I	Reset input. "L" level: reset.
19	SMCK	O	If MSEL is "H" level, 8.4672 MHz clock signal output. If MSEL is "L" level, 4.2336 MHz clock signal output
20	PMCK	O	88.2 kHz clock signal output.
21	TRV	O	Traverse forced feed output. (tristate)
22	TVD	O	Traverse drive output.
23	PC	O	Spindle motor ON signal. "L" level: ON (default).
24	ECM	O	Spindle motor drive signal (forced mode output). (tristate)
25	ECS	O	Spindle motor drive signal (servo error signal output). (tristate)
26	KICK	O	Kick pulse output. (tristate)
27	TRD	O	Tracking drive output.
28	FOD	O	Focus drive output.
29	V_{REF}	I	Reference voltage for DA output (TVD, ECS, TRD, FOD, FBAL, and TBAL).
30	FBAL	O	Focus balance adjustment output.
31	TBAL	O	Tracking balance adjustment output.
32	FE	I	Focus error signal input. (analog input)

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
33	TE	I	Tracking error signal input. (analog input)
34	RFENV	I	RF envelope signal input. (analog input)
35	VDET	I	Vibration detection signal input. "H" level: vibration detected.
36	OFT	I	Offtrack signal input. "H" level: offtrack.
37	TRCRS	I	Track cross signal input. (analog input)
38	$\overline{\text{RFDET}}$	I	RF detection signal input. "L" level: detected.
39	BDO	I	Dropout signal input. "H" level: dropout.
40	LDON	O	Laser ON signal output. "H" level: ON.
41	PLLF2	I/O	PLL loop filter characteristic selection pin.
42	PLAY	O	Play signal output. "H" level: play.
43	WVEL	O	Double-speed status signal output. "H" level: double-speed.
44	ARF	I	RF signal input.
45	I_{REF}	I	Reference current input pin.
46	DRF	I	DSL bias pin.
47	DSLF	I/O	DSL loop filter pin.
48	PLLF	I/O	PLL loop filter pin.
49	VCOF	I/O	VCO loop filter pin.
50	AV_{DD2}	I	Power supply for analog circuits (DSL, PLL, D/A converter output, and A/D converter).
51	AV_{SS2}	I	Ground for analog circuits (DSL, PLL, D/A converter output, and A/D converter).
52	EFM or CK384	O	EFM signal output. EFM output when IOSEL is "H" level. •Crystal oscillator 16.9344-MHz clock output when I •OSEL is "L" level. •384 f_s output from signal processing block. (During variable-pitch operation, this is the VCO clock.) Commands permit switching among the above three outputs.
53	PCK	O or DSLB	PLL derived clock or DSL balance output. f_{PCK} =4.3218 MHz.
54	VCOF2	I/O	VCO loop filter pin.
55	SUBC	O	Subcode serial output.
56	SBCK	I	Serial clock input for subcode serial output.
57	V_{SS}	I	Ground for oscillator circuit.
58	X1	I	Crystal oscillator circuit input/output pins. f=16.9344 MHz, 33.8688 MHz.
59	X2	O	Crystal oscillator circuit output/output pins. f=16.9344 MHz, 33.8688 MHz.
60	V_{DD}	I	Oscillator circuit power supply.
61	BYTCK or TRVSTOP	O	When IOSEL is "H" level, byte clock signal output. When IOSEL is "L" level, traverse stop signal output. "H" level: stop mode.
62	$\overline{\text{CLDCK}}$	O	Subcode frame clock signal output pin. (f_{CLDCK}=7.35 kHz)
63	FCLK	O	Crystal frame clock signal output. (f_{FCLK}=7.35 kHz)
64	IPFLAG	O	Interpolation flag signal output. "H" level: interpolation.
65	FLAG	O	Flag signal output.

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
66	CLVS	O	Spindle servo phase synchronization signal output. "H" level: CLV. "L" level: rough servo.
67	CRC or TCK	O	During default operation, subcode CRC check result output. "H" level: OK. "L" level: no good. During command execution, pulse output for external track counter.
68	DEMPH	O	De-emphasis detection signal output. "H" level: ON.
69	FLAG6 or RESY	O	When IOSEL is "L" level, FLAG6 output, signal for resetting address of RAM for error correction de-interleave. "L" level: address reset. When IOSEL is "H" level, RESY output, frame resynchronization signal. "H" level: synchronized. "L" level: out of sync.
70	$\overline{\text{IOSEL}}$	I	Mode selection pin
71	TEST	I	Test pin. Keep this at "H" level.
72	AV_{DD1}	I	Power supply for analog circuits. (common use for left and right channel audio outputs.)
73	OUTL	O	Left channel audio output.
74	AV_{SS1}	I	Ground for analog circuits. (common use for left and right channel audio outputs.)
75	OUTR	O	Right channel audio output.
76	RSEL	I	RF signal polarity selection pin. "H" level: bright level is "H." "L" level: bright level is "L."
77	CSEL	I	Crystal oscillator frequency specification pin. "H" level: 33.8688 MHz. "L" level: 16.9344 MHz
78	PSEL	I	When IOSEL is "H" level, test pin. Keep this at "L" level. When IOSEL is "L" level, SRDATA input.
79	MSEL	I	When IOSEL is "H" level, frequency selection pin for SMCK pin output. "H" level: SMCK=8.4672 MHz When IOSEL is "L" level, LRCK input. "H" level: left channel data. "L" level: right channel data. SMCK output fixed at 4.2336 MHz.
80	SSEL	I	When IOSEL is "H" level, SUBQ pin output mode selection pin. "H" level: buffered subcode Q mode. "L" level: CLDCK synchronization mode. When IOSEL is "L" level, BCKL input. Buffered subcode Q mode.

■ Package Dimensions (Unit: mm)

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