RF2945

433/868/915MHZ FSK/ASK/OOK TRANSCEIVER

Typical Applications

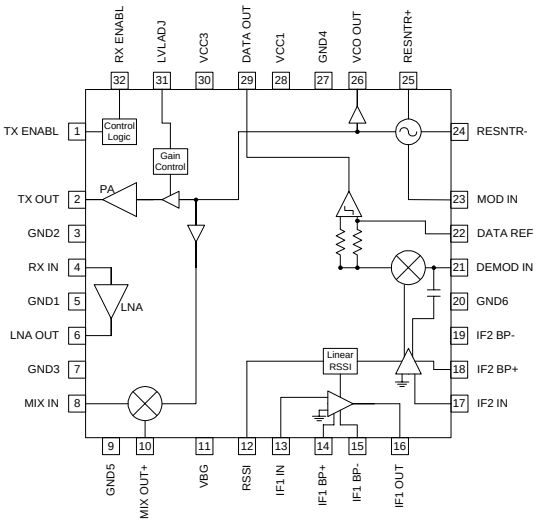
- Wireless Meter Reading
- Keyless Entry Systems
- 433, 868 and 915MHz ISM Band Systems
- Wireless Data Transceiver
- Wireless Security Systems
- Battery-Powered Portable Devices

Product Description

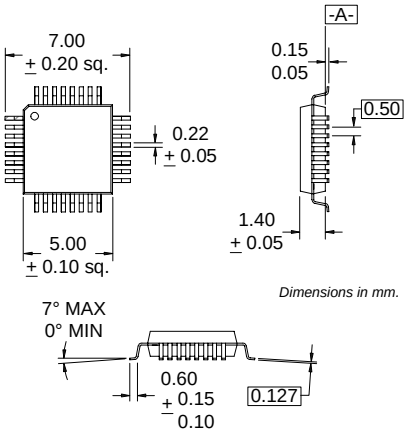
The RF2945 is a monolithic integrated circuit intended for use as a low cost FM transceiver. The device is provided in 32-lead plastic LQFP packaging and is designed to be used with a PLL IC to provide a fully functional FM transceiver. The chip is intended for digital (ASK, FSK, OOK) applications in the North American 915MHz ISM band and European 433/868MHz ISM bands. The integrated VCO has a buffered output to feed the RF signal back to the PLL IC to form the frequency synthesizer. Internal decoding of the RX ENABL and TX ENABL lines allow for half duplex operation as well as turning on the VCO to give the synthesizer time to settle and complete power downmode. The DATA REF line allows the use of an external capacitor to control the DC level at the adaptive Data Slicer input for setting the bit decision threshold.

Optimum Technology Matching® Applied

- [x] Si BJT
- [ ] GaAs HBT
- [ ] GaAs MESFET
- [ ] Si Bi-CMOS
- [ ] SiGe HBT
- [ ] Si CMOS



Functional Block Diagram



Package Style: LQFP-32_5x5

Features

- Fully Monolithic Integrated Transceiver
- 2.4V to 5.0V Supply Voltage
- Narrowband and Wideband FSK
- 300MHz to 1000MHz Frequency Range
- 10dB Cascaded Noise Figure
- 10mW Output Power With Power Control

Ordering Information

RF2945	433/868/915MHz FSK/ASK/OOK Transceiver
RF2945 PCBA-L	Fully Assembled Evaluation Board (433MHZ)
RF2945 PCBA-M	Fully Assembled Evaluation Board (868MHZ)
RF2945 PCBA-H	Fully Assembled Evaluation Board (915MHz)

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Absolute Maximum Ratings

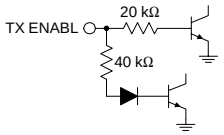
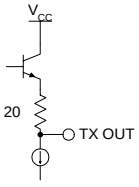
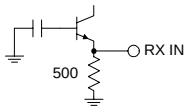
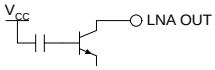
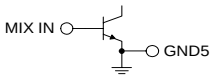
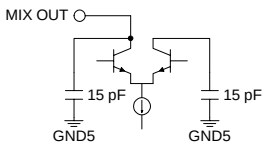
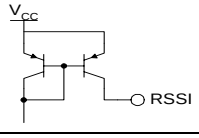
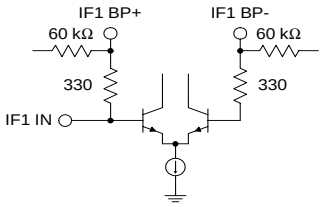
Parameter	Ratings	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Control Voltages	-0.5 to +5.0	V_{DC}
Input RF Level	+10	dBm
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

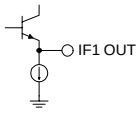
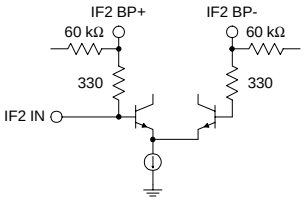
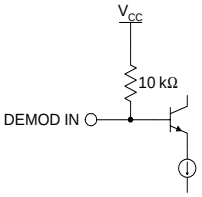
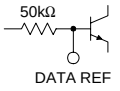
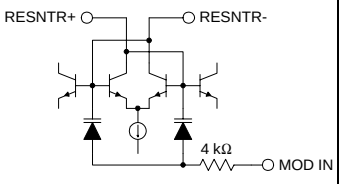
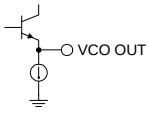
Caution! ESD sensitive device.

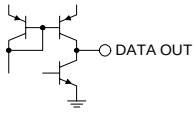
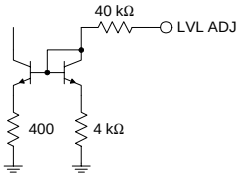
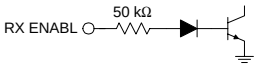
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, Freq=915MHz
RF Frequency Range		300 to 1000		MHz	
VCO and PLL Section					
VCO Frequency Range		300 to 1000		MHz	
VCO OUT Impedance		50		Ω	
VCO OUT Level		-20		dBm	Freq=915MHz
VCO/PLL Phase Noise		-72		dBc/Hz	10kHz offset, 5kHz loop BW
		-98		dBc/Hz	100kHz offset, 5kHz loop BW
Transmit Section					
Max Modulation Frequency	2			MHz	
Min Modulation Frequency	Set by loop filter bandwidth				
Maximum Power Level	+7	+8.5		dBm	Freq=433MHz
	1	+3	5	dBm	Freq=915MHz
Power Control Range	12			dB	
Power Control Sensitivity		10		dB/V	
Max FM Deviation	200			kHz	Instantaneous frequency deviation is inversely proportional with the modulation voltage. Dependent on external circuitry.
Antenna Port Impedance		50		Ω	TX ENABL="1", RX ENABL="0"
Antenna Port VSWR			1.5:1		TX Mode
Modulation Input Impedance	4			kΩ	
Harmonics		-38		dBc	Freq=915MHz, with eval board filter
Spurious				dBc	Compliant to Part 15.249 and I-ETS 300 220
Overall Receive Section					
Frequency Range		300 to 1000		MHz	
Cascaded Voltage Gain		35		dB	Freq=433MHz
		23		dB	Freq=915MHz
Cascaded Noise Figure		10		dB	
Cascaded Input IP_3		-31		dBm	Freq=433MHz
		-26		dBm	Freq=915MHz
RX Sensitivity	-91.5	-96		dBm	IF BW=400kHz, Freq=915MHz, S/N=8dB
LO Leakage		-55		dBm	Freq=915MHz
RSSI DC Output Range		0.5 to 2.5		V	R_{LOAD}=51kΩ
RSSI Sensitivity		22.5		mV/dB	
RSSI Dynamic Range	70	80		dB	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
LNA					
Voltage Gain		23		dB	433MHz
		16		dB	915MHz
Noise Figure		4.8		dB	433MHz
		5.5		dB	915MHz
Input IP_3		-27		dBm	433MHz
		-20		dBm	915MHz
Input P_{1dB}		-37		dBm	433MHz
		-30		dBm	915MHz
Antenna Port Impedance		50		Ω	RX ENABL="1", TX ENABL="0"
Antenna Port VSWR			1.5:1		RX Mode
Output Impedance		Open Collector		Ω	433MHz and 915MHz
Mixer					Single-ended configuration
Conversion Voltage Gain		8		dB	433MHz
		7		dB	915MHz
Noise Figure (SSB)		10		dB	433MHz
		17		dB	915MHz
Input IP_3		-21		dBm	433MHz
		-17		dBm	915MHz
Input P_{1dB}		-31		dBm	433MHz
		-28		dBm	915MHz
First IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		34		dB	IF=10.7MHz, Z_L=330Ω
Noise Figure		13		dB	
IF1 Input Impedance		330		Ω	
IF1 Output Impedance		330		Ω	
Second IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		60		dB	IF=10.7MHz
IF2 Input Impedance		330		Ω	
IF2 Output Impedance		1		kΩ	At IF2 OUT pin
Demod Input Impedance		10		kΩ	
Data Output Bandwidth	1.4			MHz	3dB Bandwidth, Z_{LOAD}=1MΩ || 3pF
Data Output Level	0.3		V_{CC}-0.3	V	Z_{LOAD}=1MΩ || 3pF. Output voltage is proportional with the instantaneous frequency deviation.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Down Control					
Logical Controls “ON”	2.0			V	Voltage supplied to the input
Logical Controls “OFF”			1.0	V	Voltage supplied to the input
Control Input Impedance	25k			Ω	
Turn On Time			1	ms	Turn on/off times are dependent upon
Turn Off Time			1	ms	PLL loop parameters
RX to TX and TX to RX Time			100	µs	
Power Supply					
Voltage		3.6		V	Specifications
	2.7		5.0	V	Operating limits Temperature range -40°C to +85°C
	2.4			V	Operating limits Temperature range +10°C to +40°C
Current Consumption	17	22	27.4	mA	TX ENABL, LVLADJ=3.6V, RX ENABL=0V
	4.8	6.1	7.2	mA	TX ENABL=3.6V, LVLADJ, RX ENABL=0V
	4.4	6.1	6.8	mA	TX ENABL=0V, RX ENABL=3.6V
			1	µA	TX ENABL, LVLADJ, RX ENABL=0V
		3.6		mA	PLL Only Mode, TX ENABL, RX ENABL=3.6V, LVLADJ=0V

Pin	Function	Description	Interface Schematic
1	TX ENABL	Enables the transmitter circuits. TX ENABL>2.0V powers up all transmitter functions. TX ENABL<1.0V turns off all transmitter functions except the PLL functions.	
2	TX OUT	RF output pin for the transmitter electronics. TX OUT output impedance is a low impedance when the transmitter is enabled. TX OUT is a high impedance when the transmitter is disabled.	
3	GND2	Ground connection for the 40 dB IF limiting amplifier and Tx PA functions. Keep traces physically short and connect immediately to ground plane for best performance.	
4	RX IN	RF input pin for the receiver electronics. RX IN input impedance is a low impedance when the transmitter is enabled. RX IN is a high impedance when the receiver is disabled.	
5	GND1	Ground connection for RF receiver functions. Keep traces physically short and connect immediately to ground plane for best performance.	
6	LNA OUT	Output pin for the receiver RF low noise amplifier. This pin is an open collector output and requires an external pull up coil to provide bias and tune the LNA output. A capacitor in series with this output can be used to match the LNA to 50Ω impedance image filters.	
7	GND3	Same as pin 3.	
8	MIX IN	RF input to the RF Mixer. An LC matching network between LNA OUT and MIX IN can be used to connect the LNA output to the RF mixer input in applications where an image filter is not needed or desired.	
9	GND5	GND5 is the ground connection shared by the input stage of the transmit power amplifier and the receiver RF mixer.	
10	MIX OUT	IF output from the RF mixer. Interfaces directly to 10.7MHz ceramic IF filters as shown in the application schematic. A pull-up inductor and series matching capacitor should be used to present a 330Ω termination impedance to the ceramic filter. Alternately, an IF tank can be used to tailor the IF frequency and bandwidth to meet the needs of a given application.	
11	VREF IF	DC voltage reference for the IF limiting amplifiers. A 10nF capacitor from this pin to ground is required.	.
12	RSSI	A DC voltage proportional to the received signal strength is output from this pin. The output voltage range is 0.5V to 2.3V and increases with increasing signal strength.	
13	IF1 IN	IF input to the 40dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input.	

Pin	Function	Description	Interface Schematic
14	IF1 BP+	DC feedback node for the 40dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 13.
15	IF1 BP-	Same as pin 14.	See pin 13.
16	IF1 OUT	IF output from the 40dB limiting amplifier. The IF1 OUT output presents a nominal 330 Ω output resistance and interfaces directly to 10.7MHz ceramic filters.	
17	IF2 IN	IF input to the 60dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input. The IF2 IN input presents a nominal 330 Ω input resistance and interfaces directly to 10.7MHz ceramic filters.	
18	IF2 BP+	DC feedback node for the 60dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 17.
19	IF2 BP-	Same as pin 18.	See pin 17.
20	GND6	Ground connection for 60dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
21	DEMOD IN	This pin is the input to the FM demodulator. This pin is NOT AC coupled. Therefore, a DC blocking capacitor is required on this pin to avoid shorting the demodulator input with the LC tank. A ceramic discriminator or DC blocked LC tank resonant at the IF should be connected to this pin.	
22	DATA REF	This pin is used for setting the adaptive Data Slicer DC reference level. A capacitor from this pin to ground can be used to set the reference level at the average DC level of the data bit stream.The DC level determines the bit decision threshold.	
23	MOD IN	FM analog or digital modulation can be imparted to the VCO through this pin. The VCO varies in accordance to the voltage level presented to this pin. To set the deviation to a desired level, a voltage divider referenced to Vcc is the recommended. This deviation is also dependent upon the overall capacitance of the external resonant circuit.	See pin 24.
24	RESNTR+	This port is used to supply DC voltage to the VCO as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 25 although a small imbalance can be used to tune in the proper frequency range.	
25	RESNTR-	See RESNTR+ description.	See pin 24.
26	VCO OUT	This pin is used is supply a buffered VCO output to go to the PLL chip. This pin has a DC bias and needs to be AC coupled.	
27	GND4	GND4 is the ground shared on chip by the VCO, prescaler, and PLL electronics.	

Pin	Function	Description	Interface Schematic
28	VCC1	This pin is used to supply DC bias to the LNA, Mixer, 1st IF Amp and Bandgap reference. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 68pF capacitor is recommended for 433MHz applications.	
29	DATA OUT	Demodulated data output from the demodulator. Output levels on this are TTL/CMOS compatible. The magnitude of the load impedance is intended to be 1MΩ or greater.	
30	VCC3	This pin is used to supply DC bias and collector current to the transmitter PA. It also supplies voltage to the 2nd IF Amplifier, Demod and data slicer. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 68pF capacitor is recommended for 433MHz applications.	
31	LVL ADJ	This pin is used to vary the transmitter output power. An output level adjustment range greater than 12dB is provided through analog voltage control of this pin. DC current of the transmitter power amp ia also reduced with output power. NOTE: This pin MUST be low when the transmitter is disabled.	
32	RX ENABL	Enable pin for the receiver circuits. RX ENABL>2.0V powers up all receiver functions. RX ENABL<1.0V turns off all receiver functions except the PLL functions and the RF mixer.	

Operation Mode	TX ENABL	RX ENABL	Function
Sleep Mode	Low	Low	Entire chip is powered down. Total current consumption is <1μA. *
Transmit Mode	High	Low	Transmitter, VCO are on.
Receive Mode	Low	High	Receiver, VCO are on. *
PLL Lock	High	High	VCO is on. This mode allows time for a synthesizer loop to lock without spending current on the transmitter or receiver.

* LVL ADJ pin must be low to disable transmitter.

RF2945 Theory of Operation and Application Information

The RF2945 is part of a family of low-power RF transceiver IC's that was developed for wireless data communication devices operating in the European 433MHz to 868MHz ISM band, and 915MHz U.S. ISM band. This IC has been implemented in a 15GHz silicon bipolar process technology that allows low-power transceiver operation in a variety of commercial wireless products.

In its basic form, the RF2945 can be implemented as a two-way half-duplex FSK transceiver with the addition of some crystals, filters, and passive components. The RF2945 is designed to interface with common PLL IC's to form a multi-channel radio. The receiver IF section is optimized to interface with low-cost 10.7MHz ceramic filters and has a 3dB bandwidth of 25MHz and can still be used (with lower gain) at higher frequencies with other types of filters. The PA output and LNA input are available on separate pins and are designed to be connected together through a DC blocking capacitor. In the transmit mode, the PA will have a 50Ω impedance and the LNA will have a high impedance. In the receive mode, the LNA will have a 50Ω impedance and the PA will have a high impedance. This eliminates the need for a TX/RX switch, and allows for a single RF filter to be used in transmit and receive modes. Separate access to the PA and LNA allows the RF2945 to interface with external components such as a high power PA, lower NF LNA, upconverters, and downconverters, for a variety of implementations.

FM/FSK SYSTEMS

The MOD IN pin drives an internal varactor for modulating the VCO. This pin can be driven with a voltage level needed to generate the desired deviation. This voltage can be carried on a DC bias to select desired slope (deviation/volt) for FM systems. Or, a resistor divider network referenced to VCC or ground can divide down logic level signals to the appropriate level for a desired deviation in FSK systems.

On the receiver demod, the DATA OUT pin is the output of an internal data slicer providing logic level outputs. The digital output is generated by a data slicer that compares the demodulator with a DC reference voltage recovered from the demodulator. The reference voltage is obtained by a filter capacitor on pin 22. An on-chip 1.6MHz RC filter is provided at the demodulator output to filter the undesirable 2xIF product. This type data slicer has the ability to track out minor frequency errors in the system, but requires a longer period of time for the preamble for optimum results. For best operation of the on-chip data slicer, FM deviation needs to be larger than $40kHz_{P-P}$

The data slicer itself is a transconductance amplifier, and the DATA OUT pin is capable of driving rail-to-rail output only into a very high impedance and a small capacitance. The amount of capacitance will determine the bandwidth of DATA OUT. In a 3pF load, the bandwidth is in excess of 500kHz. The rail-to-rail output of the data slicer is also limited by the frequency deviation and bandwidth of IF filters. With the 400kHz bandwidth filters on the evaluation boards, the rail-to-rail output is limited to less than 320kHz. Choosing the right IF bandwidth and deviation versus data rate (mod index) is important in evaluating the applicability of the RF2945 for a given data rate.

The primary consideration when directly modulating the VCO is the data rate versus PLL bandwidth. The PLL will track out the modulation to the extent of its bandwidth, which distorts the modulating data. Therefore, the lower frequency components of the modulating data should be five to 10 times the loop bandwidth to minimize the distortion. The lower frequency components are generated by long strings of 1's and 0's in data stream. By limiting the number of consecutive, same bits, lower frequency components can be set. In addition, the data stream should be balanced to minimize distortion. Using a coding pattern such as Manchester is highly recommended to optimize system performance.

The PLL loop bandwidth is important in several system parameters. For example, switching from transmit to receive requires the VCO to retune to another frequency. The switching speed is proportional to the loop bandwidth: the higher the loop bandwidth, the faster the switching times. Phase noise of the VCO is another factor. Phase noise outside the bandwidth is because of the VCO itself, rather than a crystal reference. The design trade-offs must be made here in selecting a PLL loop bandwidth with acceptable phase noise and switching characteristics, as well as minimal distortion of the modulation data.

ASK/OOK SYSTEMS

The transmitter of the RF2945 has an output power level adjust (LVL ADJ) that can be used to provide approximately 18dB of power control for amplitude modulation. The RSSI output of the receiver section can be used to recover the modulation. The RSSI output is from a current source, and needs to have a resis-

tor to convert to a voltage. A 51kΩ resistor load typically produces an output of 0.7V to 2.5V. A parallel capacitor is suggested to band limit the signal. For ASK applications, the 18dB range of the LVL ADJ does not produce enough voltage swing in the RSSI for reliable communications. The on/off keying (OOK) is suggested to provide reliable communications. To achieve this, the LVL ADJ and TX ENABL need to be controlled together (please note that LVL ADJ cannot be left high when TX ENABL is low). This will provide an on/off ratio of greater than 50dB. One of the unfortunate consequences of modulating in this manner is VCO pulling by the PA. This results in a spurious output outside the desired transmit band, as the PLL momentarily loses lock and reacquires. This may be avoided by pulse-shaping TX data to slow the change in the VCO load to a pace which the PLL can track with its given loop bandwidth. The loop bandwidth may also be increased to allow it to track faster changes brought about by load pulling.

For the ASK/OOK receiver demodulator, an external data slicer is required. The RSSI output is used to provide both the filter data and a very low pass filter (relative to the data rate) DC reference to the data slicer. Because the very low pass filter has a slow time constant, a longer preamble may be required to allow for the DC reference to acquire a stable state. Here, as in the case of the FSK transmitter, the data pattern also affects the DC reference and the reliability of the receive data. Again, a coding scheme such as Manchester should be used to improve data integrity.

APPLICATION AND LAYOUT CONSIDERATIONS

Both the RX IN and the TX OUT have a DC bias on them. Therefore, a DC blocking cap is required. If the RF filter has DC blocking characteristics (such as a ceramic dielectric filter), then only one DC blocking cap would be needed to separate the DC of the RX and TX. These are RF signals and care should be taken to run the signal keeping them physically short. Because of the 50Ω/high impedance nature of these two signals, they may be connected together into a single 50Ω device (such as a filter). An external LNA or PA may be used, if desired, but an external RX/TX switch may be required.

The VCO is a very sensitive block in the system. RF signals feeding back into the VCO (either radiated or coupled by traces) may cause the PLL to become unlocked. The trace(s) for the anode of the tuning varactor should also be kept short. The layout of the resonator and varactor are very important. The capacitor and varactor should be close to the RF2945 pins, and the trace length should be as short as possible. The inductors may be placed further away, and reducing the value of the inductors can compensate any trace inductance. Printed inductors may also be used with careful design. For best results, physical layout should be as symmetrical as possible. Figure 1 is a recommended layout pattern for the VCO components. When using the loop bandwidth lower than 5kHz shown on the evaluation board, better filtering of the VCC at the resonators (and lower VCC noise, as well) will help reduce phase noise of the VCO. A series resistor of 100Ω to 200Ω, and a 1µF or larger capacitor may be used.

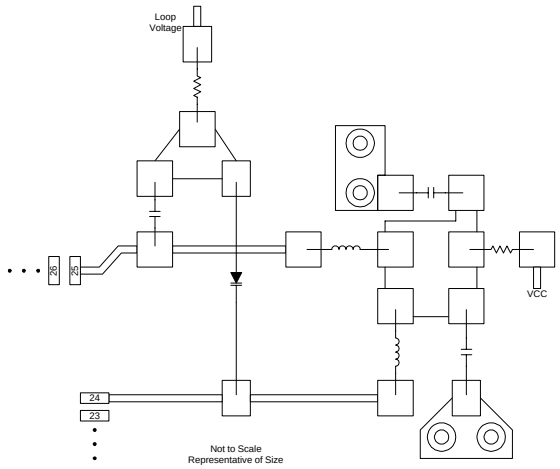


Figure 1. Recommended VCO Layout

For the interface between the LNA/mixer, the coupling capacitor should be as close to the RF2945 pins as possible, with the bias inductors further away. Once again, the value of the inductor may be changed to compensate for trace inductance. The output impedance of the LNA is in the order of several kΩ, which makes matching to 50Ω very difficult. If image filtering is desired, a high impedance filter is recommended.

The quad tank of the discriminator may be implemented with ceramic discriminator available from a couple of sources. This design works well for wideband applications where temperature range is limited. The temperature coefficient of ceramic discriminators may be in the order of +50ppm/°C. The alternative to the ceramic discriminator is the LC tank, which provides a broadband discriminator more useful for high data rates.

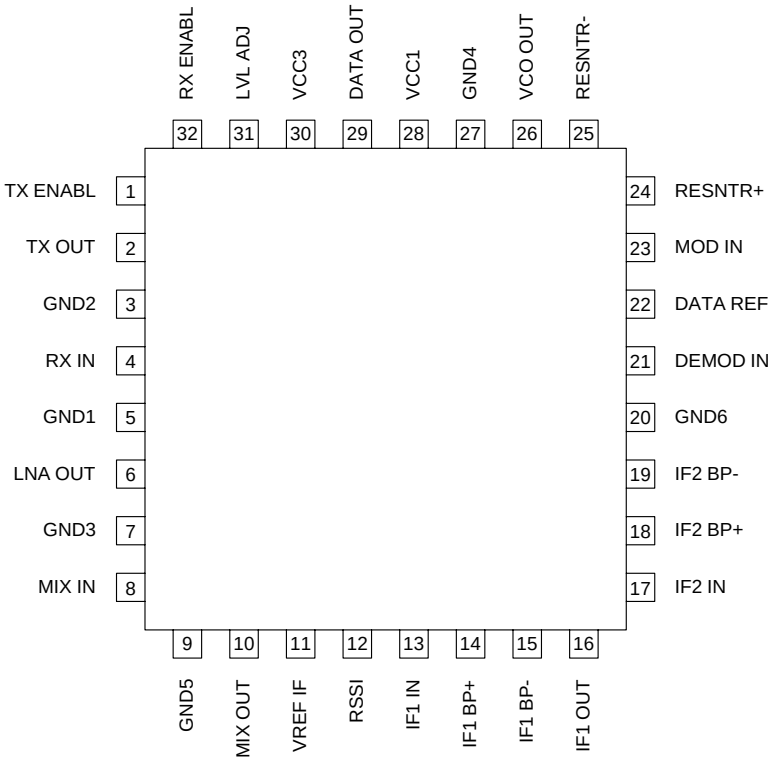
PLL Synthesizer

The RF2945 evaluation board uses an LMX2316 PLL IC from National Semiconductor. This PLL IC may be programmed from the software available from National Semiconductor (codeloader at www.national.com/appinfo/wireless/). An external reference oscillator is required for the PLL IC allowing for the evaluation of different reference frequencies or step sizes. The National Semiconductor software also has a calculator for determining the R and C component values for a given loop bandwidth.

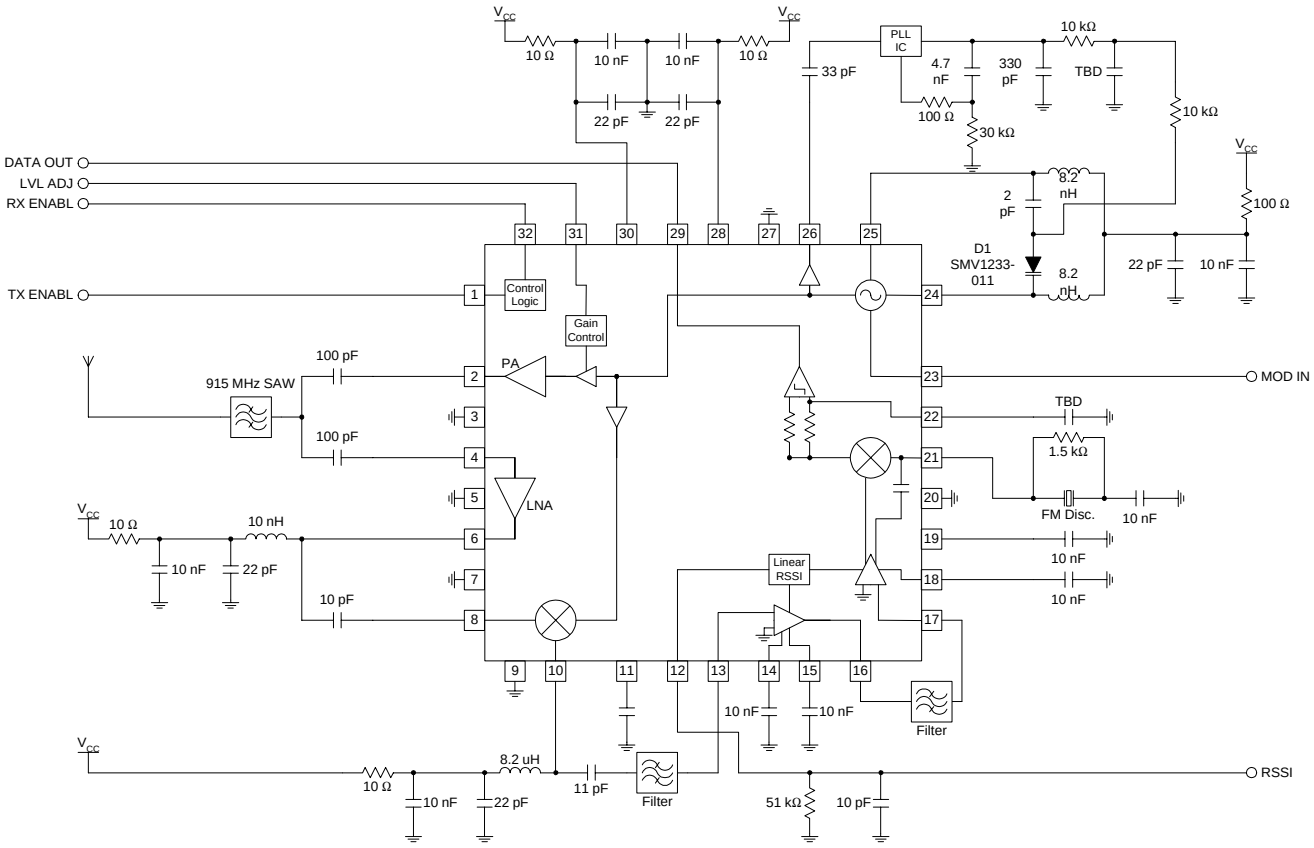
The RF2945 is controlled by RX ENABL and TX ENABL which are decoded to put the RF2945 into one of four states. It may be put into a PLL-only mode with TX ENABL and RX ENABL both high. This condition is used to provide time for the synthesizer to turn on and obtain lock before turning on the receiver or transmitter. Note that LVL ADJ needs to be held low for PLL-only mode. Sometimes, it is desirable to ramp up the power amplifier to minimize load pulling on the VCO. To do this with the RF2945, first put the RF2945 into PLL mode by putting TX ENABL and RX ENABL high. Then, ramp up LVL ADJ to turn on the transmitter and PA. The rate at which LVL ADJ is allowed to ramp up is dependent on the PLL loop bandwidth. VCC pushing also affects the VCO frequency. A good low pass filter on VCC will minimize the VCC pushing effects.

For applications requiring fast switching speeds or turn-on times, and low data rate loop filter bandwidths, the LMX2316 may be configured to drive the loop filter in a fast switching mode. Please refer to literature on the LMX2316 for more information.

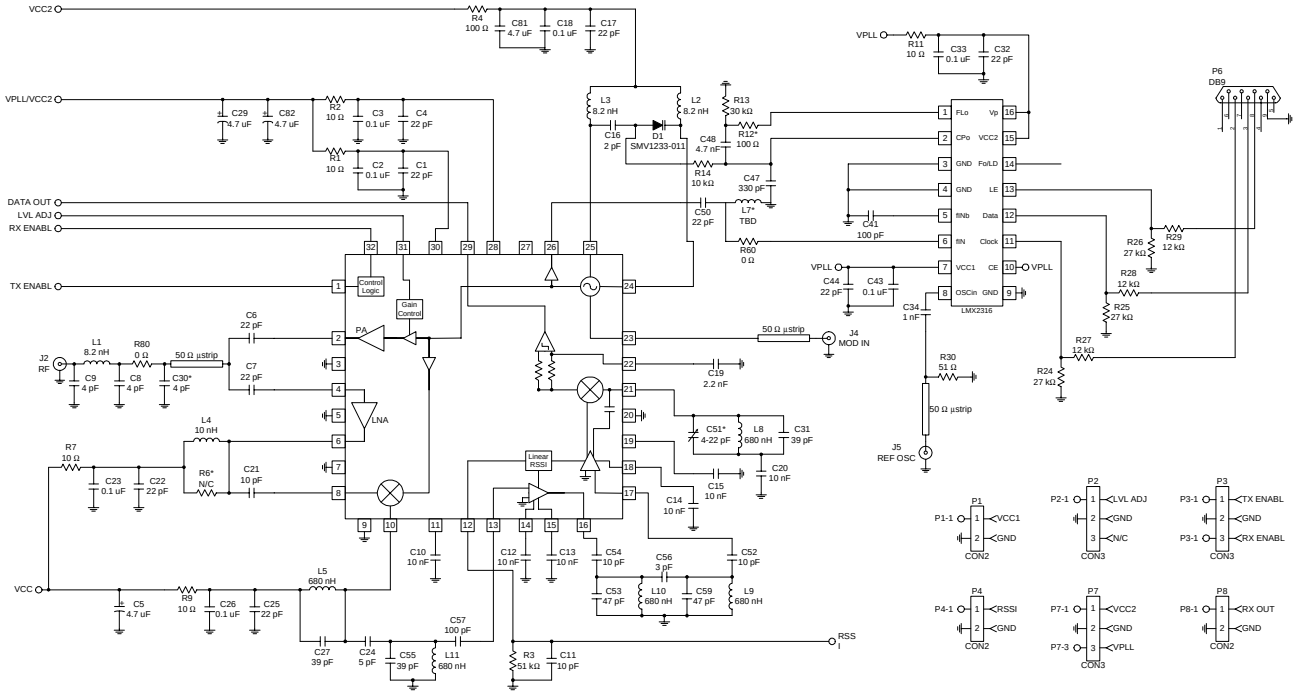
Pin Out


1 TX ENABL
2 TX OUT
3 GND2
4 RX IN
5 GND1
6 LNA OUT
7 GND3
8 MIX IN
9 GND5
10 MIX OUT
11 VREF IF
12 RSSI
13 IF1 IN
14 IF1 BP+
15 IF1 BP-
16 IF1 OUT
17 IF2 IN
18 IF2 BP+
19 IF2 BP-
20 GND6
21 DEMOD IN
22 DATA REF
23 MOD IN
24 RESNTR+
25 RESNTR-
26 VCO OUT
27 GND4
28 VCC1
29 DATA OUT
30 VCC3
31 LVL ADJ
32 RX ENABL

Application Schematic - 915 MHz

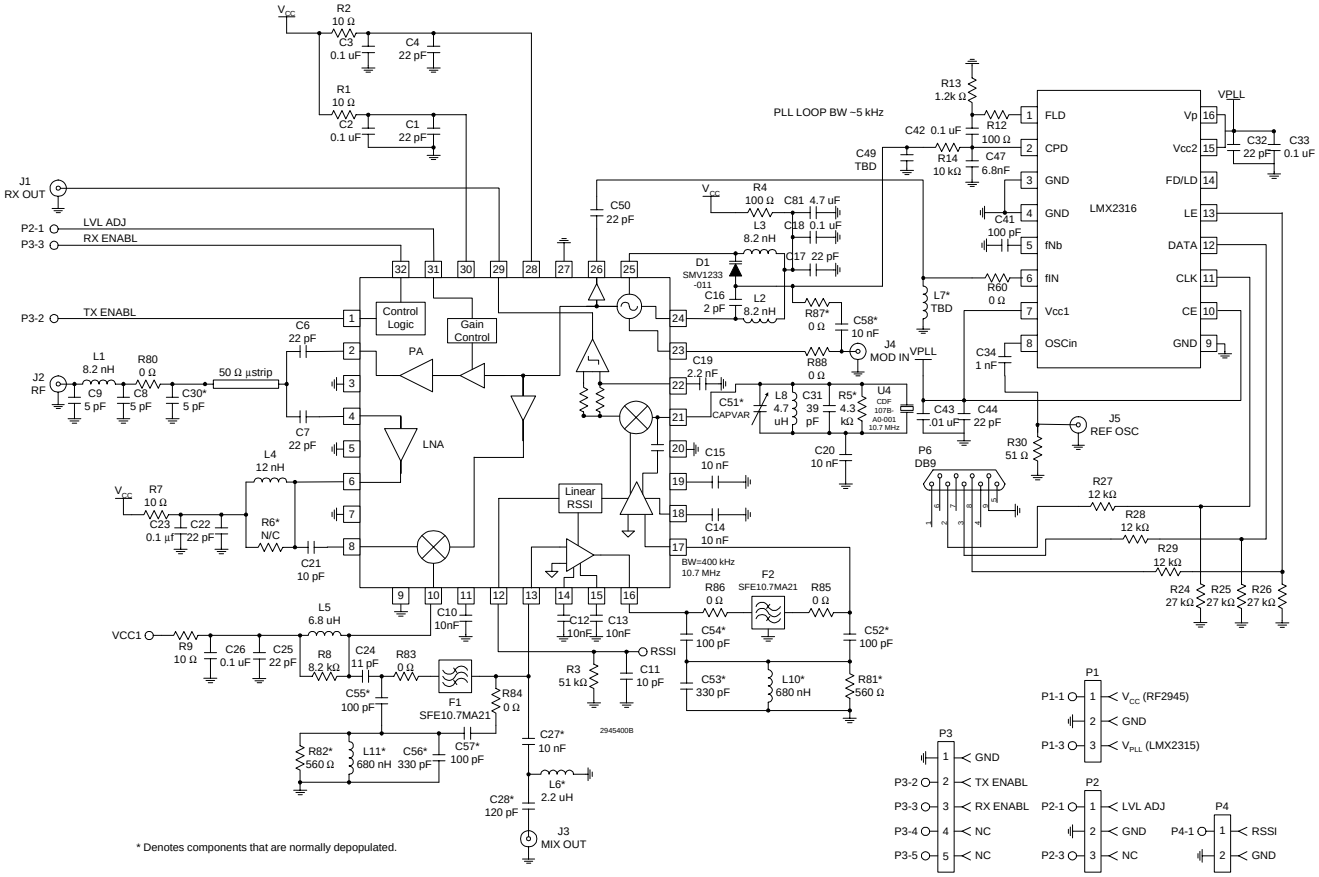


Application Schematic - 915 MHz
IF=25MHz, BW=2MHz



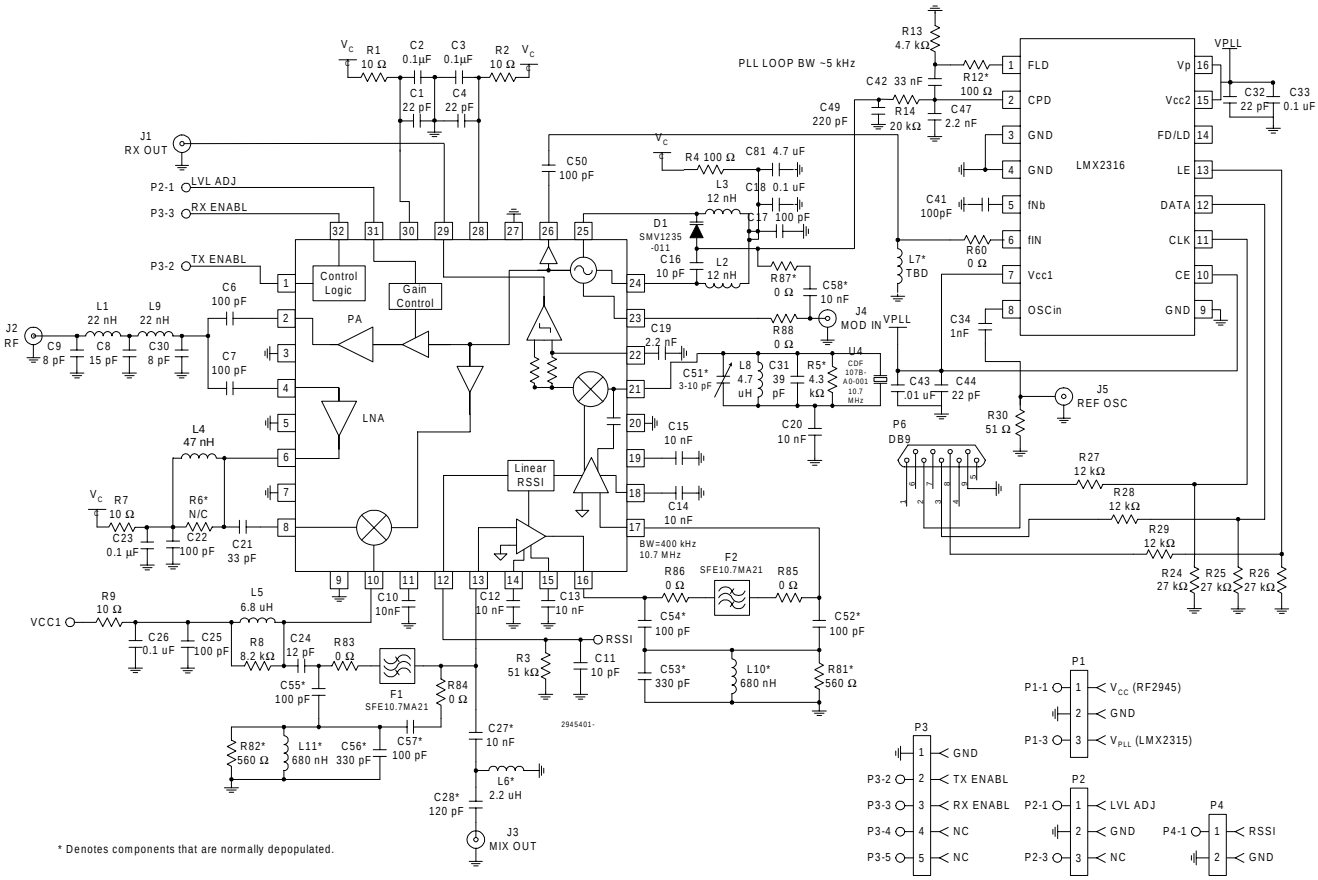
Evaluation Board Schematic - 915MHz

(Download Bill of Materials from www.rfmd.com.)

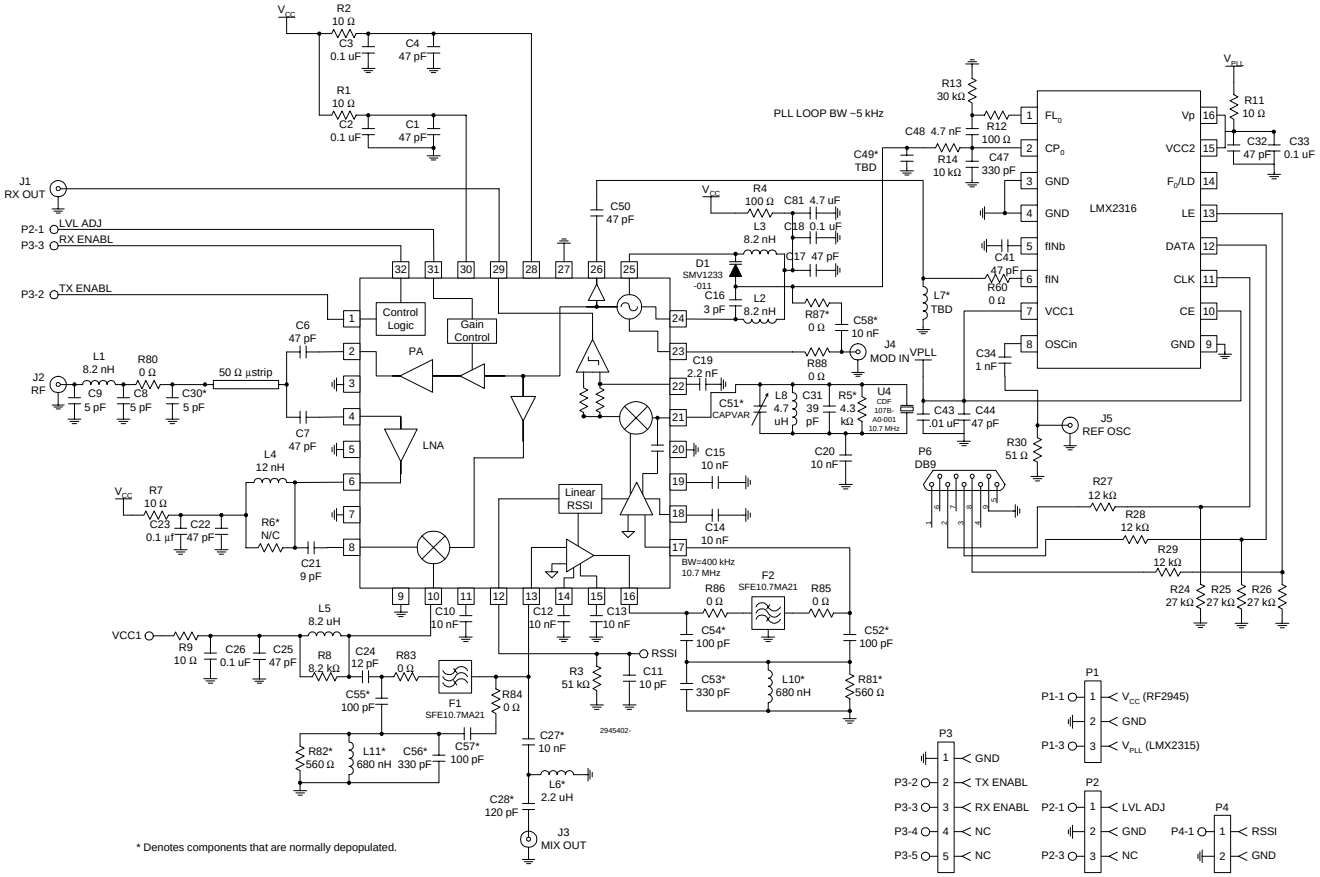


* Denotes components that are normally depopulated.

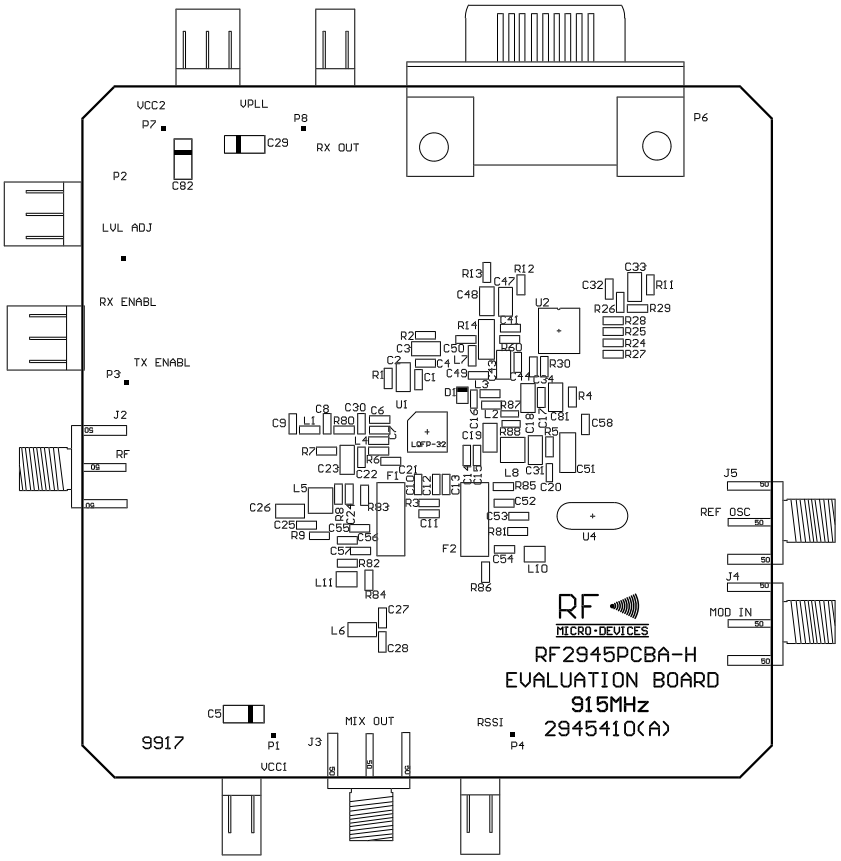
Evaluation Board Schematic - 433MHz

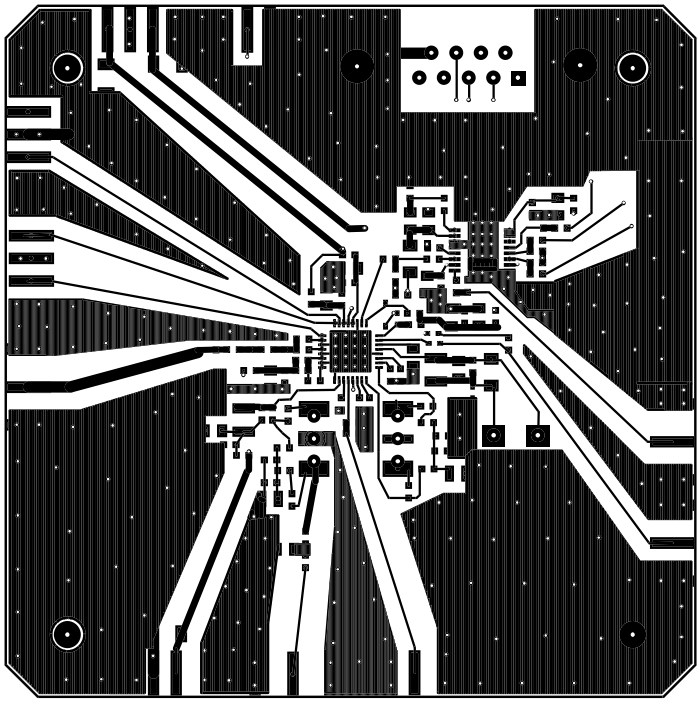


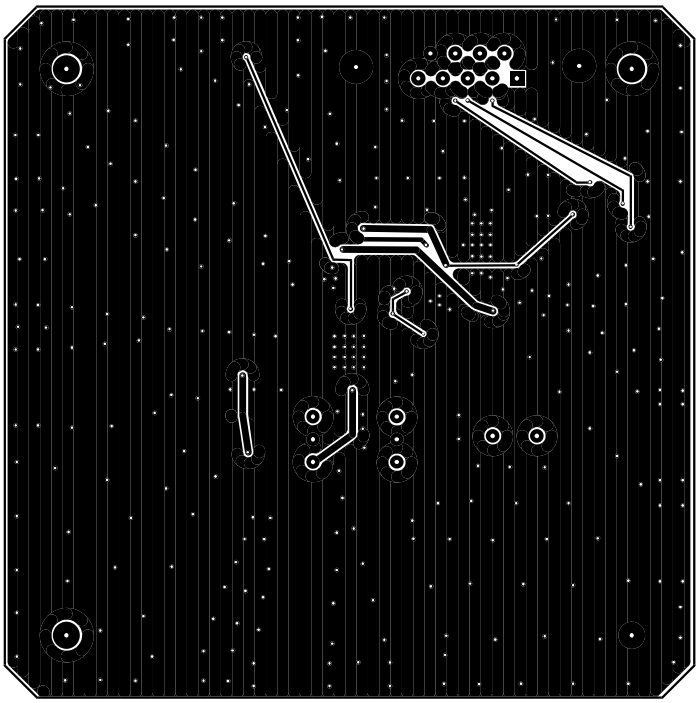
Evaluation Board Schematic - 868MHz



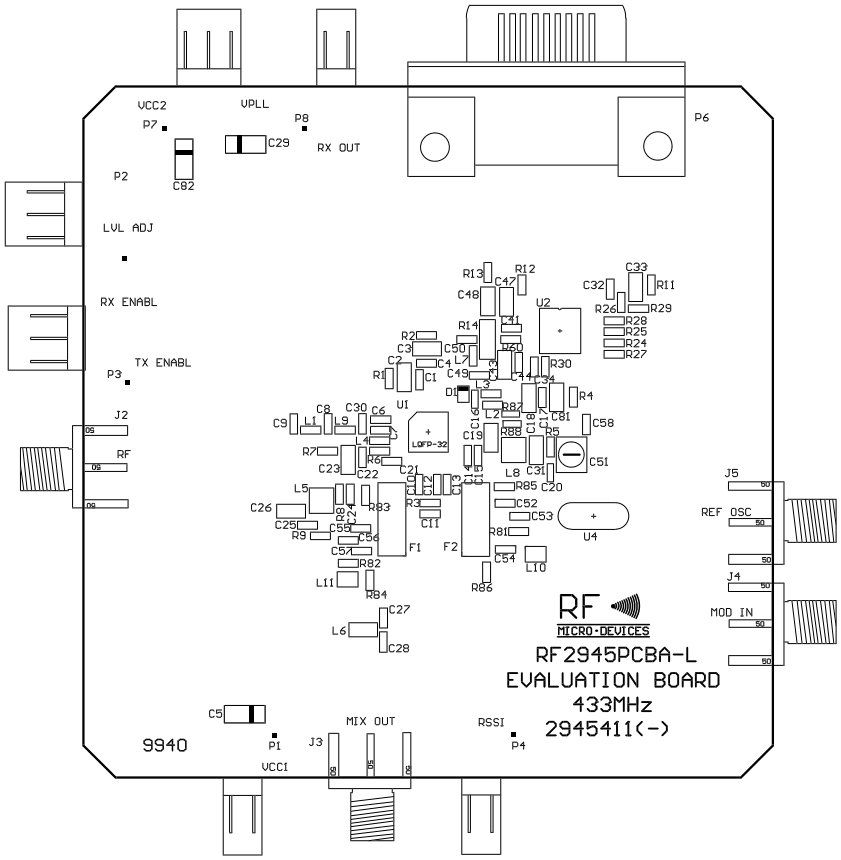
Evaluation Board Layout - 915MHz
Board Size 3.050” x 3.050”
Board Thickness 0.031”, Board Material FR-4

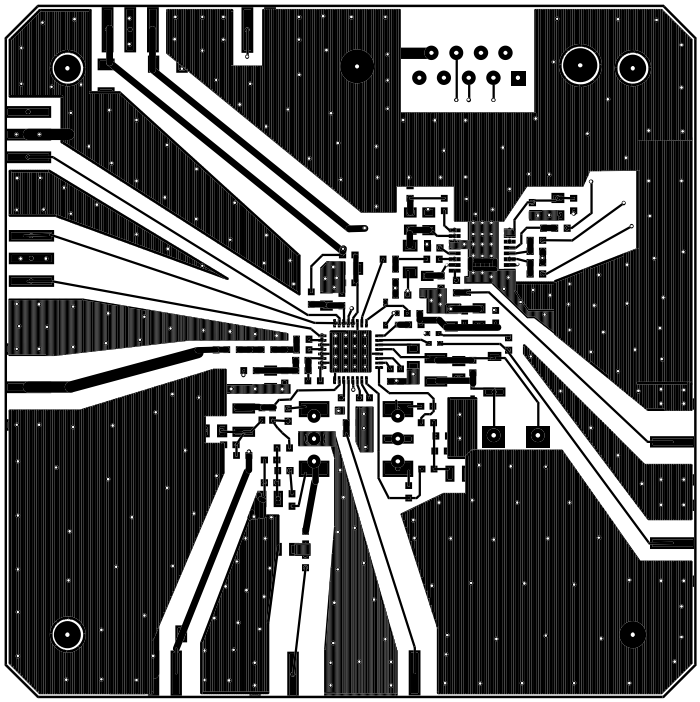


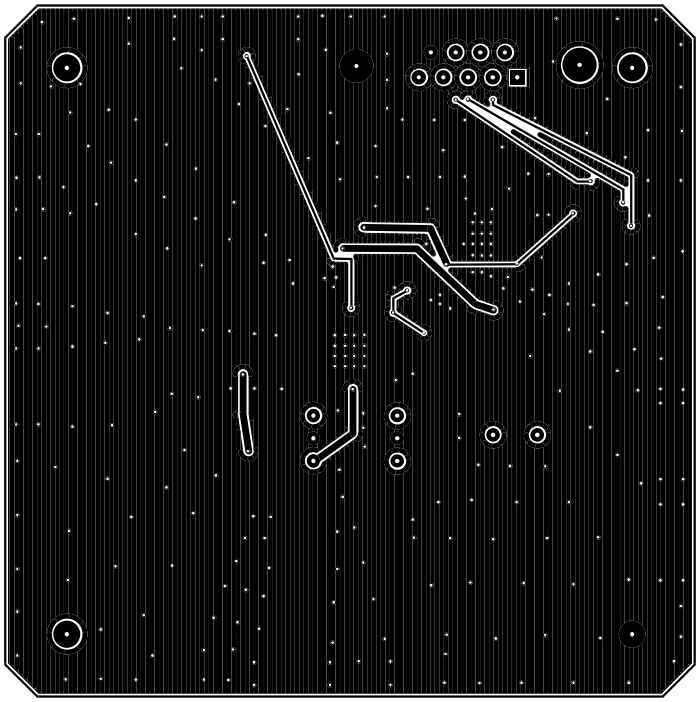




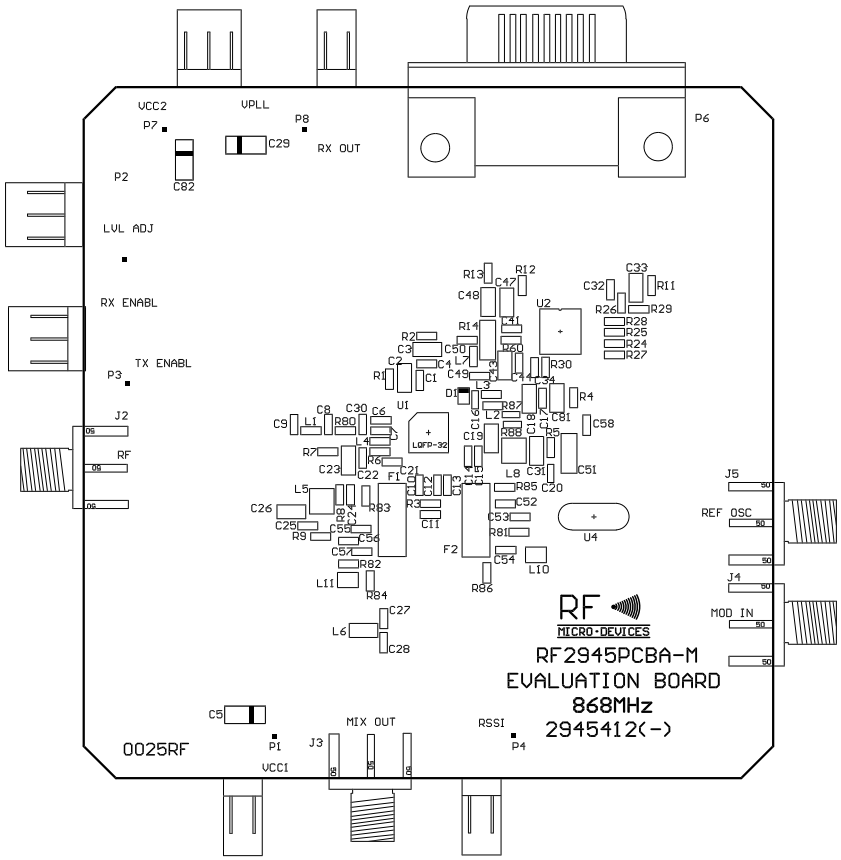
Evaluation Board Layout - 433MHz

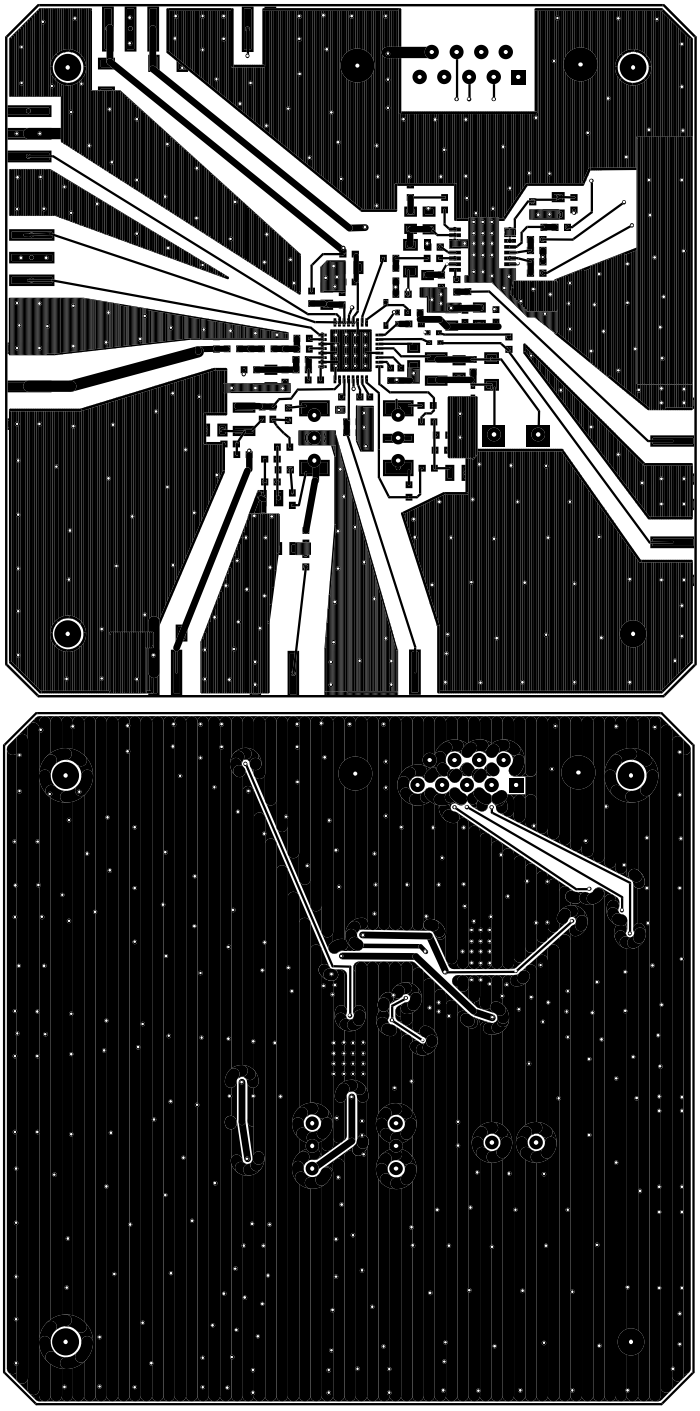




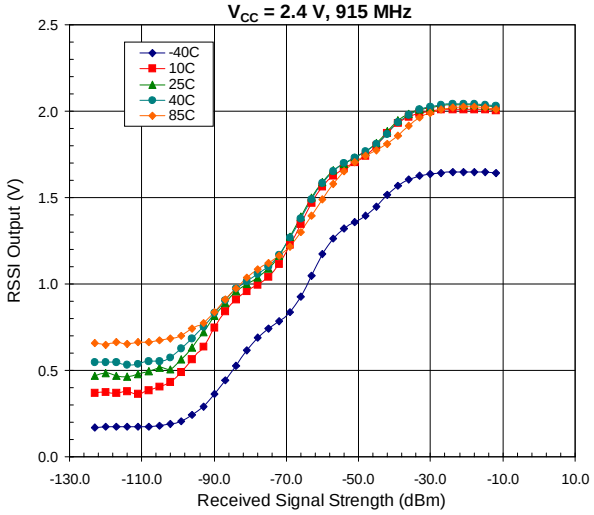


Evaluation Board Layout - 868MHz

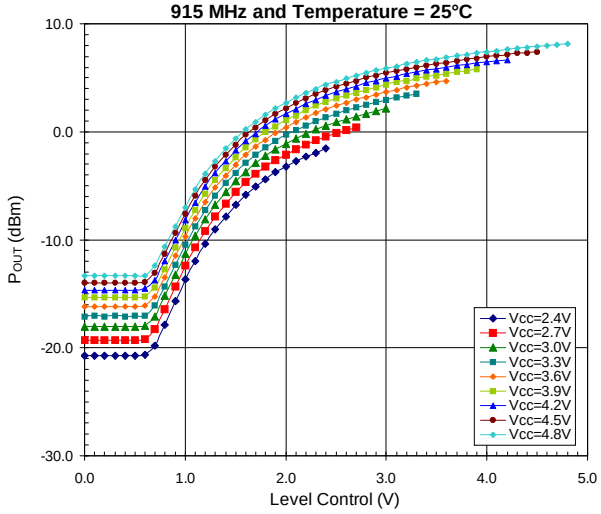




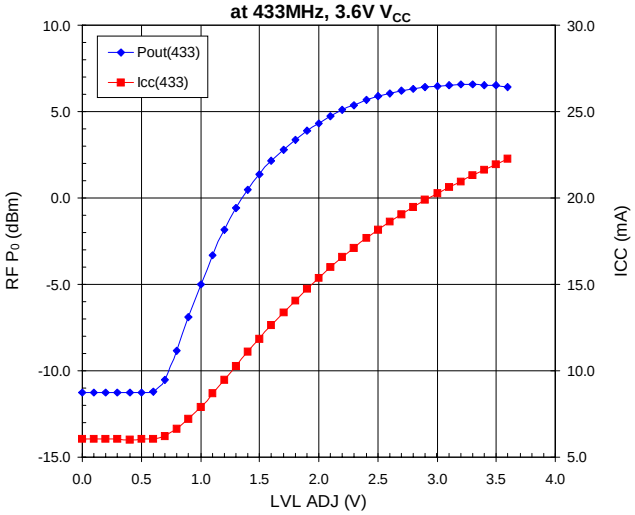
RSSI Output versus Temperature
V_{CC} = 2.4 V, 915 MHz



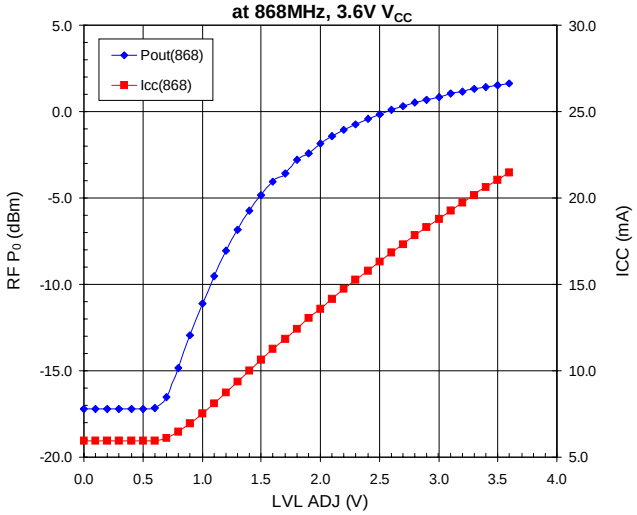
P_{OUT} versus Level Control and V_{CC}
915 MHz and Temperature = 25°C



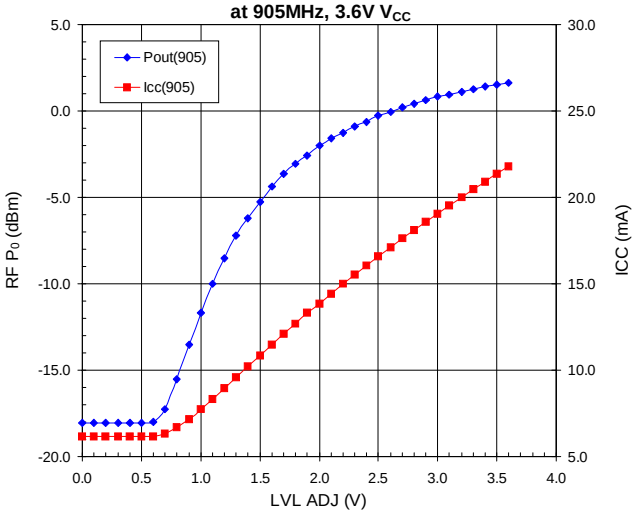
TX Power Output and ICC versus Level Adjust
at 433MHz, 3.6V V_{CC}



TX Power Output and ICC versus Level Adjust
at 868MHz, 3.6V V_{CC}



TX Power Output and ICC versus Level Adjust
at 905MHz, 3.6V V_{CC}



Receive Current versus V_{CC}
(Excluding PLL IC)