

DATA SHEET

74LVC2G14

**Dual inverting Schmitt-trigger with
5 V tolerant input**

Product specification
Supersedes data of 2003 Jul 31

2004 Sep 08

Dual inverting Schmitt-trigger with 5 V tolerant input

74LVC2G14

FEATURES

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V).
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Multiple package options
- ESD protection:
 - HBM EIA/JESD22-A114-B exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C.

APPLICATIONS

- Wave and pulse shapers for highly noisy environments
- Astable multivibrators
- Monostable multivibrators.

DESCRIPTION

The 74LVC2G14 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device as translator in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{off} . The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC2G14A provides two inverting buffers with Schmitt-trigger action. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay input nA to output nY	$V_{CC} = 1.8$ V; $C_L = 30$ pF; $R_L = 1$ k Ω	5.6	ns
		$V_{CC} = 2.5$ V; $C_L = 30$ pF; $R_L = 500$ Ω	3.7	ns
		$V_{CC} = 2.7$ V; $C_L = 50$ pF; $R_L = 500$ Ω	4.1	ns
		$V_{CC} = 3.3$ V; $C_L = 50$ pF; $R_L = 500$ Ω	3.9	ns
		$V_{CC} = 5.0$ V; $C_L = 50$ pF; $R_L = 500$ Ω	2.7	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	$V_{CC} = 3.3$ V; notes 1 and 2	18.1	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total switching outputs;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

2. The condition is $V_I = \text{GND}$ to V_{CC} .

Dual inverting Schmitt-trigger with 5 V tolerant input

74LVC2G14

FUNCTION TABLE

See note 1.

INPUT		OUTPUT	
nA		nY	
L		H	
H		L	

Note

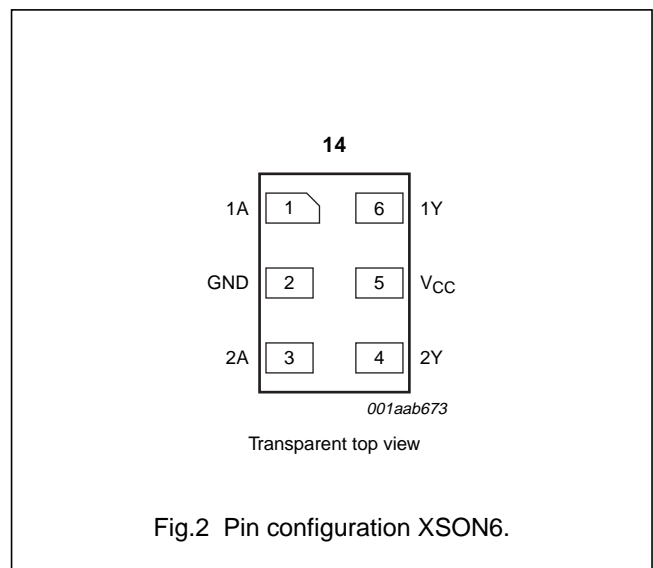
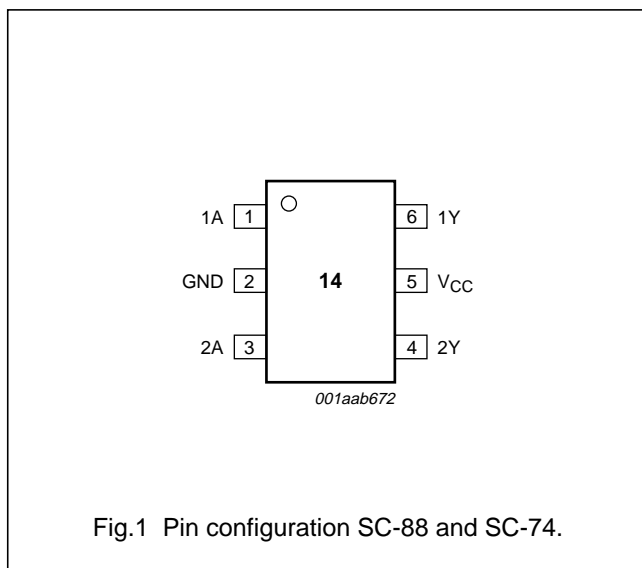
1. H = HIGH voltage level;
L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC2G14GW	-40 °C to +125 °C	6	SC-88	plastic	SOT363	VK
74LVC2G14GV	-40 °C to +125 °C	6	SC-74	plastic	SOT457	V14
74LVC2G14GM	-40 °C to +125 °C	6	XSON6	plastic	SOT886	VK

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	GND	ground (0 V)
3	2A	data input
4	2Y	data output
5	V _{CC}	supply voltage
6	1Y	data output



Dual inverting Schmitt-trigger with 5 V tolerant input

74LVC2G14

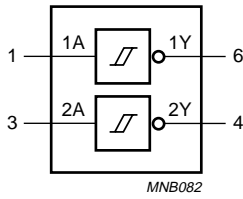


Fig.3 Logic symbol.

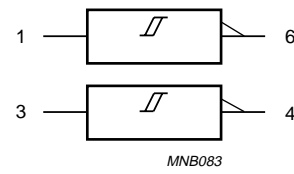


Fig.4 IEEE/IEC logic symbol.

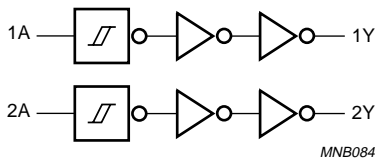


Fig.5 Logic diagram.

Dual inverting Schmitt-trigger with 5 V tolerant input

74LVC2G14

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	operating ambient temperature		-40	+125	°C

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V	-	-50	mA
V_I	input voltage	note 1	-0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	enable mode; notes 1 and 2	-0.5	$V_{CC} + 0.5$	V
		Power-down mode; notes 1 and 2	-0.5	+6.5	V
I_O	output source or sink current	$V_O = 0$ V to V_{CC}	-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	±100	mA
T_{stg}	storage temperature		-65	+150	°C
P_D	power dissipation	$T_{amb} = -40$ °C to +125 °C	-	300	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.

Dual inverting Schmitt-trigger with 5 V tolerant input

74LVC2G14

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = -40 °C to +85 °C; note 1							
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}	1.65 to 5.5	–	–	0.1	V
		I _O = 100 μA	1.65	–	–	0.45	V
		I _O = 4 mA	2.3	–	–	0.3	V
		I _O = 8 mA	2.7	–	–	0.4	V
		I _O = 12 mA	3.0	–	–	0.55	V
		I _O = 24 mA	4.5	–	–	0.55	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}	1.65 to 5.5	V _{CC} – 0.1	–	–	V
		I _O = -100 μA	1.65	1.2	–	–	V
		I _O = -4 mA	2.3	1.9	–	–	V
		I _O = -8 mA	2.7	2.2	–	–	V
		I _O = -12 mA	3.0	2.3	–	–	V
		I _O = -24 mA	4.5	3.8	–	–	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	5.5	–	±0.1	±5	μA
I _{off}	power OFF leakage current	V _I or V _O = 5.5 V	0	–	±0.1	±10	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A	5.5	–	0.1	10	μA
ΔI _{CC}	additional quiescent supply current per pin	V _I = V _{CC} – 0.6 V; I _O = 0 A	2.3 to 5.5	–	5	500	μA

Dual inverting Schmitt-trigger with
5 V tolerant input

74LVC2G14

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 °C to +125 °C							
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}	1.65 to 5.5	–	–	0.1	V
		I _O = 100 μA	1.65	–	–	0.70	V
		I _O = 4 mA	2.3	–	–	0.45	V
		I _O = 8 mA	2.7	–	–	0.60	V
		I _O = 12 mA	3.0	–	–	0.80	V
		I _O = 24 mA	4.5	–	–	0.80	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}	1.65 to 5.5	V _{CC} – 0.1	–	–	V
		I _O = -100 μA	1.65	0.95	–	–	V
		I _O = -4 mA	2.3	1.7	–	–	V
		I _O = -8 mA	2.7	1.9	–	–	V
		I _O = -12 mA	3.0	2.0	–	–	V
		I _O = -24 mA	4.5	3.4	–	–	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	5.5	–	–	±20	μA
I _{off}	power OFF leakage current	V _I or V _O = 5.5 V	0	–	–	±20	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A	5.5	–	–	40	μA
ΔI _{CC}	additional quiescent supply current per pin	V _I = V _{CC} – 0.6 V; I _O = 0 A	2.3 to 5.5	–	–	5000	μA

Note

- All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

Dual inverting Schmitt-trigger with
5 V tolerant input

74LVC2G14

TRANSFER CHARACTERISTICS

Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 °C to +85 °C; note 1							
V _{T+}	positive-going threshold	see Figs 6 and 7	1.8	0.70	1.10	1.50	V
			2.3	1.00	1.40	1.80	V
			3.0	1.30	1.76	2.20	V
			4.5	1.90	2.47	3.10	V
			5.5	2.20	2.91	3.60	V
V _{T-}	negative-going threshold	see Figs 6 and 7	1.8	0.25	0.61	0.90	V
			2.3	0.40	0.80	1.15	V
			3.0	0.60	1.04	1.50	V
			4.5	1.00	1.55	2.00	V
			5.5	1.20	1.86	2.30	V
V _H	hysteresis (V _{T+} - V _{T-})	see Figs 6, 7 and 8	1.8	0.15	0.49	1.00	V
			2.3	0.25	0.60	1.10	V
			3.0	0.40	0.73	1.20	V
			4.5	0.60	0.92	1.50	V
			5.5	0.70	1.02	1.70	V
T_{amb} = -40 °C to +125 °C							
V _{T+}	positive-going threshold	see Figs 6 and 7	1.8	0.70	–	1.70	V
			2.3	1.00	–	2.00	V
			3.0	1.30	–	2.40	V
			4.5	1.90	–	3.30	V
			5.5	2.20	–	3.80	V
V _{T-}	negative-going threshold	see Figs 6 and 7	1.8	0.25	–	1.10	V
			2.3	0.40	–	1.35	V
			3.0	0.60	–	1.70	V
			4.5	1.00	–	2.20	V
			5.5	1.20	–	2.50	V
V _H	hysteresis (V _{T+} - V _{T-})	see Figs 6, 7 and 8	1.8	0.15	–	1.20	V
			2.3	0.25	–	1.30	V
			3.0	0.40	–	1.40	V
			4.5	0.60	–	1.70	V
			5.5	0.70	–	1.90	V

Note1. All typical values are measured at T_{amb} = 25 °C.

Dual inverting Schmitt-trigger with 5 V tolerant input

74LVC2G14

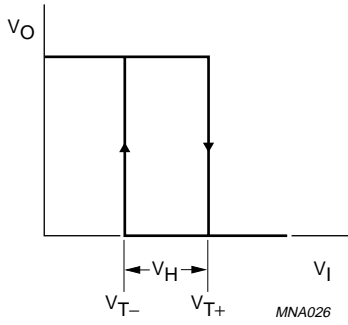
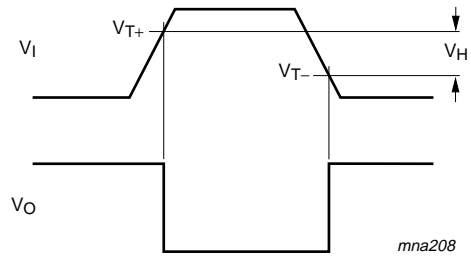
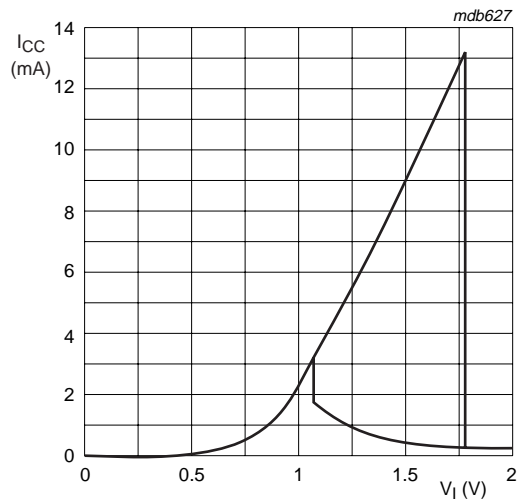


Fig.6 Transfer characteristic.



V_{T+} and V_{T-} are limits of 20 % and 70 %.

Fig.7 Definition of V_{T+} , V_{T-} and V_H .



$V_{CC} = 3.0\text{ V.}$

Fig.8 Typical transfer characteristic.

Dual inverting Schmitt-trigger with 5 V tolerant input

74LVC2G14

AC CHARACTERISTICS

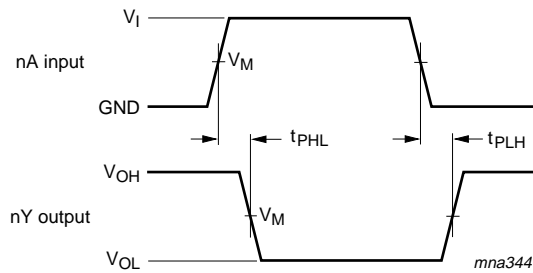
GND = 0 V.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 °C to +85 °C; note 1							
t _{PHL} /t _{PLH}	propagation delay input nA to output nY	see Figs 9 and 10	1.65 to 1.95	1.0	5.6	11.0	ns
			2.3 to 2.7	0.5	3.7	6.5	ns
			2.7	0.5	4.1	7.0	ns
			3.0 to 3.6	0.5	3.9	6.0	ns
			4.5 to 5.5	0.5	2.7	4.3	ns
T_{amb} = -40 °C to +125 °C							
t _{PHL} /t _{PLH}	propagation delay input nA to output nY	see Figs 9 and 10	1.65 to 1.95	1.0	–	12.0	ns
			2.3 to 2.7	0.5	–	7.2	ns
			2.7	0.5	–	7.7	ns
			3.0 to 3.6	0.5	–	6.7	ns
			4.5 to 5.5	0.5	–	4.7	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

AC WAVEFORMS



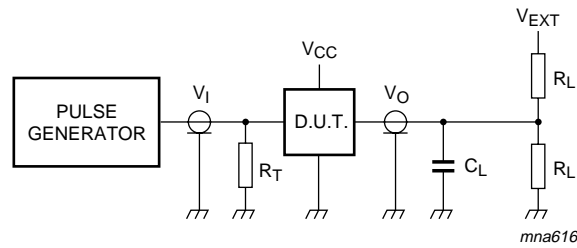
V _{CC}	V _M	INPUT	
		V _I	t _r = t _f
1.65 V to 1.95 V	0.5 × V _{CC}	V _{CC}	≤ 2.0 ns
2.3 V to 2.7 V	0.5 × V _{CC}	V _{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	0.5 × V _{CC}	V _{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.9 The input (nA) to output (nY) propagation delays.

Dual inverting Schmitt-trigger with
5 V tolerant input

74LVC2G14



V _{CC}	V _I	C _L	R _L	V _{EXT}
				t _{PLH} /t _{PHL}
1.65 V to 1.95 V	V _{CC}	30 pF	1 kΩ	open
2.3 V to 2.7 V	V _{CC}	30 pF	500 Ω	open
2.7 V	2.7 V	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open
4.5 V to 5.5 V	V _{CC}	50 pF	500 Ω	open

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

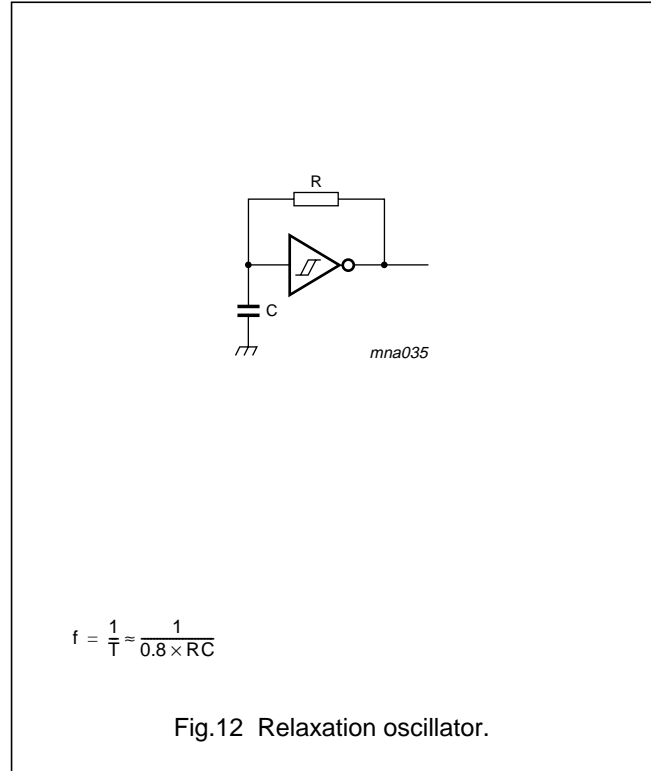
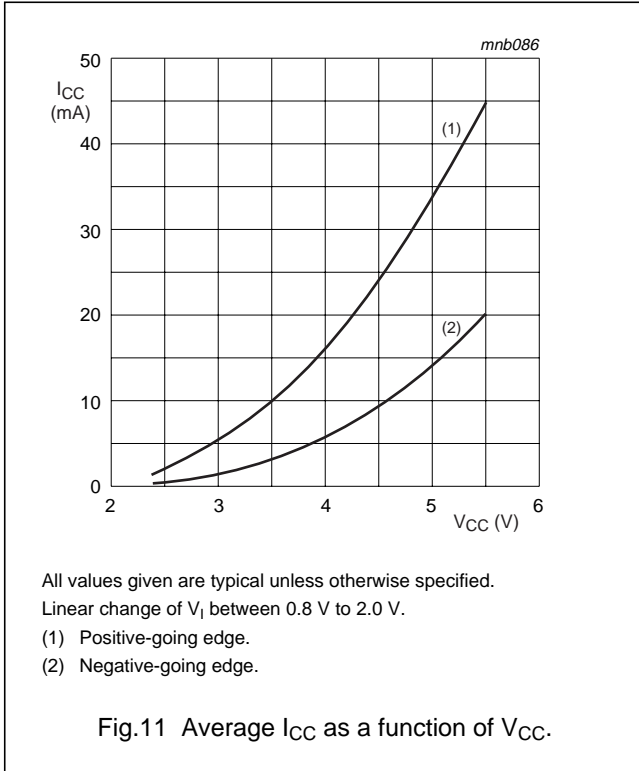
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.10 Load circuitry for switching times.

Dual inverting Schmitt-trigger with 5 V tolerant input

74LVC2G14

APPLICATION INFORMATION



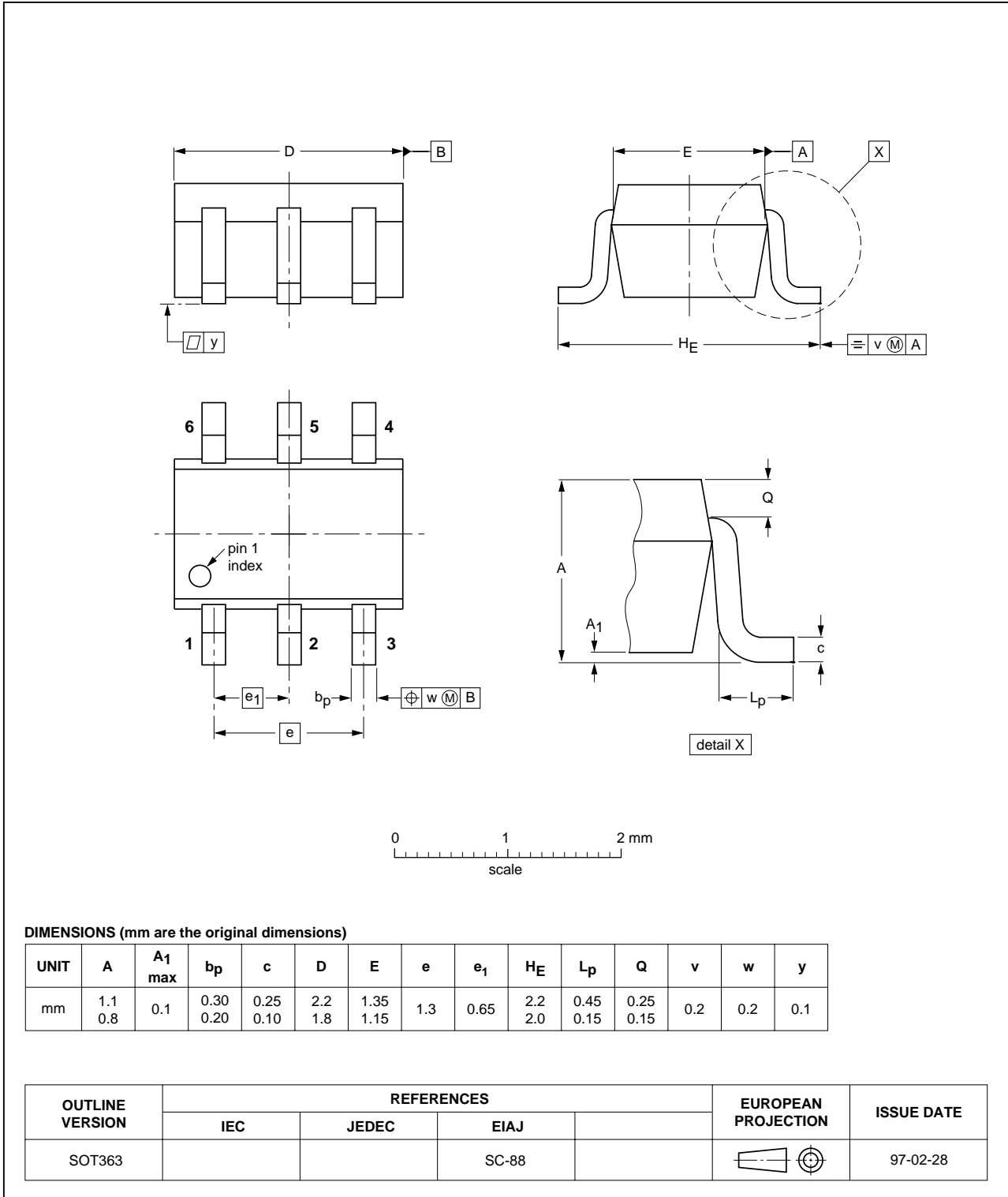
Dual inverting Schmitt-trigger with 5 V tolerant input

74LVC2G14

PACKAGE OUTLINES

Plastic surface mounted package; 6 leads

SOT363

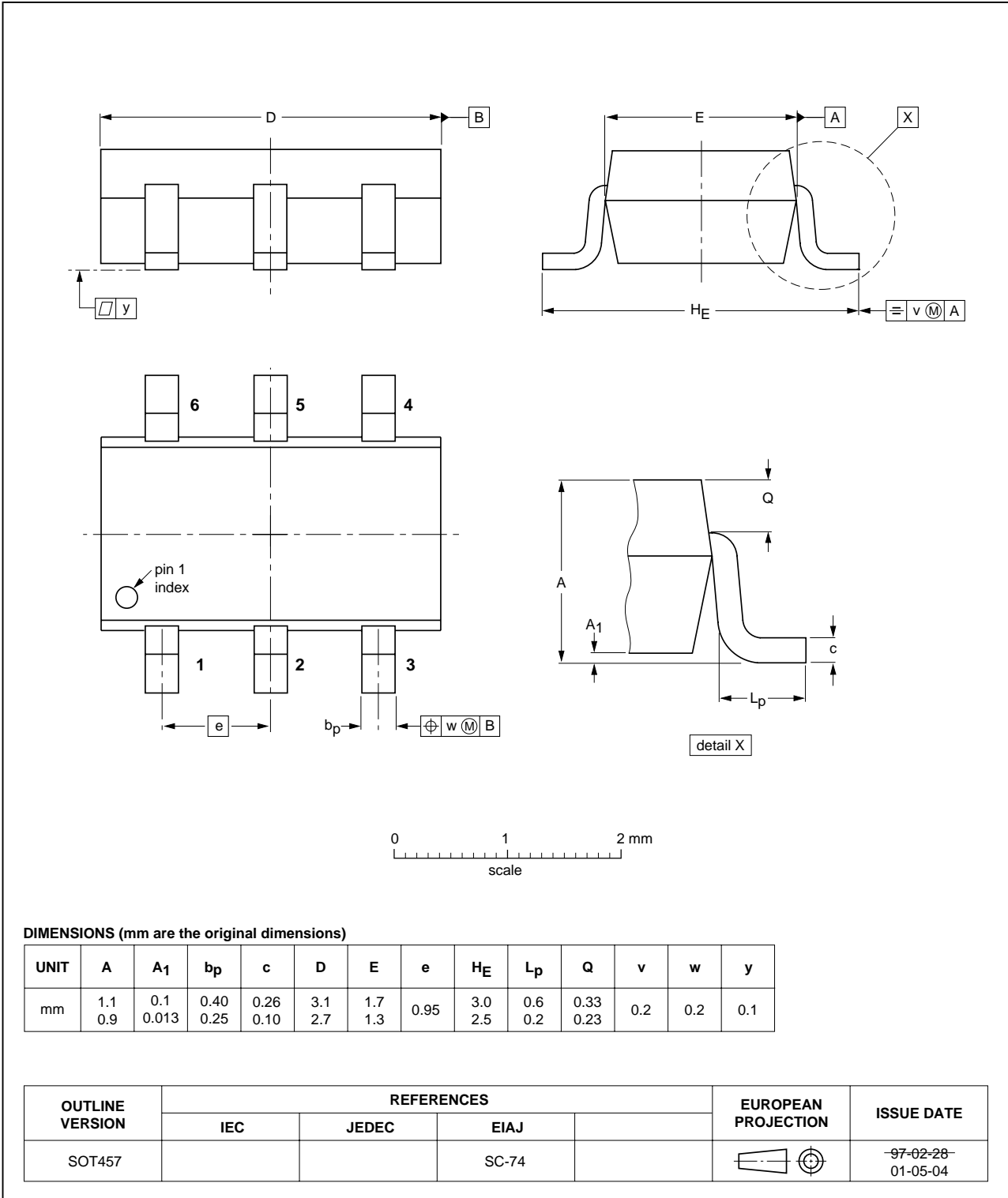


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Plastic surface mounted package; 6 leads

SOT457

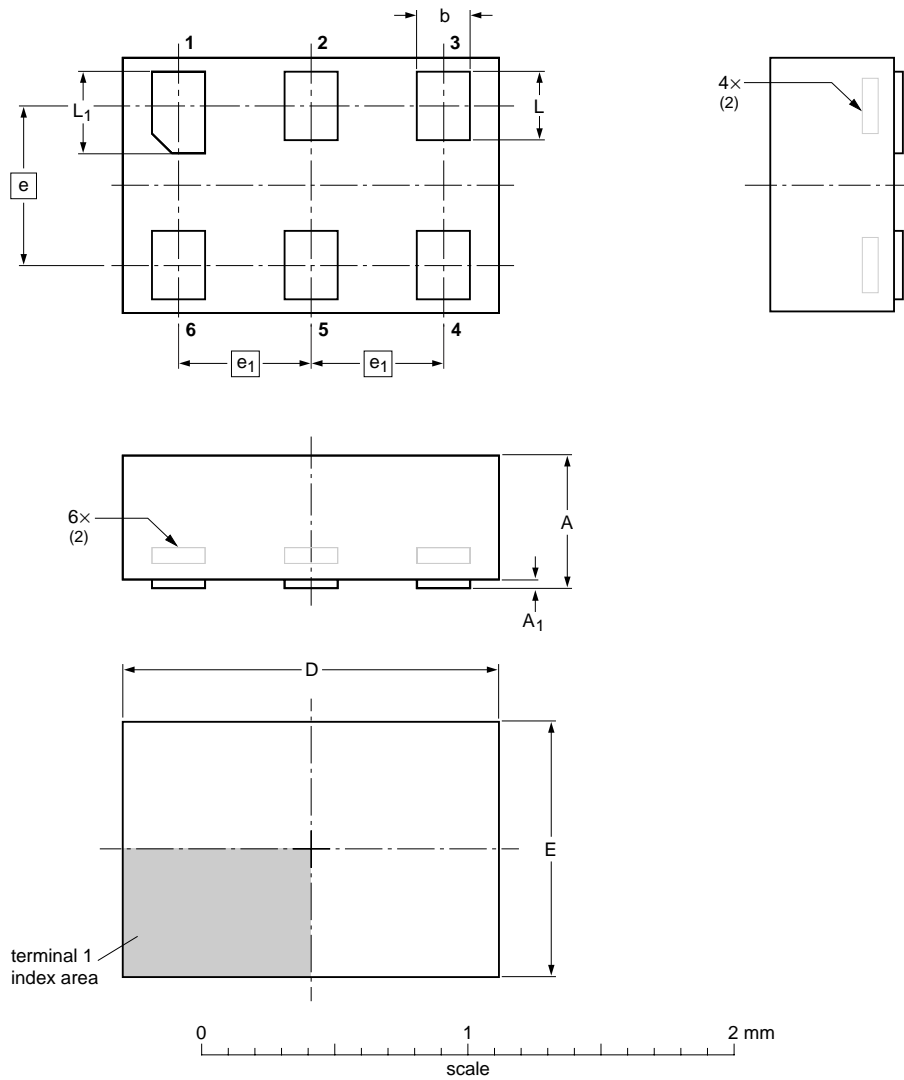


Dual inverting Schmitt-trigger with 5 V tolerant input

74LVC2G14

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max	A ₁ max	b	D	E	e	e ₁	L	L ₁
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT886		MO-252			04-07-15 04-07-22

Dual inverting Schmitt-trigger with 5 V tolerant input

74LVC2G14

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LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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