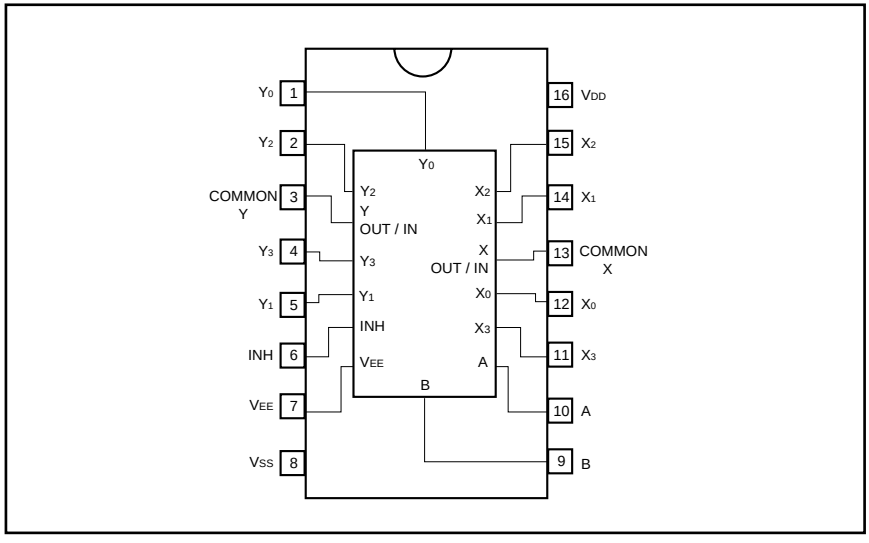
Dual 4-channel analog multiplexer / demultiplexer

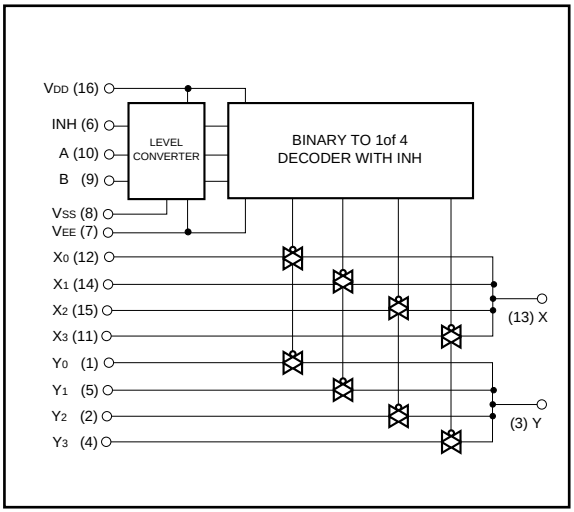
BU4052BC / BU4052BCF / BU4052BCFV

The BU4052BC, BU4052BCF, and BU4052BCFV are multiplexers / demultiplexers capable of selecting and combining analog signals and digital signals with a configuration of 4 ch × 2.
Inhibit signals and control signals are used to turn on the switch of the corresponding channel. In addition, even if the logical amplitude (V_{DD}-V_{SS}) of the control signal is low, signals with a large amplitude (V_{DD}-V_{EE}) can be switched.
In addition, as each switch has a low ON resistance, it can be connected to a low impedance circuit.

●Block diagram



●Logic circuit diagram



●Truth table

INH	A	B	ON SWITCH
L	L	L	X_0 Y_0
L	H	L	X_1 Y_1
L	L	H	X_2 Y_2
L	H	H	X_3 Y_3
H	X	X	NONE

X: Irrelevant

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage 1	V_{DD}	– 0.5 ~ + 20	V
Power supply voltage 2	V_{DD} — V_{EE}	– 0.5 ~ + 20	V
Power dissipation	Pd	1000 (DIP), 500 (SOP), 400 (SSOP)	mW
Operating temperature	Topr	– 40 ~ + 85	°C
Storage temperature	Tstg	– 55 ~ + 150	°C
Input voltage	V_{IN}	– 0.5 ~ V_{DD} + 0.5	V

●Electrical characteristics

DC characteristics (unless otherwise noted, Ta = 25°C, V_{EE} = V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V_{DD} (V)	Conditions	Measurement circuit
High-level input voltage	V_{IH}	3.5	—	—	V	5	—	Fig.1
		7.0	—	—		10		
		11.0	—	—		15		
Low-level input voltage	V_{IL}	—	—	1.5	V	5	—	Fig.1
		—	—	3.0		10		
		—	—	4.0		15		
High-level input current	I_{IH}	—	—	0.3	µA	15	V_{IH} = 15V	Fig.1
Low-level input current	I_{IL}	—	—	– 0.3	µA	15	V_{IL} = 0V	Fig.1
ON resistance	R_{ON}	—	—	950	Ω	5	V_{IN} = V_{DD} / 2	Fig.2
		—	—	250		10		
		—	—	160		15		
ON resistance deflexion	ΔR_{ON}	—	10	—	Ω	5	—	Fig.2
		—	6	—		10		
		—	4	—		15		
OFF-channel leakage current	I_{OFF}	—	—	0.3	µA	15	—	Fig.3
		—	—	– 0.3		15		
Static current dissipation	I_{DD}	—	—	5	µA	5	V_I = V_{DD} or GND	—
		—	—	10		10		
		—	—	15		15		

Switching characteristics (unless otherwise noted, Ta = 25°C, V_{EE} = V_{SS} = 0V, R_L = 1kΩ, C_L = 50pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V_{DD} (V)	Conditions	Measurement circuit
Propagation delay time Switch IN → OUT	t_{PLH}, t_{PHL}	—	15	45	ns	5	—	Fig.4
		—	8	20		10		
		—	6	15		15		
Propagation delay time CONT → OUT	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	—	170	550	ns	5	—	Fig.5, 6
		—	90	240		10		
		—	70	160		15		
Propagation delay time INH → OUT	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	—	150	380	ns	5	—	Fig.5, 6
		—	70	200		10		
		—	50	160		15		
Maximum propagation frequency	$f_{Max.}$	—	20	—	MHz	5	V_{EE} = – 5V*1	Fig.7
Feedthrough attentuation	FT	—	0.5	—	MHz	5	V_{EE} = – 5V*2	Fig.7
Sine wave distortion ratio	D	—	0.02	—	%	5	V_{EE} = – 5V*3	Fig.7
Input capacitance (control)	C_C	—	5	—	pF	—	—	—
Input capacitance (switch)	C_S	—	10	—	pF	—	—	—

*1 V_{IN} = 5V_{P-P} sine wave, frequency that enables 20 $\log_{10} V_{OUT} / V_{IN}$ = – 3dB.

*2 V_{IN} = 5V_{P-P} sine wave, frequency that enables 20 $\log_{10} V_{OUT} / V_{IN}$ = – 50dB at channel off.

*3 V_{IN} = 5V_{P-P} sine wave.

●Measurement circuits

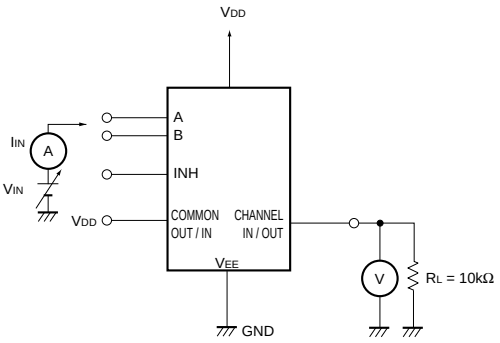


Fig.1 Input voltage, current

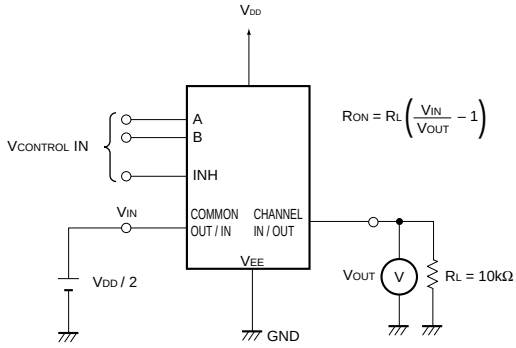


Fig.2 ON resistance

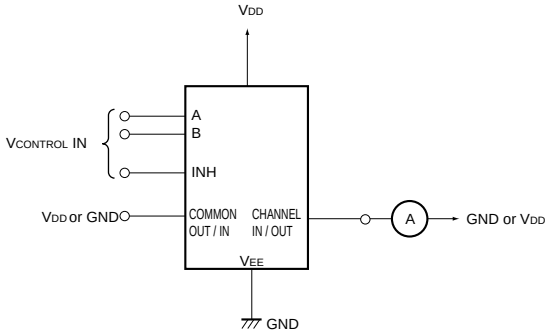


Fig.3 OFF-channel leakage current

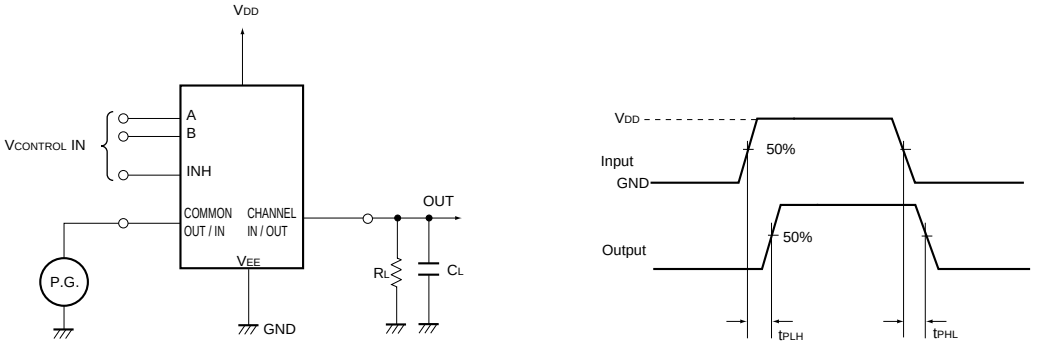


Fig.4 Propagation delay time (Switch IN to OUT)

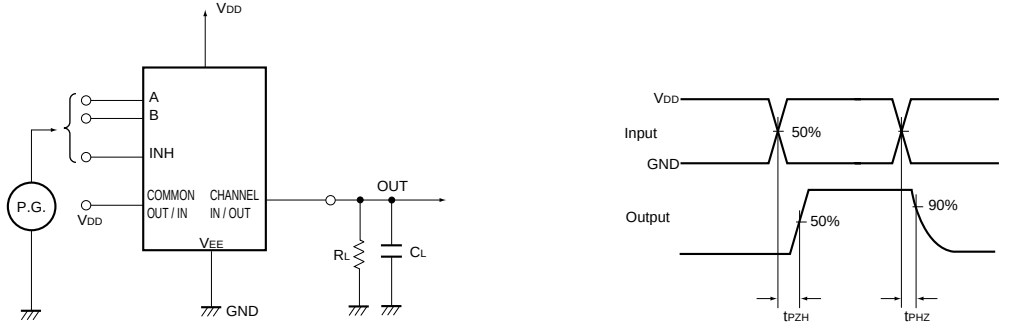


Fig.5 Propagation delay time (CONT, INH to OUT)

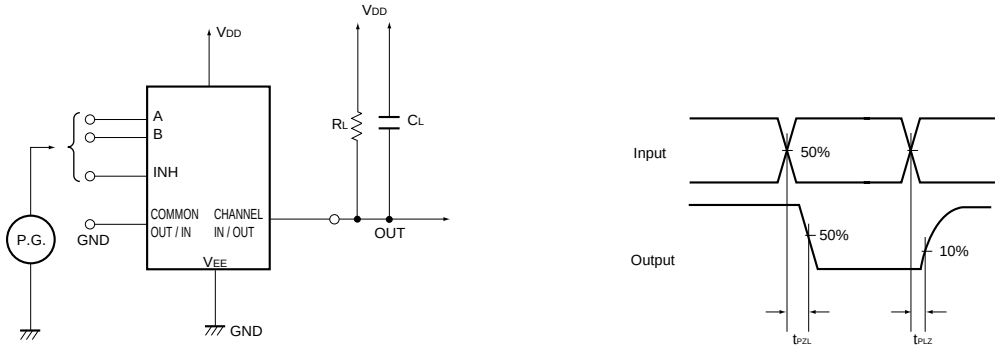


Fig.6 Propagation delay time (CONT, INH to OUT)

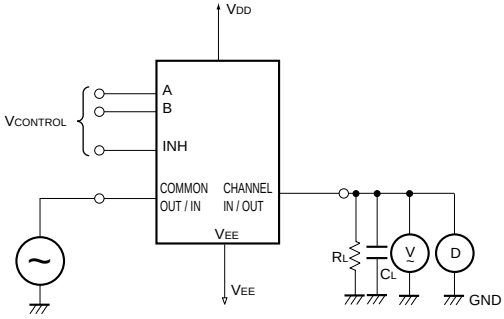


Fig.7 Maximum propagation frequency, feedthrough, sine wave distortion

●Electrical characteristic curve

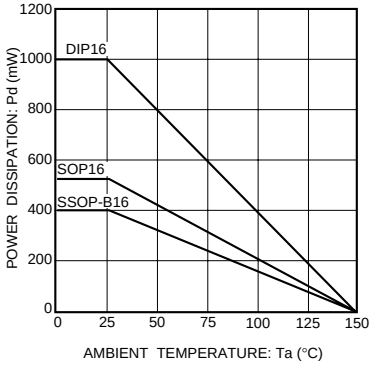
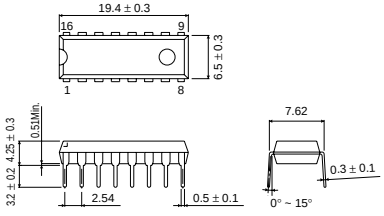


Fig.8 Power dissipation vs. Ta characteristic

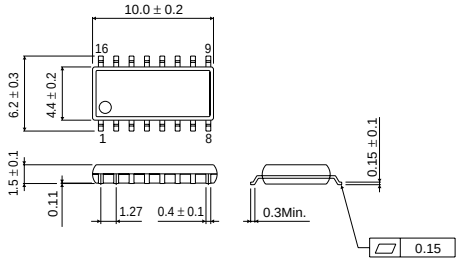
●External dimensions (Units: mm)

BU4052BC



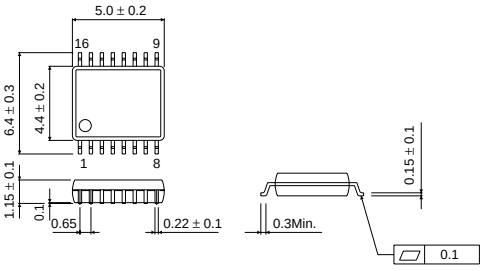
DIP16

BU4052BCF



SOP16

BU4052BCFV



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