

QMOS 8 x 8 x 1 Crosspoint Switches with Memory Control

The CD74HC22106 is a digitally controlled analog switch which utilize silicon-gate CMOS technology. The CD74HC22106 features CMOS input-voltage-level compatibility.

The Master Reset has an internal pull-up resistor and is normally used with a 0.1 μ F capacitor. During power up all switches are automatically reset. The crosspoint switches will reset with MR = 0 even if CE is high. A 6-bit address through a 6 line to 64 line decoder selects the transmission gate which can be turned on by applying a logic ONE to the DATA input and logic ZERO to the STROBE. Similarly, any transmission gate can be turned OFF by applying a logic ZERO to the DATA input while strobing the STROBE with a logic ZERO.

The CE pin allows the crosspoint array to be cascaded for matrix expansion in both the X and Y directions.

Ordering Information

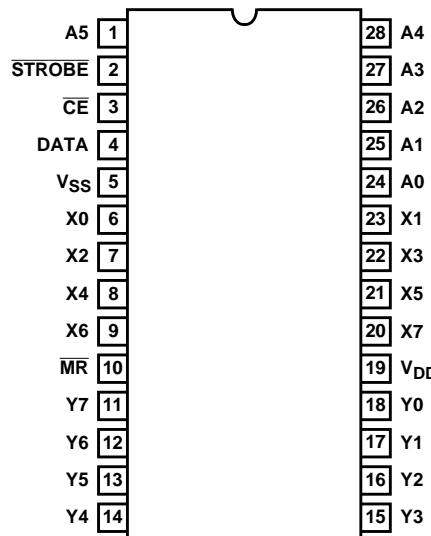
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC22106E	-40 to 85	28 Ld PDIP	E28.6

Features

- 64 Analog Switches in an 8 x 8 x 1 Array
- On-Chip Line Decoder and Control Latches
- Automatic Power-Up Reset by Using a 0.1 μ F Capacitor at the MR Pin
- R_{ON} Resistance 95 Ω at V_{CC} = 4.5V
- Analog Signal Capability: V_{DD}/2
- Wide Operating Temp. Range: -40°C to 85°C
- 2V to 10V Operation
- High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{DD}; at V_{DD} = 5V and 10V

Pinout

CD74HC22106
(PDIP)
TOP VIEW



Absolute Maximum Ratings

DC Supply Voltage (V_{DD})							
Voltage Reference to V_{SS} Terminal	-0.5V to 11V						
DC Input Diode Current							
I_{IK} (for $V_I < -0.5$ or $V_I > V_{DD}$ 0.5V)	$\pm 20\text{mA}$						
DC Output Diode Current							
I_{OK} (For $V_O < -0.5$ or $V_O > V_{DD}$ 0.5V)	$\pm 20\text{mA}$						
DC Transmission Gate Current	$\pm 25\text{mA}$						
Power Dissipation per Package (P_D)							
For $T_A = -40^\circ\text{C}$ to 60°C (Package Type E)	500mW						
For $T_A = -60^\circ\text{C}$ to 85°C (Package Type E)	Derate Linearly at $12\text{mW}/^\circ\text{C}$ to 200mW						

Thermal Information

Maximum Junction Temperature	175°C
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C $\leq T_A \leq$ 150°C
Maximum Lead Temperature (Soldering 10s)	300°C

Operating Conditions

Temperature Range (T_A)	
Package Type E	-40°C to 85°C
Supply Voltage Range (for $T_A = \text{Full Package Temp. Range}$) V_{DD}	
CD74HC22106	2V to 10V
DC Input or Output Voltage V_I, V_O	0V to V_{DD}

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{SS} = \text{GND}$

PARAMETER	TEST CONDITIONS		25°C			-40°C TO 85°C		UNITS
	V_{IS} (V)	V_{DD} (V)	MIN	TYP	MAX	MIN	MAX	
STATIC SPECIFICATIONS								
High-Level Input Voltage, V_{IH}	-	2	1.5	-	-	1.5	-	V
	-	4.5	3.15	-	-	3.5	-	
	-	9	6.3	-	-	6.3	-	
Low-Level Input Voltage, V_{IL}	-	2	-	-	0.5	-	0.5	V
	-	4.5	-	-	1.35	-	1.35	
	-	9	-	-	2.7	-	2.7	
Input Leakage Current (Any Control), I_L	V_{DD} or GND	10	-	-	± 0.1	-	± 1	μA
Quiescent Device Current, I_{CC} (with $\overline{MR} = 1$)	V_{DD} or GND	10	-	-	5	-	50	μA
Off Leakage Current, I_L (with $\overline{MR} = 1$)	All Switches OFF	10	-	-	0.1	-	1	μA
“On” Resistance, R_{ON}	V_{DD} to GND Figures 7, 8	2	-	470	700	-	875	Ω
		4.5	-	64	95	-	120	
		9	-	45	70	-	90	
	$V_{DD}/2$	-	-	-	-	-	-	Ω
		4.5	-	58	85	-	110	
		9	-	40	60	-	80	
“On” Resistance Between Any Two Channels ΔR_{ON}	V_{DD} to GND	-	-	-	-	-	-	Ω
		4.5	-	25	-	-	-	
		9	-	23	-	-	-	

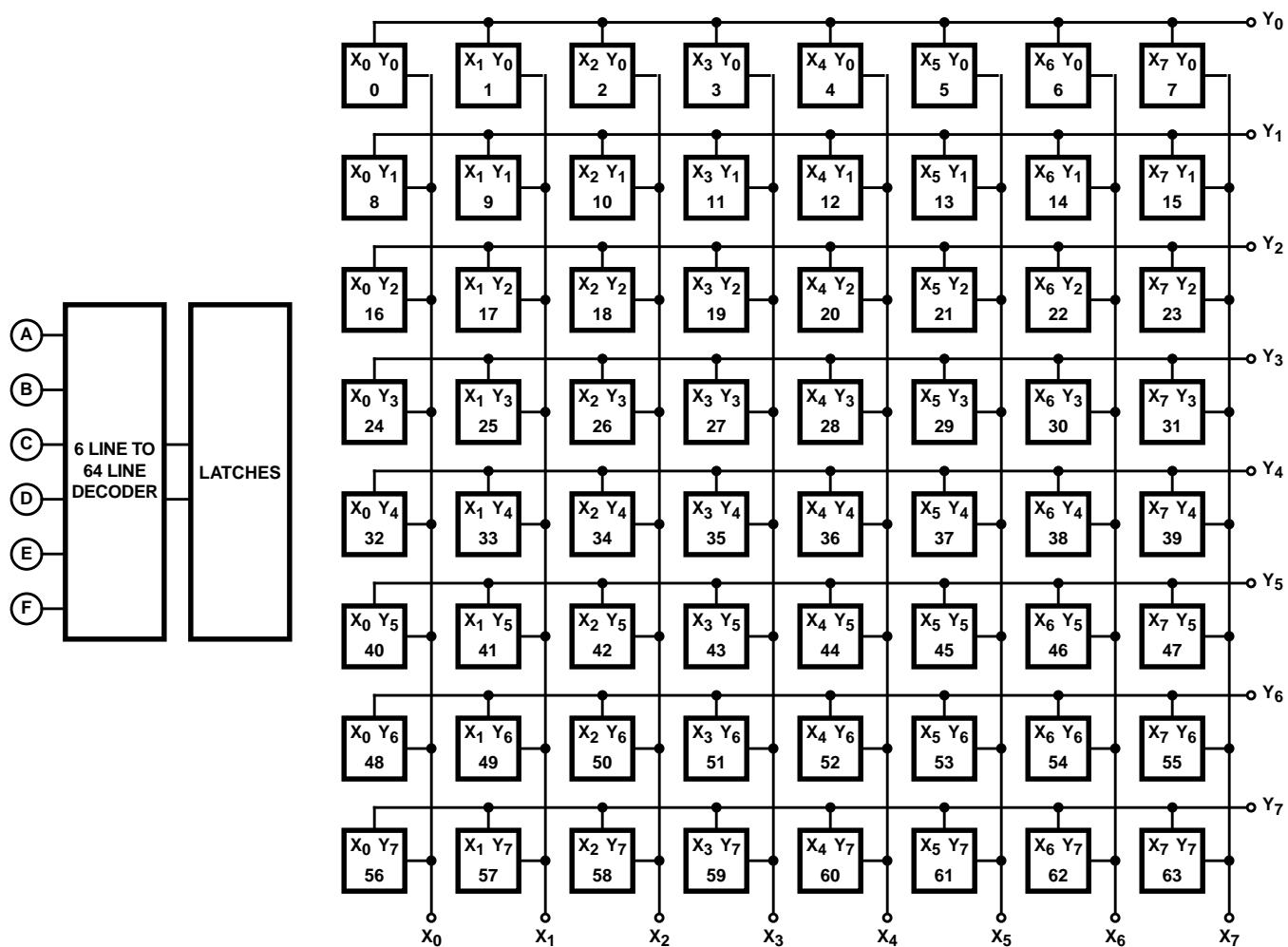
CD74HC22106

Electrical Specifications $V_{SS} = 0V$

PARAMETER	SYMBOL	TEST CONDITIONS			25°C		-40°C TO 85°C		UNITS
			FIG.	V_{DD} (V)	MIN	MAX	MIN	MAX	
DYNAMIC CONTROLS									
Propagation Delay Time:	t_{PZH}	$R_L = 10k\Omega$ $C_L = 50pF$ $t_R, t_F = 6ns$	1	2	-	370	-	385	ns
Strobe to Output (Switch Turn-On to High Level)				4.5	-	110	-	125	ns
				9	-	65	-	70	ns
Data-In to Output (Turn-On to High Level)			2	2	-	240	-	255	ns
				4.5	-	75	-	85	ns
				9	-	50	-	55	ns
Address to Output (Turn-On to High Level)			3	2	-	380	-	400	ns
				4.5	-	110	-	125	ns
				9	-	65	-	75	ns
Propagation Delay Time:	t_{PHZ}		1	2	-	400	-	420	ns
Strobe to Output Switch Turn-Off				4.5	-	135	-	155	ns
				9	-	90	-	100	ns
Data-In to Output (Turn-On to Low Level)			2	2	-	240	-	255	ns
				4.5	-	75	-	85	ns
				9	-	50	-	55	ns
Address to Output (Turn-Off)			3	2	-	420	-	440	ns
				4.5	-	140	-	155	ns
				9	-	95	-	100	ns
Minimum Setup Time (Data-In to Strobe, Address to Strobe)	t_{SU}		-	2	35	-	40	-	ns
				4.5	20	-	20	-	ns
				9	15	-	15	-	ns
Minimum Hold Time (Data-In to Strobe, Address to Strobe)	t_H		-	2	85	-	90	-	ns
				4.5	25	-	25	-	ns
				9	20	-	20	-	ns
Minimum Strobe Pulse Width	t_W		-	2	200	-	210	-	ns
				4.5	45	-	55	-	ns
				9	25	-	30	-	ns
Maximum Switching Frequency	F_O		-	2	0.7	-	0.6	-	MHz
				4.5	3.0	-	2.8	-	MHz
				9	7	-	6.5	-	MHz
Input (Control) Capacitance	C_I		-	-	-	10	-	10	pF

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	V _{IS} (V _{P-P})	V _{SS} (V)	V _{DD} (V)	25°C		-40°C TO 85°C		UNITS
						MIN	MAX	MIN	MAX	
DYNAMIC SPECIFICATIONS										
Propagation Delay Time, Signal Input to Output	t _{PLH} , t _{PHL}	R _L = 10kΩ C _L = 50pF t _R , t _F = 6ns	-	0	2	-	30	-	33	ns
			-	0	4.5	-	20	-	22	ns
			-	-	9	-	15	-	17	ns
						Typical				
Switch Frequency Response at -3dB	f _{3dB}	R _S = R _L = 600Ω	2	-2.25	2.25	5		-	-	MHz
			2	-4.5	4.5	6		-	-	MHz
Crosstalk Between Any Two Channels	F _{CT}	R _S = R _L = 600Ω f = 1kHz	2	-2.25	2.25	-110		-	-	dB
			2	-2.25	2.25	-53		-	-	dB
		R _S = R _L = 600Ω f = 1MHz	2	-4.5	4.5	-55		-	-	dB
Switch "OFF" -40dB Feed Through Frequency	F _{DT}	R _S = R _L = 600Ω	2	-2.25	2.25	7		-	-	MHz
			2	-4.5	4.5	8		-	-	MHz
Total Harmonic Distortion	THD	R _L = 10kΩ f = 1kHz sinewave	4	-2.25	2.25	0.05		-	-	%
			8	-4.5	4.5	0.05		-	-	%
		R _L = 600Ω f = 1kHz sinewave	4	-2.25	2.25	0.25		-	-	%
			7	-4.5	4.5	0.12		-	-	%
Control to Switch FeedThrough Noise (DATA IN, Strobe, Address)		R _L = 10kΩ t _R , t _F = 6ns	V _{DD}	0	5	35		-	-	mV
			V _{DD}	0	10	65		-	-	mV
Capacitance,	C _{IS}									
Xn to GND		f = 1MHz	-	0	10	48		-	-	pF
Yn to GND			-	0	10	44		-	-	pF

Functional Diagram

TRUTH TABLE

A₅	A₄	A₃	A₂	A₁	A₀	SWITCH SELECT	A₅	A₄	A₃	A₂	A₁	A₀	SWITCH SELECT
0	0	0	0	0	0	X ₀ Y ₀	1	0	0	0	0	0	X ₀ Y ₄
0	0	0	0	0	1	X ₁ Y ₀	1	0	0	0	0	1	X ₁ Y ₄
0	0	0	0	1	0	X ₂ Y ₀	1	0	0	0	1	0	X ₂ Y ₄
0	0	0	0	1	1	X ₃ Y ₀	1	0	0	0	1	1	X ₃ Y ₄
0	0	0	1	0	0	X ₄ Y ₀	1	0	0	1	0	0	X ₄ Y ₄
0	0	0	1	0	1	X ₅ Y ₀	1	0	0	1	0	1	X ₅ Y ₄
0	0	0	1	1	0	X ₆ Y ₀	1	0	0	1	1	0	X ₆ Y ₄
0	0	0	1	1	1	X ₇ Y ₀	1	0	0	1	1	1	X ₇ Y ₄
0	0	1	0	0	0	X ₀ Y ₁	1	0	1	0	0	0	X ₀ Y ₅
0	0	1	0	0	1	X ₁ Y ₁	1	0	1	0	0	1	X ₁ Y ₅
0	0	1	0	1	0	X ₂ Y ₁	1	0	1	0	1	0	X ₂ Y ₅
0	0	1	0	1	1	X ₃ Y ₁	1	0	1	0	1	1	X ₃ Y ₅
0	0	1	1	0	0	X ₄ Y ₁	1	0	1	1	0	0	X ₄ Y ₅
0	0	1	1	0	1	X ₅ Y ₁	1	0	1	1	0	1	X ₅ Y ₅
0	0	1	1	1	0	X ₆ Y ₁	1	0	1	1	1	0	X ₆ Y ₅
0	0	1	1	1	1	X ₇ Y ₁	1	0	1	1	1	1	X ₇ Y ₅
0	1	0	0	0	0	X ₀ Y ₂	1	1	0	0	0	0	X ₀ Y ₆
0	1	0	0	0	1	X ₁ Y ₂	1	1	0	0	0	1	X ₁ Y ₆
0	1	0	0	1	0	X ₂ Y ₂	1	1	0	0	1	0	X ₂ Y ₆
0	1	0	0	1	1	X ₃ Y ₂	1	1	0	0	1	1	X ₃ Y ₆
0	1	0	1	0	0	X ₄ Y ₂	1	1	0	1	0	0	X ₄ Y ₆
0	1	0	1	0	1	X ₅ Y ₂	1	1	0	1	0	1	X ₅ Y ₆
0	1	0	1	1	0	X ₆ Y ₂	1	1	0	1	1	0	X ₆ Y ₆
0	1	0	1	1	1	X ₇ Y ₂	1	1	0	1	1	1	X ₇ Y ₆
0	1	1	0	0	0	X ₀ Y ₃	1	1	1	0	0	0	X ₀ Y ₇
0	1	1	0	0	1	X ₁ Y ₃	1	1	1	0	0	1	X ₁ Y ₇
0	1	1	0	1	0	X ₂ Y ₃	1	1	1	0	1	0	X ₂ Y ₇
0	1	1	0	1	1	X ₃ Y ₃	1	1	1	0	1	1	X ₃ Y ₇
0	1	1	1	0	0	X ₄ Y ₃	1	1	1	1	0	0	X ₄ Y ₇
0	1	1	1	0	1	X ₅ Y ₃	1	1	1	1	0	1	X ₅ Y ₇
0	1	1	1	1	0	X ₆ Y ₃	1	1	1	1	1	0	X ₆ Y ₇
0	1	1	1	1	1	X ₇ Y ₃	1	1	1	1	1	1	X ₇ Y ₇

Test Circuits and Waveforms

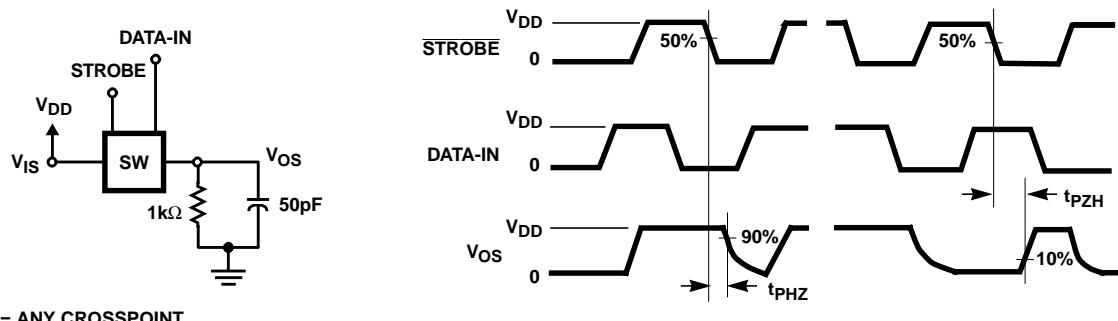


FIGURE 1. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (STROBE TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

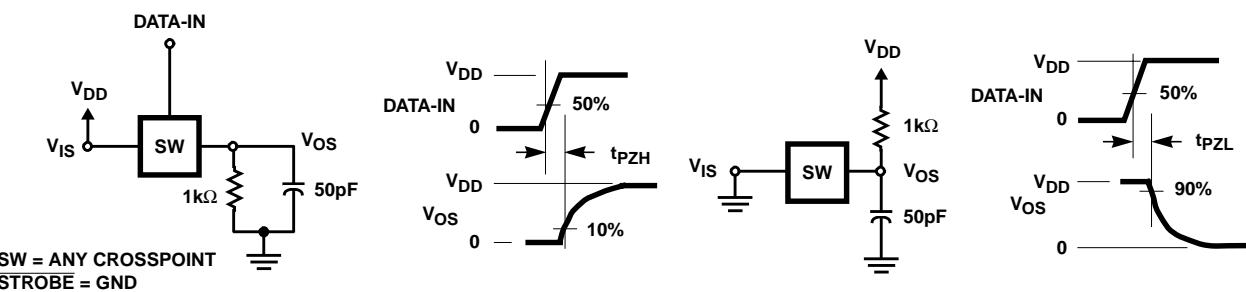


FIGURE 2. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (DATA-IN TO SIGNAL OUTPUT, SWITCH TURN-ON TO HIGH OR LOW LEVEL)

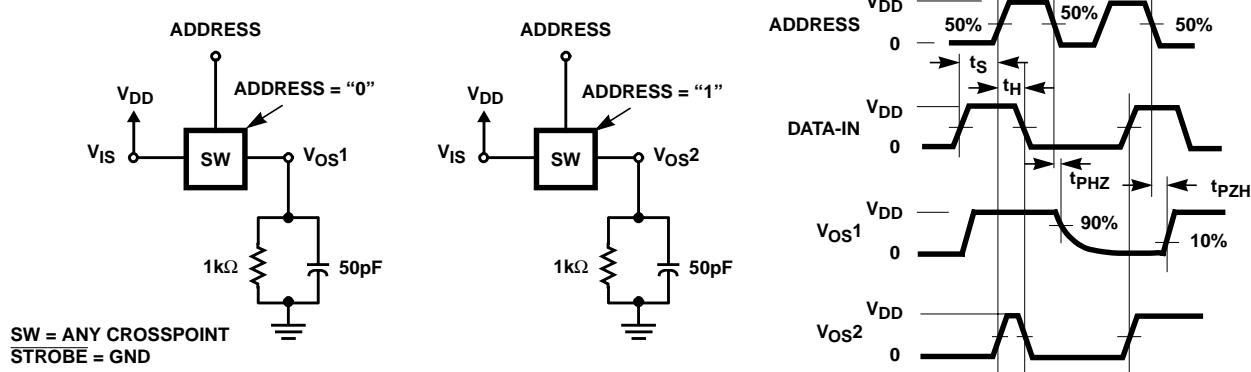


FIGURE 3. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (ADDRESS TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

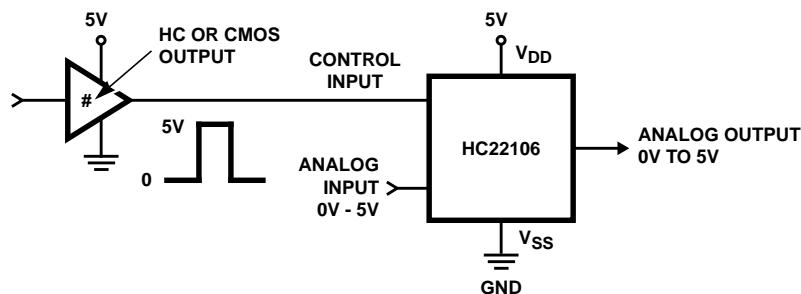
Typical Application Information

FIGURE 4. TYPICAL SINGLE SUPPLY CONNECTION FOR HC22106

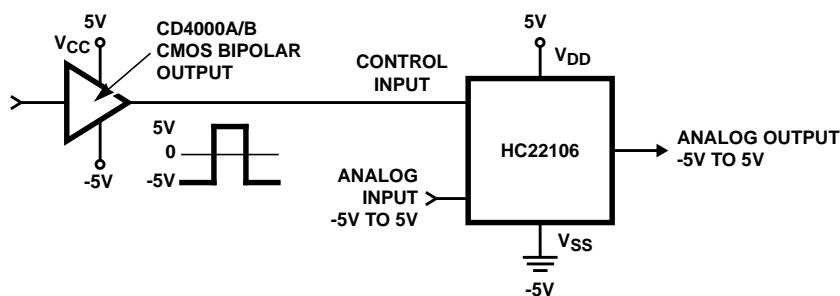


FIGURE 5. TYPICAL DUAL SUPPLY CONNECTION FOR HC22106

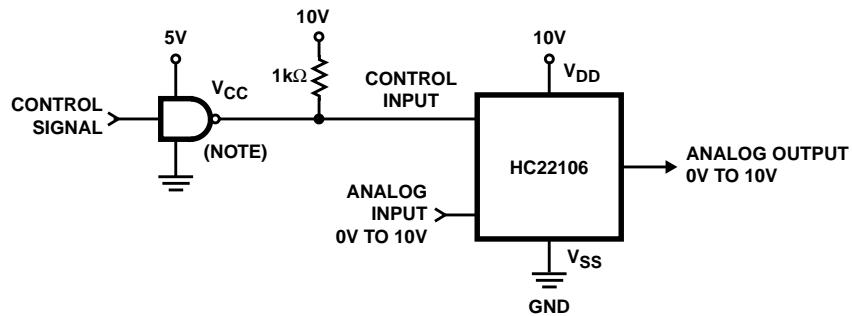


FIGURE 6. USE OF HC22106 WHEN CONTROL IS 0V TO 5V AND ANALOG SIGNAL IS 0V TO 10V

Typical Performance Curves

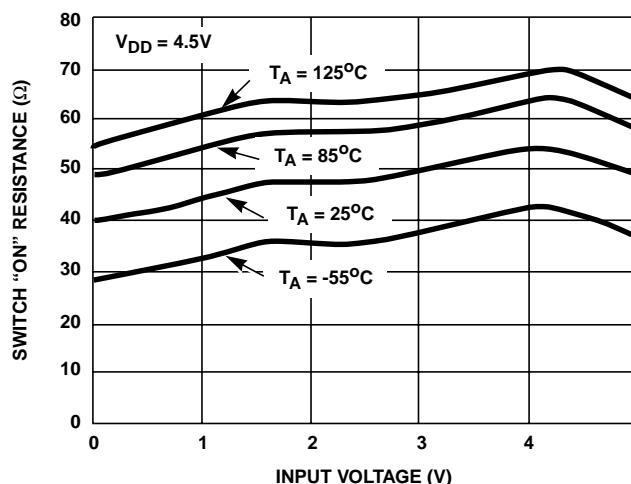


FIGURE 7. TYPICAL "ON" RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE vs TEMPERATURE

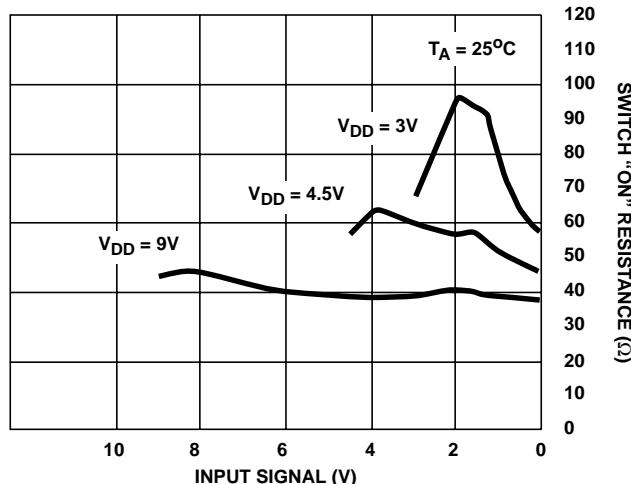


FIGURE 8. TYPICAL "ON" RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE vs V_{DD}

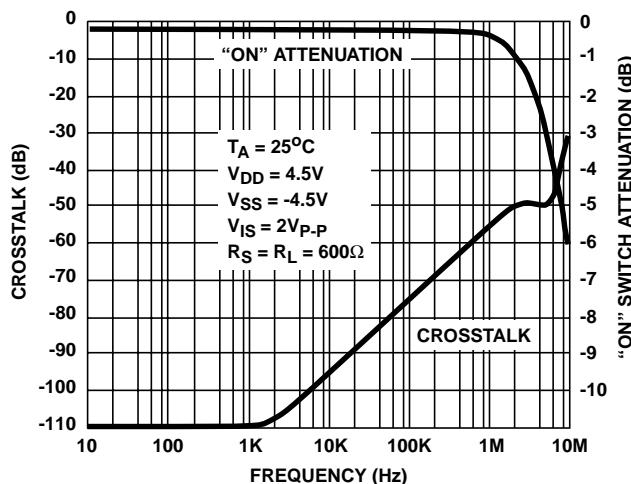


FIGURE 9. TYPICAL "ON" SWITCH ATTENUATION AND CROSSTALK AS A FUNCTION OF FREQUENCY

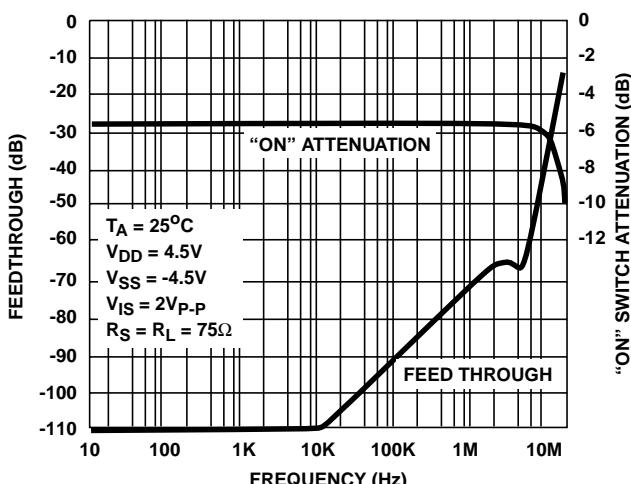


FIGURE 10. TYPICAL "ON" SWITCH ATTENUATION AND "OFF" SWITCH FEED THROUGH AS A FUNCTION OF FREQUENCY

All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusée
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029