SONY

CXD2064Q

Digital Comb Filter (NTSC/PAL)

Description

The CXD2064Q is an adaptive intra-field comb filter compatible with NTSC and PAL systems, and can provide high-precision Y/C separation with a single chip.

Features

- Adaptive intra-field Y/C separation
- M-PAL and N-PAL supported
- Vertical enhancer
- Horizontal aperture correction
- 8-bit A/D converter (1-channel)
- 8-bit D/A converter (2-channel)
- 4× PLL
- Sync tip clamp
- Four 1H delay lines

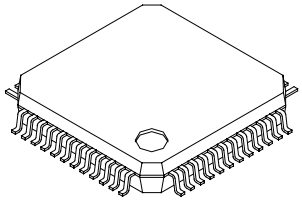
Applications

Y/C separation for color TVs and VCRs

Structure

Silicon gate CMOS ICStructure

48 pin QFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0V)

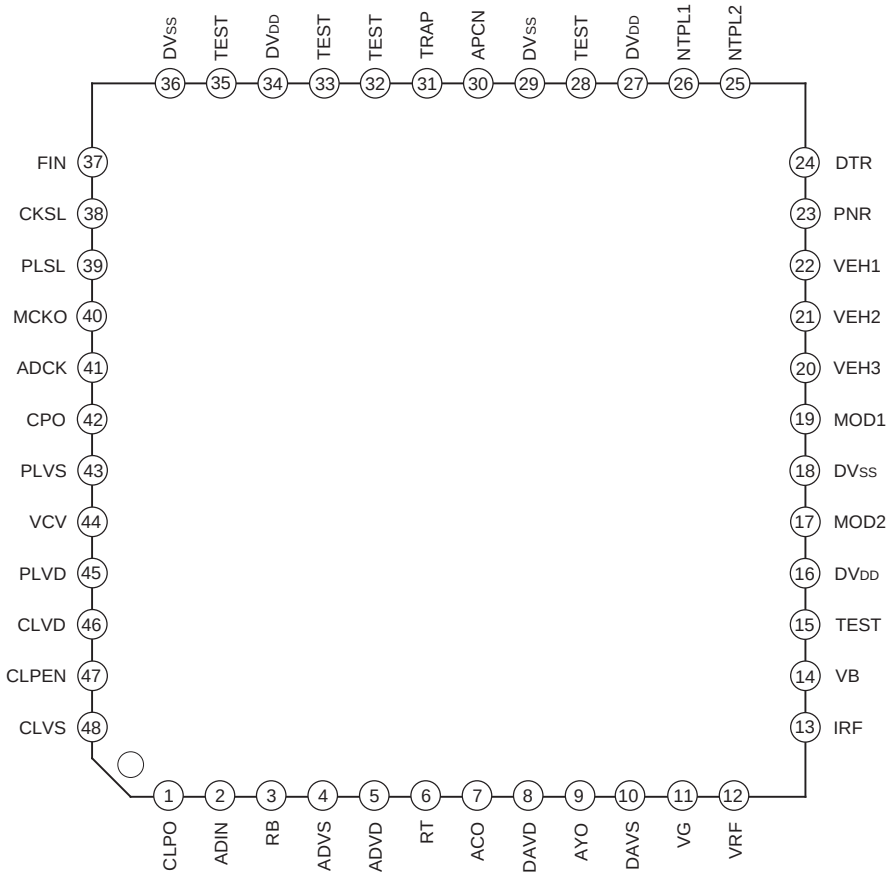
• Supply voltage	DV_{DD}	V_{SS} – 0.5 to +7.0	V
	DAVD	V_{SS} – 0.5 to +7.0	V
	ADVD	V_{SS} – 0.5 to +7.0	V
	PLVD	V_{SS} – 0.5 to +7.0	V
	CLVD	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Storage temperature			
	Tstg	–55 to +150	°C

Recommended Operating Conditions

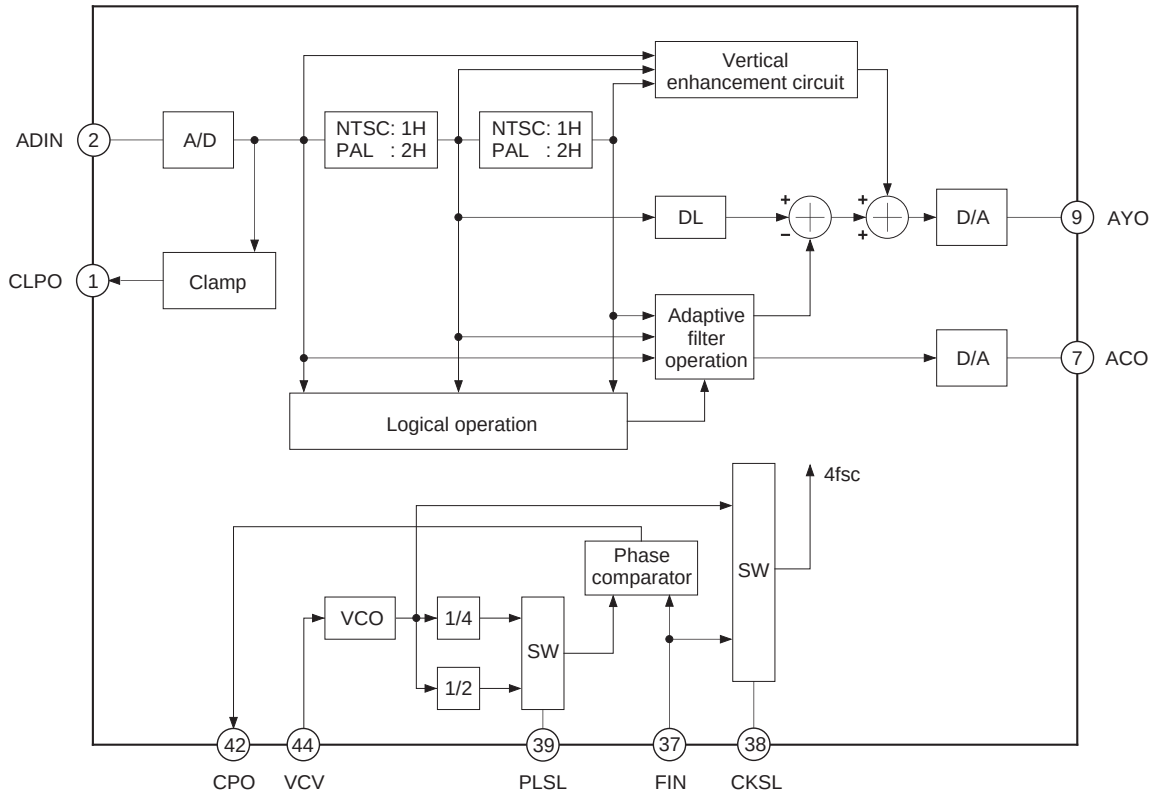
• Supply voltage	DV_{DD}	5.0 ± 0.25	V
	DAVD	5.0 ± 0.25	V
	ADVD	5.0 ± 0.25	V
	PLVD	5.0 ± 0.25	V
	CLVD	5.0 ± 0.25	V
• Analog input	ADIN	1.75	Vp-p
• Operating temperature			
	Topr	–20 to +70	°C

E96X19B91-PS

Pin Configuration



Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	CLPO	O	Internal clamp circuit current output. Connect to ADIN when using the internal clamp. Leave this pin open when not in use.
2	ADIN	I	Comb filter analog input (A/D converter input).
3	RB	O	Reference bottom voltage for the A/D converter (0.52V typ.).
4	ADVS	—	A/D converter analog ground.
5	ADVD	—	A/D converter analog power supply. (5.0V)
6	RT	O	Reference top voltage for the A/D converter (2.60V typ.).
7	ACO	O	Analog chroma signal output. Output can be obtained by connecting a resistor between this pin and the analog ground.
8	DAVD	—	D/A converter analog power supply. (5.0V)
9	AYO	O	Analog luminance signal output. Output can be obtained by connecting a resistor between this pin and the analog ground.
10	DAVS	—	D/A converter analog ground.
11	VG	O	D/A converter related pin. Connect a capacitor of approximately 0.1µF between this pin and the analog power supply (DAVD).
12	VRF	I	Sets the full-scale value of the Y and C-channel D/A converter output signal.
13	IRF	O	Connect a resistor of “16R” (16 times the output resistor “R” of the D/A converter).
14	VB	O	D/A converter related pin. Connect to the analog ground (DAVS) via a capacitor of approximately 0.1µF.
15	TEST	I	Test pin. Normally fix to “Low”.
16	DV_{DD}	—	Digital power supply. (5.0V)
18	DV_{SS}	—	Digital ground.
17	MOD2	I	Y/C separation mode setting. MOD2 / MOD1 L / L: Adaptive processing mode H / L: BPF separation mode H / H: Through mode
19	MOD1	I	
20	VEH3	I	Vertical enhancement setting. Can be set in 8 stages from VEH3 VEH2 VEH1: LLL (off) to HHH (max.)
21	VEH2	I	
22	VEH1	I	
23	PNR	I	L: NTSC/H: PAL, M-PAL, N-PAL
24	DTR	I	Normally fix to “Low”.
25	NTPL2	I	NTSC/PAL/M-PAL/N-PAL mode setting. NTPL2 / NTPL1 L / L: NTSC L / H: PAL H / L: M-PAL H / H: N-PAL
26	NTPL1	I	
27	DV_{DD}	—	Digital power supply. (5.0V)

Pin No.	Symbol	I/O	Description
28	TEST	I	Test pin. Normally fix to “Low”.
29	DV_{SS}	—	Digital ground.
30	APCN	I	Horizontal aperture correction circuit setting. Low: Off, High: On.
31	TRAP	I	Trap filter setting. Low: Off, High: On.
32	TEST	I	Test pin. Normally open or fix to “Low”.
33	TEST	I	Test pin. Normally open or fix to “Low”.
34	DV_{DD}	—	Digital power supply. (5.0V)
35	TEST	I	Test pin. Normally open or fix to “Low”.
36	DV_{SS}	—	Digital ground.
37	FIN	I	Clock input. Input the burst-locked fsc (2fsc) when using the internal PLL. Input the burst-locked 4fsc when not using the internal PLL.
38	CKSL	I	PLL control. Low: The internal PLL is not used. The clock (4fsc) which is input to FIN is supplied internally. High: The internal PLL is used. VCO oscillation output 4fsc clock is supplied internally.
39	PLSL	I	Selects the clock input to FIN. Low: fsc, High: 2fsc. When inputting 4fsc to FIN (when not using the internal PLL), this pin may be set to either “Low” or “High”.
40	MCKO	O	Clock (4fsc) output.
41	ADCK	I	Clock input for A/D converter. Normally connect to MCKO.
42	CPO	O	PLL phase comparator output. Leave open when not using the PLL.
43	PLVS	—	PLL analog ground.
44	VCV	I	VCO control voltage input. Connect to PLVS when not using the PLL.
45	PLVD	—	PLL analog power supply. (5.0V)
46	CLVD	—	Clamp D/A converter analog power supply. (5.0V)
47	CLPEN	I	Clamp circuit enable pin. Low: Clamp on, High: Clamp off.
48	CLVS	—	Clamp D/A converter analog ground.

Electrical Characteristics

DC Characteristics

(V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = –20 to +70°C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit	Applicable pins
Supply voltage	DV_{DD}	—	4.75	5.0	5.25	V	*1
	DAVD						
	ADVD						
	PLVD						
	CLVD						
Operating temperature	Topr	—	–20		+70	°C	
Supply current	I_{DD}	Clock 18MHz	—	90	—	mA	—
Input/output voltage	V_I, V_O	—	Vss		V_{DD}	V	*2
Input voltage	V_{IH}	CMOS level input	$0.7V_{DD}$			V	*3
	V_{IL}				$0.3V_{DD}$		
Input rise/fall time	tr, tf	—	0		500	ns	*1
Output voltage	V_{OH}	I_{OH} = –2mA	V_{DD} – 0.8			V	*4
		I_{OH} = –3mA					*5
	V_{OL}	I_{OL} = 4mA			0.4		*4
		I_{OL} = 1.5mA					*5
Clock input amplitude	V_{IN}	fmax = 50MHz sine wave	0.5			Vp-p	*6
Feedback resistance value	R_{FB}	V_{IN} = Vss or V_{DD}	250k	1M	2.5M	Ω	
Input leak current	I_{IL}, I_{IH}	V_{IN} = Vss or V_{DD}	–10		10	µA	*7
	I_{IH}	V_{IH} = V_{DD}	40	100	240		*8
Clock amplifier output delay	—	—	3.0	9.0	18.0	ns	*9

*1 All pins
*2 All pins other than *6
*3 All input pins other than *6
*4 All output pins other than *5
*5 CPO (Pin 42)
*6 FIN (Pin 37)
*7 All input pins other than *8
*8 Pins 32, 33 and 35
*9 MCKO (Pin 40)

I/O Pin Capacitance

(Ta = 25°C, f = 1MHz, V_{IN} = V_{OUT} = 0V)

Item	Symbol	Min.	Min.	Max.	Unit
Input pin capacitance	C_{IN}	—	—	9	pF
Output pin capacitance	C_{OUT}	—	—	11	

Internal 8-bit A/D Converter Characteristics

(V_{DD} = 5V, Ta = 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	fmax		18	—	—	MSPS
Analog input bandwidth	BW	–3dB	—	18	—	MHz
Self bias	VRB		0.48	0.52	0.56	V
	VRT – VRB		1.96	2.08	2.22	V
Output data delay	tpd		—	—	45	ns
Differential linearity error	E_D		–1.0	—	+1.0	LSB
Integral linearity error	E_L		–2.0	—	+2.0	LSB

Internal 8-bit D/A Converter Characteristics

(V_{DD} = 5V, V_{RF} = 2V, R_{IRF} = 3.3kΩ, R = 200Ω, Ta = 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	fmax		18	—	—	MSPS
Differential linearity error	E_D		–0.8	—	+0.8	LSB
Integral linearity error	E_L		–2.0	—	+2.0	LSB
Output full-scale voltage	V_{FS}		1.805	1.90	1.995	V
Output full-scale current	I_{FS}		—	9.5	15	mA
Output offset voltage	V_{OS}		—	—	1.0	mV
Glitch energy	G_E	R = 75Ω, 1Vp-p output	—	30	—	pV-s

Internal Clamp

(V_{DD} = 5V, Ta = 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clamp level *1	CLV		—	0.67	—	V

*1 Sync tip clamp

Description of Functions

• Y/C separation mode

The Y/C separation mode can be switched by the following pin settings.

Mode name	MOD2 (Pin 17)	MOD1 (Pin 19)
Adaptive processing mode	L	L
BPF separation mode	H	L
Through mode	H	H

Adaptive processing mode:

Y/C separation is performed by detecting the correlation between three lines and switching between comb filter and BPF processing.

BPF separation mode:

Y/C separation is performed only by BPF processing.

Through mode:

The composite video signal input from ADIN (Pin 2) is A/D converted and then D/A converted without modification. D/A outputs are AYO (Pin 9) and ACO (Pin 7).

• Horizontal aperture correction circuit

This circuit corrects the frequency response degradation caused by the aperture effects accompanying D/A conversion. This circuit is valid in the adaptive processing and BPF separation modes noted above.

• Trap filter circuit

A trap filter is applied to remove the frequency components near fsc in the luminance signal after Y/C separation.

This reduces the fsc frequency component gain by approximately 2.5dB.

This circuit is valid in the adaptive processing and BPF separation modes noted above.

• Using the internal PLL (clock selection method)

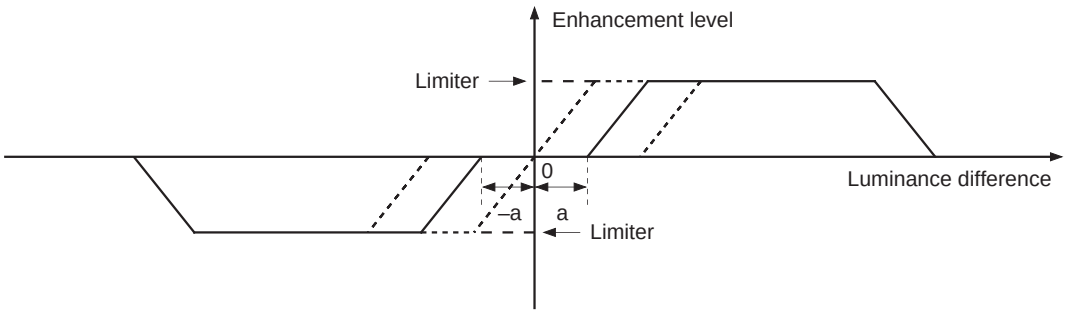
	FIN (Pin 37)	CKSL (Pin 38)	PLSL (Pin 39)
PLL used	fsc input	H	L
	2fsc input	H	H
PLL not used	4fsc input	L	L/H

• Vertical enhancement circuit

This circuit generates an enhanced component in accordance with the vertical aperture component (luminance difference from the preceding and following lines) of the luminance signal. The vertical aperture of the picture can be enhanced naturally by adding this enhanced component to the luminance signal after Y/C separation.

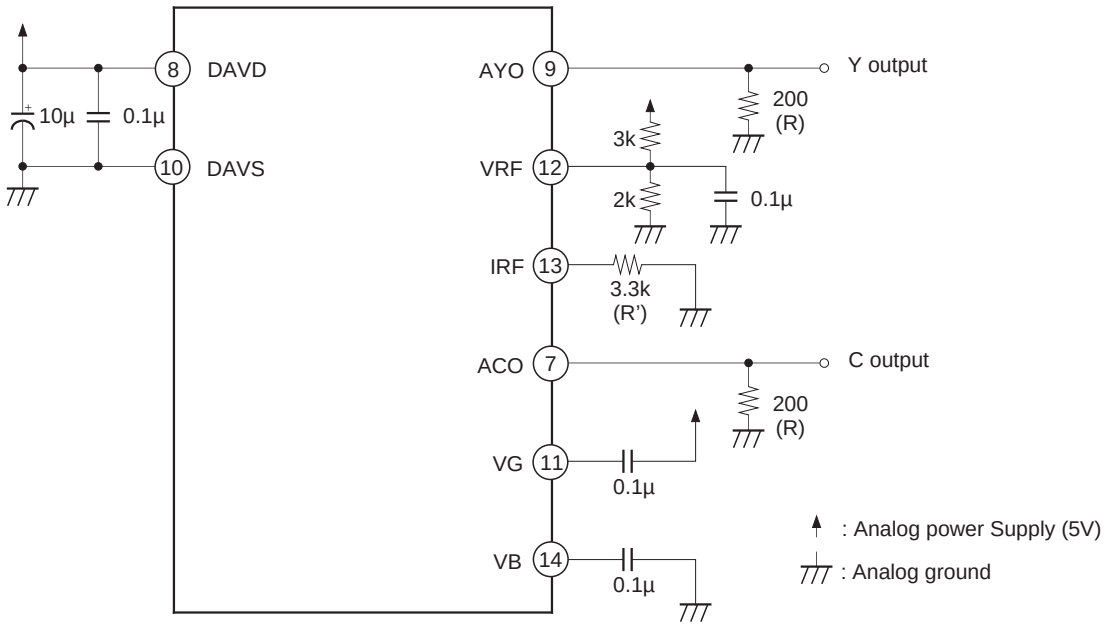
The enhancement level can be set in eight steps. The size of | a | in the figure below varies according to the pin settings. Accordingly,enhanced level can be changed for portions of natural pictures with small luminance differences where the effects are particularly easy to see.

Portions with large luminance differences are cut with a limiter so that they are not excessively enhanced. Also, portions with extremely large luminance differences such as white and black lines are not enhanced because they need be enhanced any more.



Enhancement level	Pin settings			| a |
	VEH3 (Pin 20)	VEH2 (Pin 21)	VEH1 (Pin 22)	
OFF	L	L	L	—
1	L	L	H	Large
2	L	H	L	↑
3	L	H	H	
4	H	L	L	
5	H	L	H	
6	H	H	L	↓
Max	H	H	H	Small

Application Circuit for D/A Converter Block



• Method of selecting the output resistor

The CXD2064Q has a built-in current output type D/A converter. To obtain the output voltages, connect resistors to the AYO and ACO pins.

The specs are as follows: output full-scale voltage V_{FS} = 0.5 to 2.0 [V], output full-scale current I_{FS} = 0 to 15 [mA].

Calculate the output resistance value using the relationship $V_{FS} = I_{FS} \times R$. In addition, connect a resistor of 16 times the output resistor to the reference current pin (IRF). In case this results in a unpractical value, use a resistance value as close to the calculated value as possible.

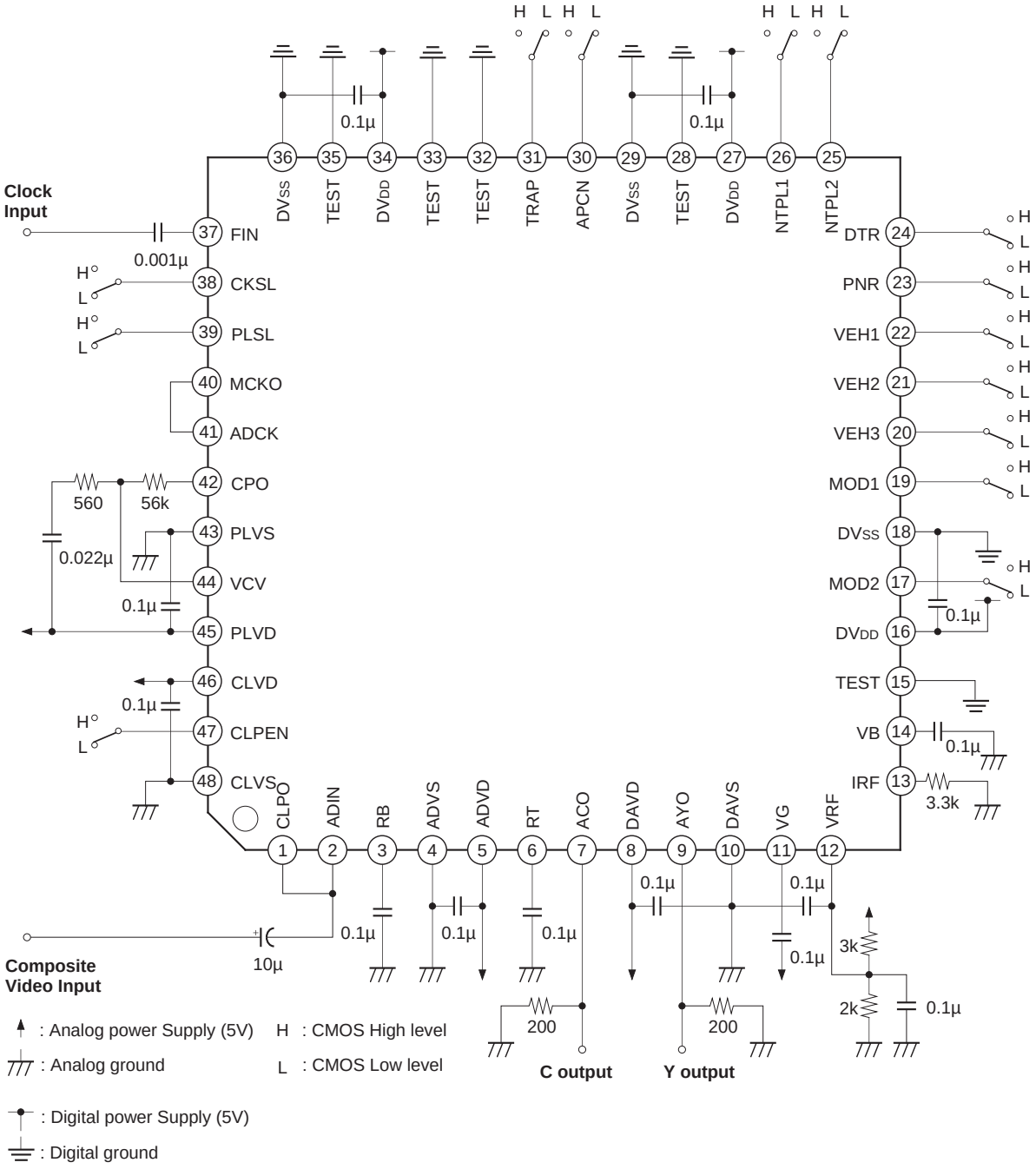
Note that, at this time, $V_{FS} = V_{RF} \times 16R/R'$ (V_{RF}: Pin voltage of V_{RF}). Here, R is the resistor connected to AYO/ACO, and R' is the resistor connected to IRF.

Power consumption can be reduced by using higher resistance values, but the glitch energy and data settling time increase contrastingly. Set the optimum values according to the system applications.

• V_{DD}, V_{SS}

Separate the analog and digital systems around the device to reduce the effects of noise. DAVD is by-passed to DAVS as close to each other as possible through a ceramic capacitor of approximately 0.1µF.

External Connection Diagram



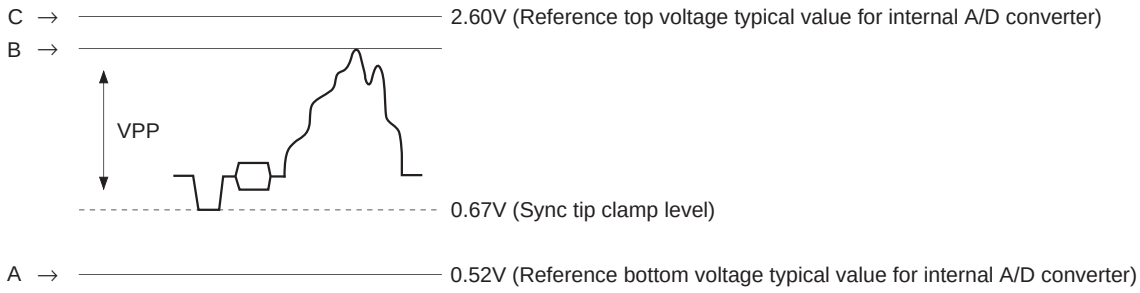
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

- Make the wiring for the signal input to ADIN (Pin 2) as short as possible. Also, drive the input signal to ADIN at low impedance.
- Make the analog and digital power supply and GND lines as wide and short as possible to ensure low impedance.
- Bypass the analog and digital power supply pins to GND with a ceramic capacitor of about 0.1µF connected as close to the pin as possible.
- Input a clock that is locked to the burst signal of the input video signal.
- Separate the wiring to the clock input pin FIN (Pin 37) from the external analog circuits, analog power supplies and analog GND.

- ADIN (analog input signal)

  Set the input signal peak-to-peak value VPP to 1.75V or less. Additionally, VPP is recommended to be 1.3V or more since the A/D converter input dynamic range should be made as large as possible.



  The DC level at the ADIN pin is as shown in the diagram above when the internal sync tip clamp is used.

  Labeling the internal D/A converter AYO output full-scale voltage as VFS, the correspondence between the ADIN pin voltage and AYO output pin voltage (DC level) is as follows;

  DC voltage at point B → AYO maximum output voltage [V]
  DC voltage at point A → 0 [V]
  DC voltage at point C → VFS [V]

  The VFS is the AYO output voltage generated when the voltage equivalent to the point C is input.

- Internal delay

  The delay from the internal A/D converter to the D/A converter output is as follows;

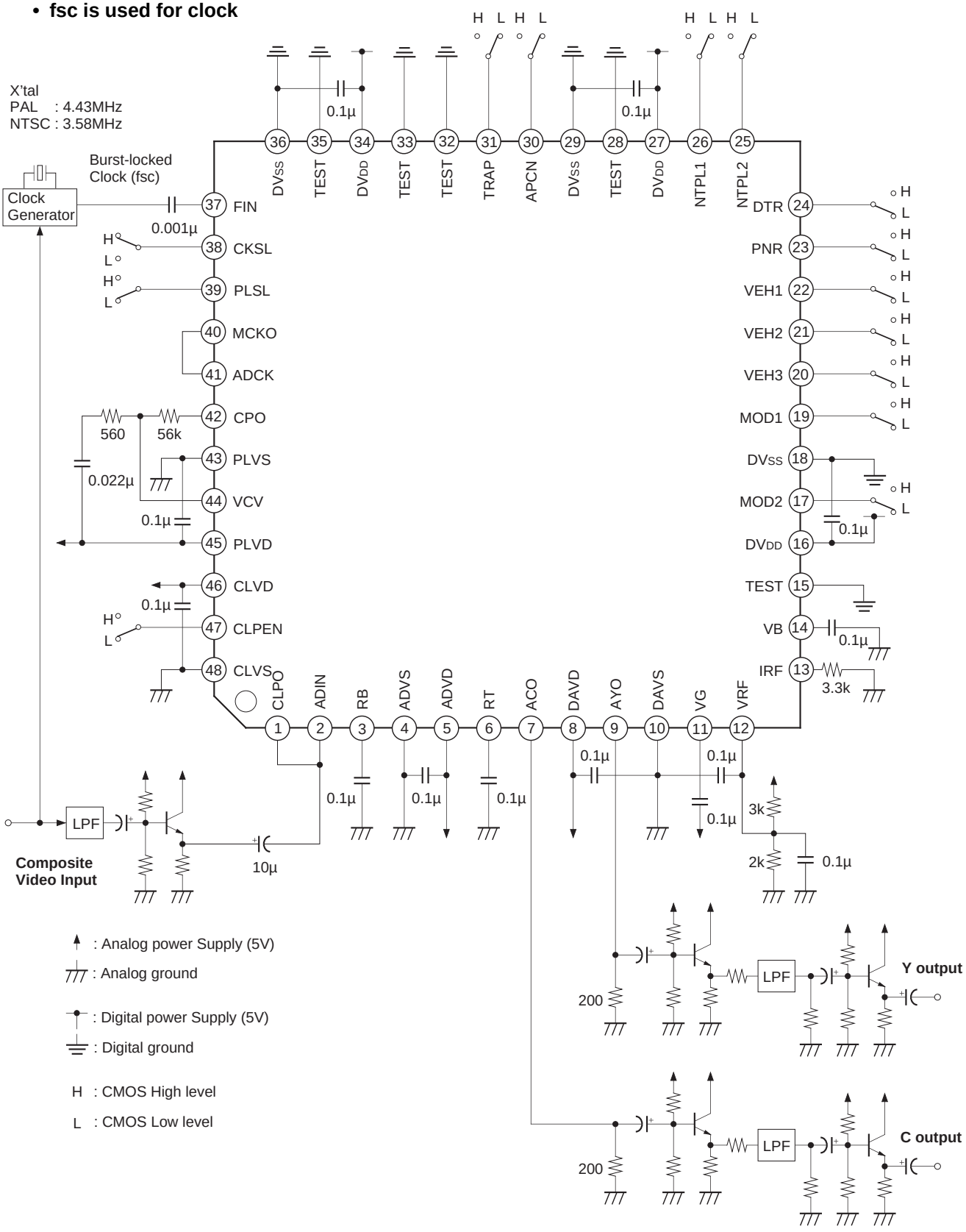
  NTSC: 1H + 24.5 clocks + αns
  PAL: 2H + 24.5 clocks + αns
  (α: D/A converter analog output delay = approximately 20ns)

  The 24.5 clocks are the sum of the clocks shown below;

  A/D converter: 3.5 clocks (“0.5” is for fetching the data at the fall of the clock.)
  Internal logic: 20 clocks
  D/A converter: 1 clock

Application Circuit 1

- **fsc is used for clock**



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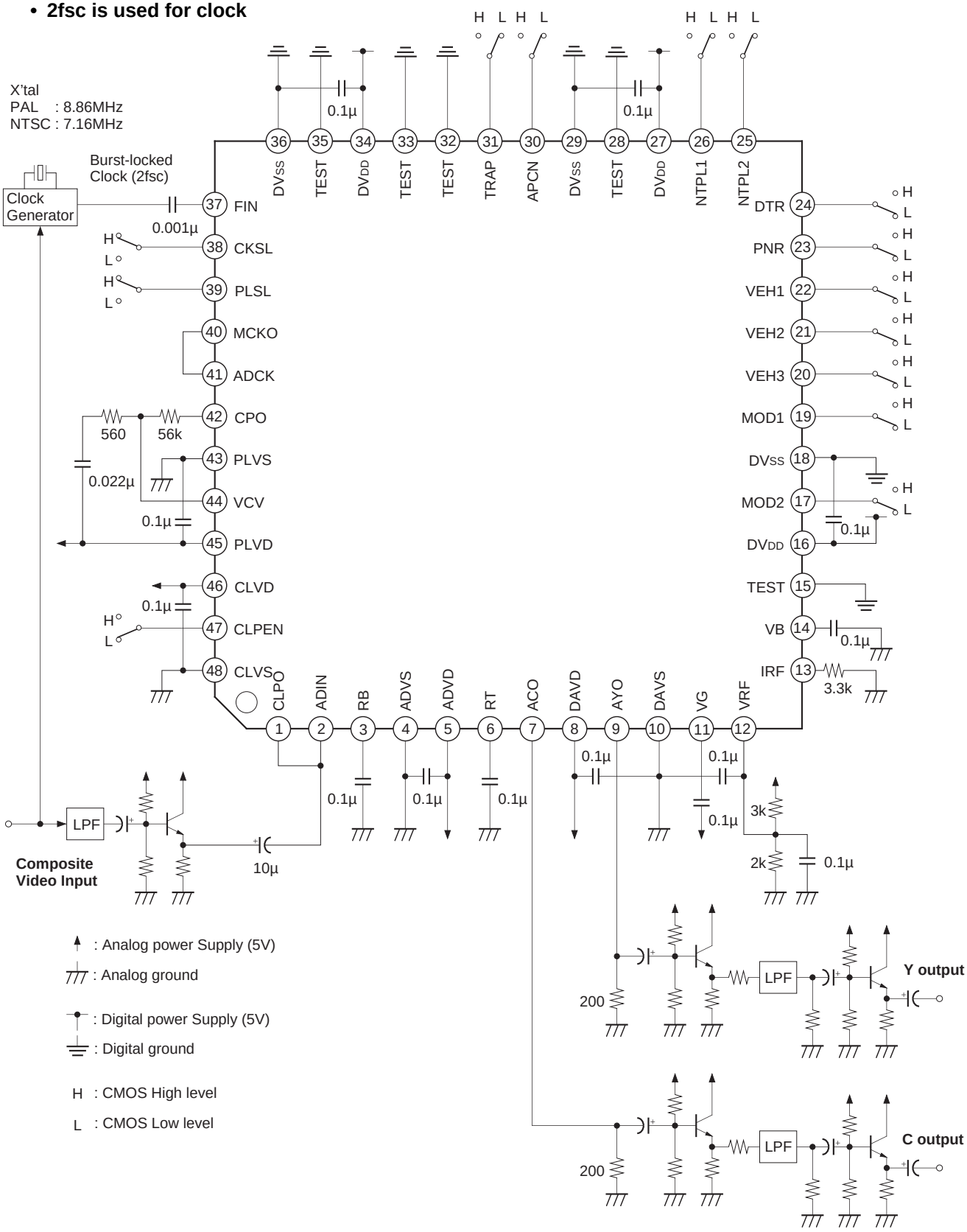
Application Circuit 2

- **2fsc is used for clock**



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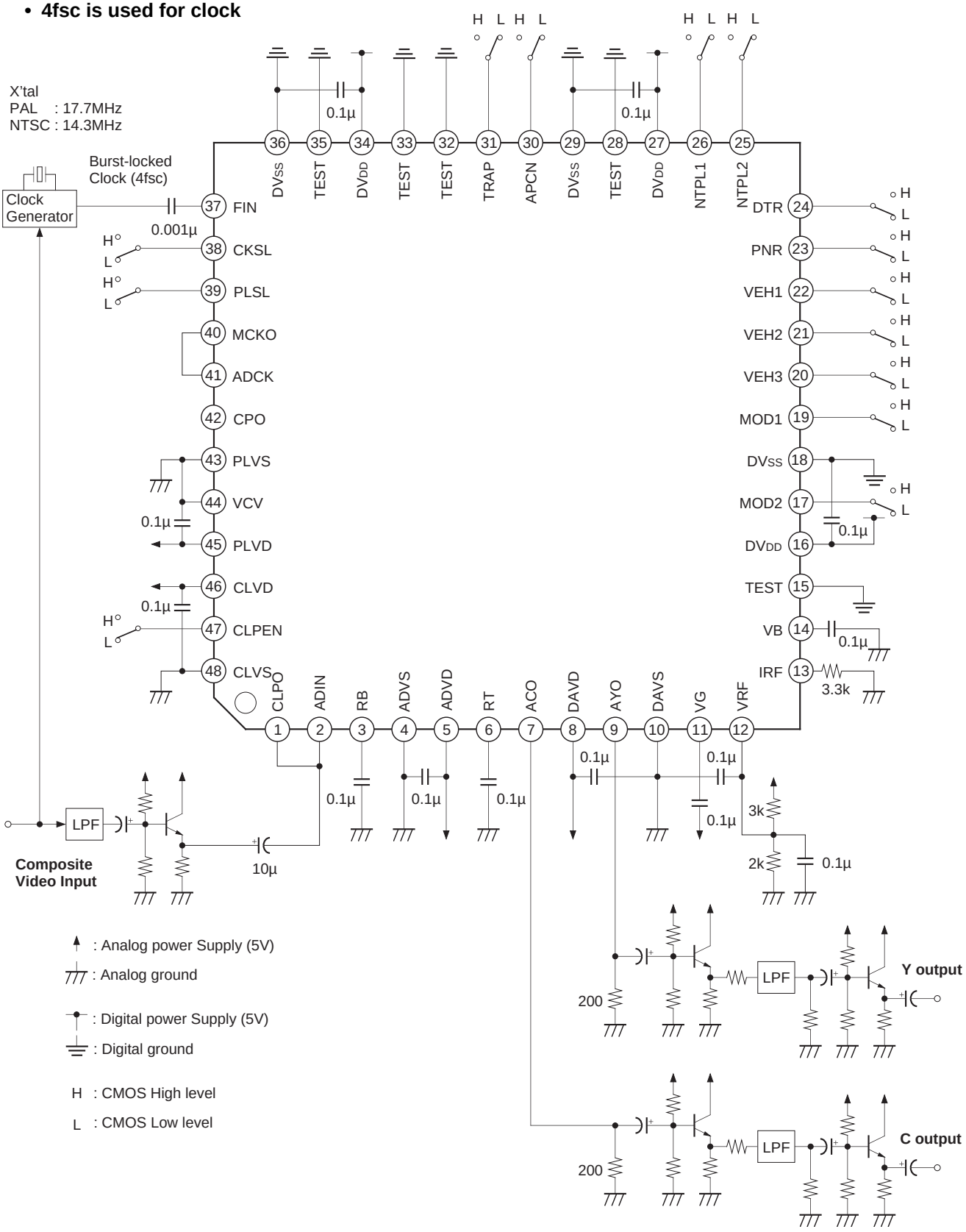
Application Circuit 3

- **4fsc is used for clock**



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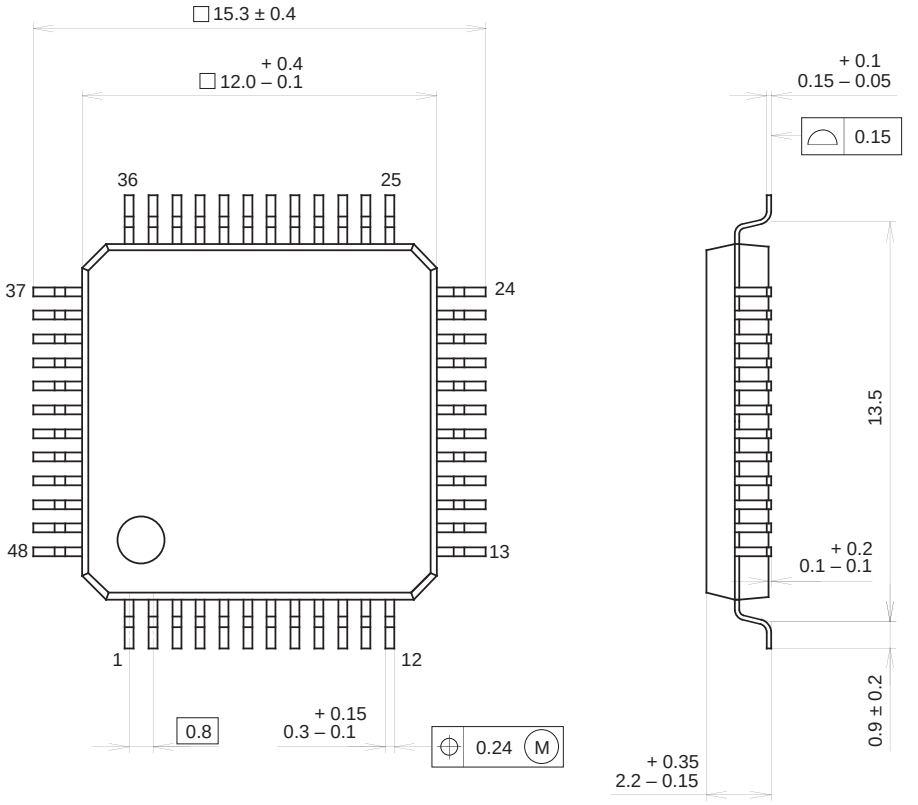
Package Outline Unit : mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	QFP048-P-1212
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.7g