

## CMOS-CCD Signal Processor

### Description

The CXL1502M is a CMOS-CCD signal processor designed for 8-mm video signal processing. In combination with the 8-mm video Y/C signal processing IC CXA1200Q, this IC configures a comb filter for Y/C separation in recording an image, elimination of line crawling and crosstalk in playing back.

### Features

- Single power supply 5V
- Low power consumption
- Built-in peripheral circuits
- Completely adjustment free
- Built-in triple progression PLL circuit
- For PAL signals

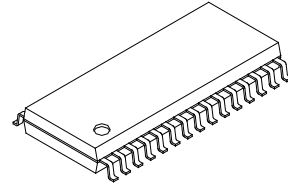
### Functions

- 1H comb filter, 2H comb filter output
- Dropout compensation
- PLL circuit (triple progression)
- Clock driver
- Autobias circuit
- Sync tip clamp circuit
- Sample and hold circuit
- Delay time matching through output (THR)

### Structure

CMOS-CCD

30 pin SOP (Plastic)



### Absolute Maximum Ratings (Ta = 25°C)

- |                               |                  |             |    |
|-------------------------------|------------------|-------------|----|
| • Supply voltage              | V <sub>DD</sub>  | 6           | V  |
| • Operating temperature       | T <sub>opr</sub> | -10 to +60  | °C |
| • Storage temperature         | T <sub>stg</sub> | -55 to +150 | °C |
| • Allowable power dissipation | P <sub>D</sub>   | 500         | mW |

### Recommended Operating Conditions (Ta = 25°C)

- |                |                 |        |   |
|----------------|-----------------|--------|---|
| Supply voltage | V <sub>DD</sub> | 5 ± 5% | V |
|----------------|-----------------|--------|---|

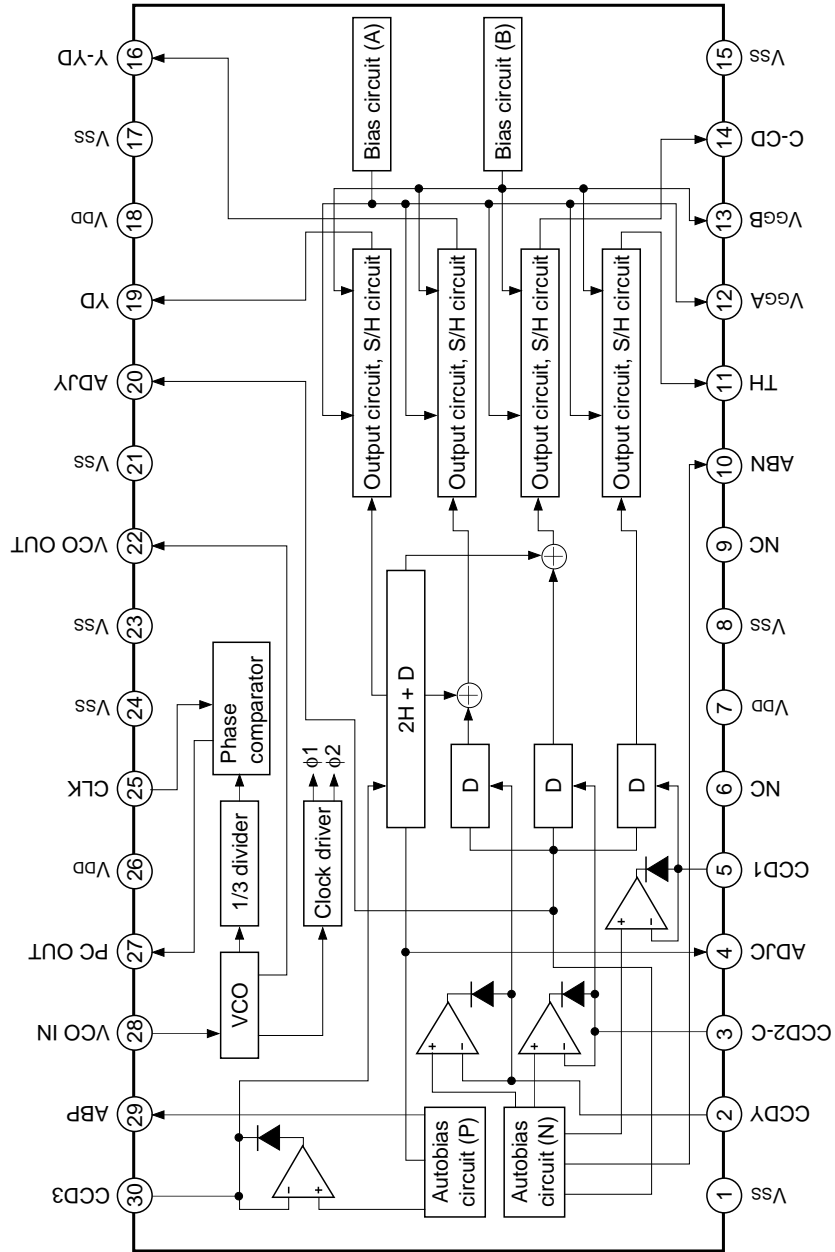
### Recommended Clock Conditions (Ta = 25°C)

- |                         |                  |   |
|-------------------------|------------------|---|
| • Input clock amplitude | V <sub>CLK</sub> | 0.3 to 1.0 V <sub>p-p</sub><br>(0.4V <sub>p-p</sub> Typ.) |
| • Clock frequency       | f <sub>CLK</sub> | 4.433619 MHz  |
| • Input clock waveform  |                  | sine wave   |

### Input Signal Amplitude

- |                  |     |                             |
|------------------|-----|-----------------------------|
| V <sub>SIG</sub> | 575 | mV <sub>p-p</sub><br>(Max.) |
|------------------|-----|-----------------------------|

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Block Diagram

## Pin Description

Pin No.	Symbol	I/O	Description	Impedance ( $\Omega$ )
1	V <sub>SS</sub>	—	GND	
2	CCDY	I	Signal input 4 (Reverse phase signal)	> 100k (at no clamp)
3	CCD2-C	I	Signal input 2 (Reverse phase signal)	> 100k (at no clamp)
4	ADJC	O	Forward CCD bias DC output	600 to 2k
5	CCD1	I	Signal input 1 (Reverse phase signal)	> 100k (at no clamp)
6	NC	—		
7	V <sub>DD</sub>	—	5V power supply	
8	V <sub>SS</sub>	—	GND	
9	NC	—		
10	ABN	O	Reverse phase autobias DC output	2k to 200k
11	TH	O	THR signal output (Forward phase signal)	40 to 500
12	V <sub>GG</sub> A	O	Gate bias (A) DC output	2k to 10k
13	V <sub>GG</sub> B	O	Gate bias (B) DC output	2k to 10k
14	C-CD	O	2H comb filter signal output	40 to 500
15	V <sub>SS</sub>	—	GND	
16	Y-YD	O	1H comb filter signal output	40 to 500
17	V <sub>SS</sub>	—	GND	
18	V <sub>DD</sub>	—	5V power supply	
19	YD	O	DOC signal output (Reverse phase signal)	40 to 500
20	ADJY	O	Reverse phase CCD bias DC output	600 to 2k
21	V <sub>SS</sub>	—	GND	
22	VCO OUT	O	VCO output	
23	V <sub>SS</sub>	—	GND	
24	V <sub>SS</sub>	—	GND	
25	CLK	I	Clock input	4k to 40k
26	V <sub>DD</sub>	—	5V power supply	
27	PC OUT	O	Phase comparator output	2k to 5k
28	VCO IN	I	VCO input	> 100k
29	ABP	O	Forward phase autobias DC output	2k to 200k
30	CCD3	I	Signal input 3 (Forward phase signal)	> 100k (at no clamp)





Electrical Characteristics Test Circuit

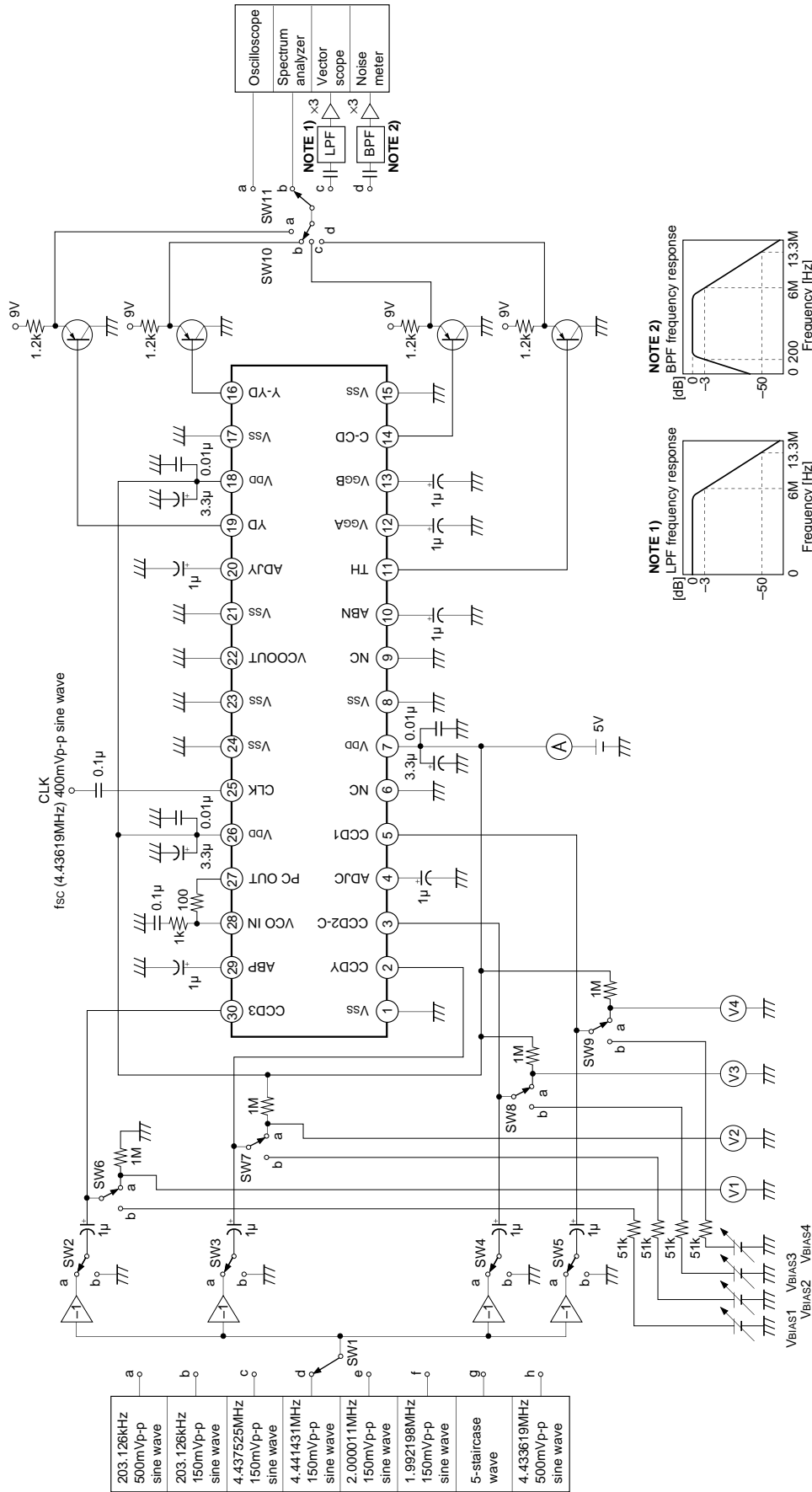


Fig. 1

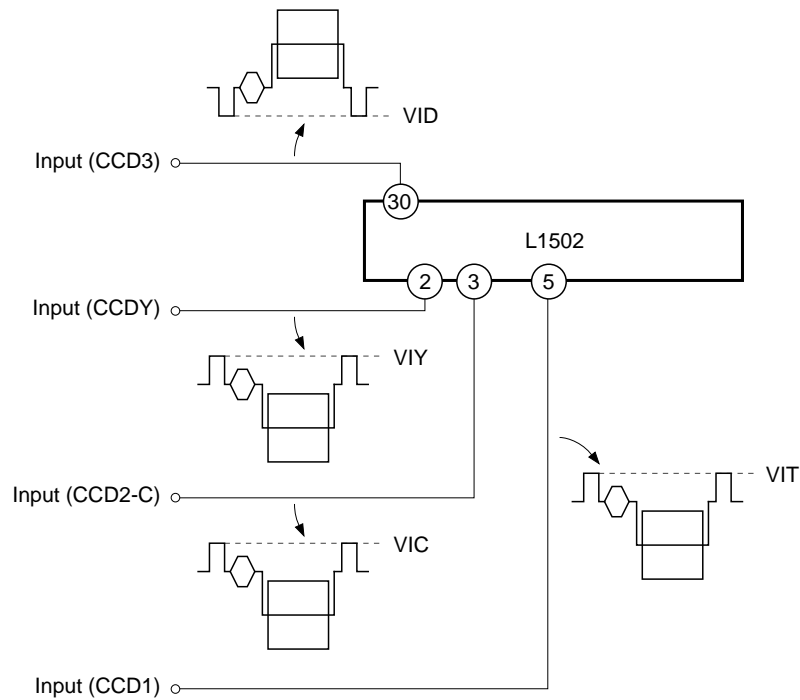
a	203.126kHz
b	500mVp-p
c	sine wave
d	203.126kHz
e	150mVp-p
f	sine wave
g	4.437525MHz
h	150mVp-p
	sine wave
	4.441431MHz
	150mVp-p
	sine wave
	2.000011MHz
	150mVp-p
	sine wave
	1.992198MHz
	150mVp-p
	sine wave
	5-staircase
	wave
	4.433619MHz
	500mVp-p
	sine wave

**Notes)**

\*1 Adjust the output amplitude of the inversion and the non-inversion amplifiers in the signal input block to an equal value, as well as the phase difference to a precise 180°. Also set the clock and input signal frequency accurately.

\*2 VIC, VIY, VID and VIT are defined as follows:

VIC, VIY, VID and VIT are input signal clamp levels. They clamp the Video signal sync tip level. They are the pin voltages at no-input signal for pins 3, 2, 30 and 5, respectively.



Testing of VIC, VIY, VID and VIT is executed with a voltmeter under the following SW conditions:

Item	SW conditions											Test point
	1	2	3	4	5	6	7	8	9	10	11	
VIC	—	b	b	b	b	a	a	a	a	—	—	V3
VIY	—	b	b	b	b	a	a	a	a	—	—	V2
VID	—	b	b	b	b	a	a	a	a	—	—	V1
VIT	—	b	b	b	b	a	a	a	a	—	—	V4

\*3 This is the IC supply current value during clock and signal input.

\*4 GLC, GLY, GLD and GLT are output gains of C-CD, Y-YD, YD and TH pins when a 500mVp-p, 203.126kHz sine wave is simultaneously fed to CCD2-C, CCDY, CCD3 and CCD1 pins, respectively.

(Example of calculation)

$$GLC = 20 \log \frac{\text{C-CD pin output voltage [mVp-p]}}{500 \text{ [mVp-p]}} \text{ [dB]}$$

\*5 GHC, GHY, GHD and GHT are output gains of C-CD, Y-YD, YD and TH pins when a 150mVp-p, 4.437525MHz sine wave is simultaneously fed to CCD2-C, CCDY, CCD3 and CCD1 pins, respectively. Bias at input ( $V_{BIAS1}$ ,  $V_{BIAS2}$ ,  $V_{BIAS3}$  and  $V_{BIAS4}$ ) is tested respectively at  $V_{ID} + 0.25V$ ,  $V_{IY} - 0.25V$ ,  $V_{IC} - 0.25V$  and  $V_{IT} - 0.25V$ .

(Example of calculation)

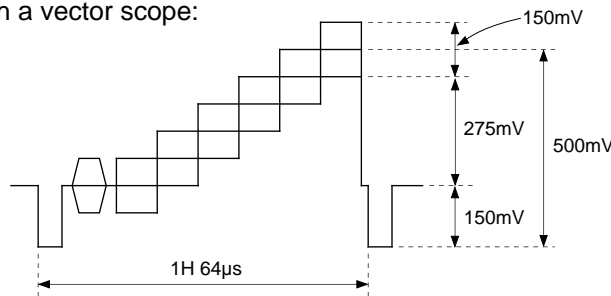
$$GHC = 20 \log \frac{\text{C-CD pin output voltage [mVp-p]}}{150 \text{ [mVp-p]}} \text{ [dB]}$$

\*6 Indicates the dissipation at 4.437525MHz in relation to 203.126kHz. From the output voltage at TH, C-CD, Y-YD and YD pins when a 150mVp-p, 203.126kHz sine wave is simultaneously fed to CCD1, CCD2-C, CCDY and CCD3 pins, and from the output voltage at TH, C-CD, Y-YD and YD pins when a 150mVp-p, 4.437525MHz sine wave is simultaneously fed to same, calculation is made according to the following formula. The input block bias for  $V_{BIAS1}$ ,  $V_{BIAS2}$ ,  $V_{BIAS3}$  and  $V_{BIAS4}$  is tested at  $V_{ID} + 0.25V$ ,  $V_{IY} - 0.25V$ ,  $V_{IC} - 0.25V$  and  $V_{IT} - 0.25V$ , respectively.

(Example of calculation)

$$fT = 20 \log \frac{\text{TH pin output voltage (4.437525MHz) [mVp-p]}}{\text{TH pin output voltage (203.126kHz) [mVp-p]}} \text{ [dB]}$$

\*7 The differential gain (DG) and the differential phase (DP), when the 5-staircase wave in the following figure is fed, are tested with a vector scope:



CCD3 pin input waveform (the input waveform of CCD1, CCD2-C and CCDY pins is the inverted waveform of the figure above.)

\*8 The noise level of output signal at no-input signal is tested with a video noise meter in the Sub Carrier Trap mode at BPF 100kHz to 5MHz.  $V_n$  [Vrms]

The signal component is determined either by testing the output voltage (the same test system as that of noise level) at input of 350mVp-p, 203.126kHz, or by performing calculation from the values of GLT, GLC, GLY and GLD in accordance with the following formula.  $V_s$  [Vp-p]

(Example of  $V_s$  calculation)

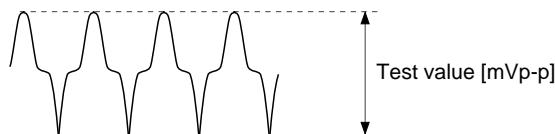
$$V_{S-T} = 0.35 \times 10^{\frac{GLT}{20}} \text{ (} V_{S-T}: \text{ TH output voltage)}$$

(Example of S/N ratio calculation)

$$SNT = 20 \log \frac{V_{N-T} \text{ (noise component) [Vrms]}}{V_{S-T} \text{ (signal component) [Vp-p]}} \text{ [dB]}$$



\*9 The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested. The input block bias for V<sub>BIAS1</sub> is tested at VID + 0.5V and VIC – 0.25V.



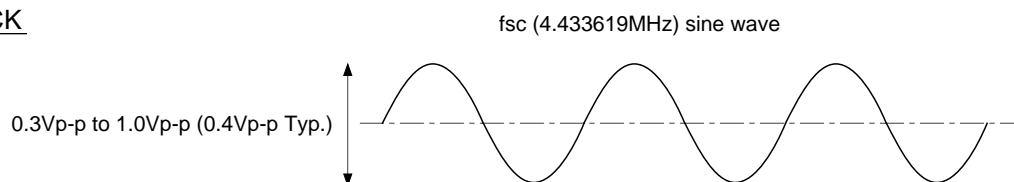
\*10 C-CD is calculated in accordance with the following formula from the C-CD pin output voltage when a 200mVp-p, 4.437525MHz sine wave is simultaneously fed to CCD1, CCD2-C, CCDY and CCD3 pins and from the C-CD pin output voltage when a 200mVp-p, 4.441431MHz sine wave is simultaneously fed to same. The input block bias for V<sub>BIAS1</sub>, V<sub>BIAS2</sub>, V<sub>BIAS3</sub> and V<sub>BIAS4</sub> is set to VID + 0.3V, VIY – 0.3V, VIC – 0.3V and VIT – 0.3V, respectively.

$$C-CD = 20 \log \frac{C-CD \text{ pin output voltage (4.437525MHz)}}{C-CD \text{ pin output voltage (4.441431MHz)}} \text{ [dB]}$$

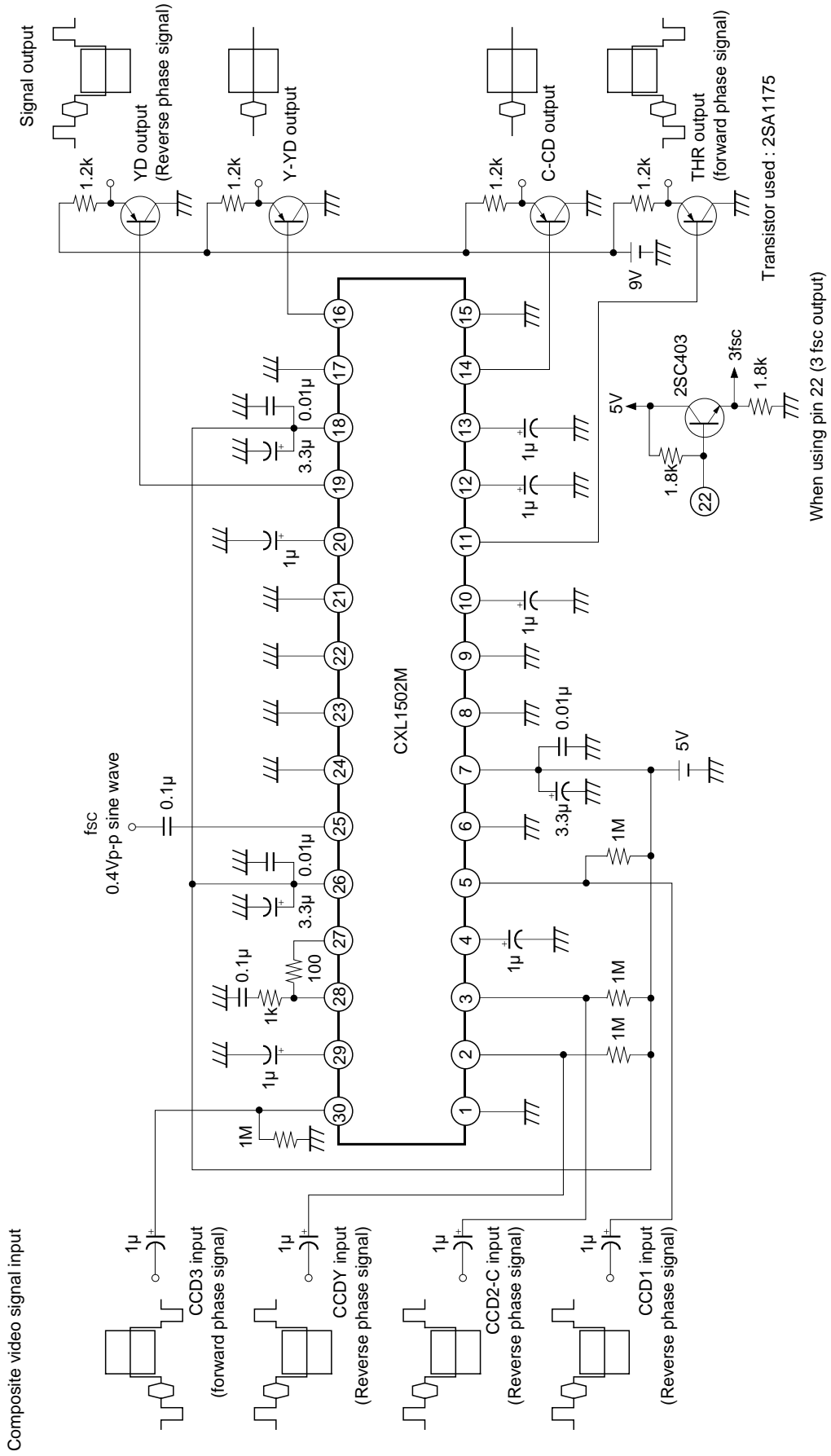
\*11 Y-CD is calculated in accordance with the following formula from the Y-YD pin output voltage when a 200mVp-p, 2.000011MHz sine wave is simultaneously fed to CCD1, CCD2-C, CCDY and CCD3 pins and from the Y-YD pin output voltage when a 200mVp-p, 1.992198MHz sine wave is simultaneously fed to same. The input block bias is set to the same conditions as in testing CCD.

$$Y-CD = 20 \log \frac{Y-YD \text{ pin output voltage (1.992198MHz)}}{Y-YD \text{ pin output voltage (2.000011MHz)}} \text{ [dB]}$$

CLOCK

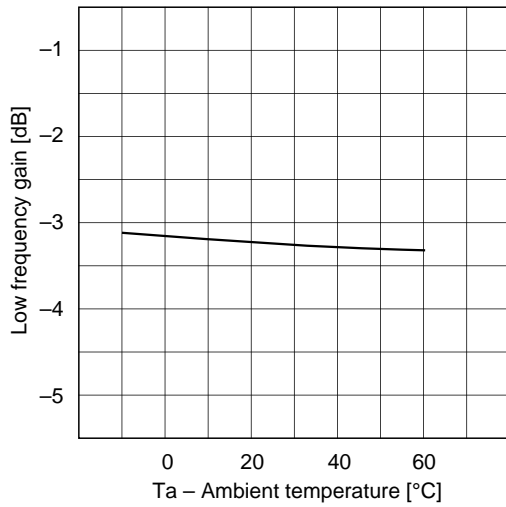


Application Circuit

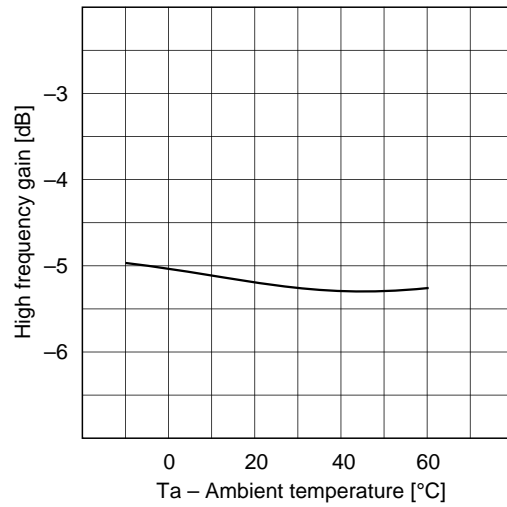


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

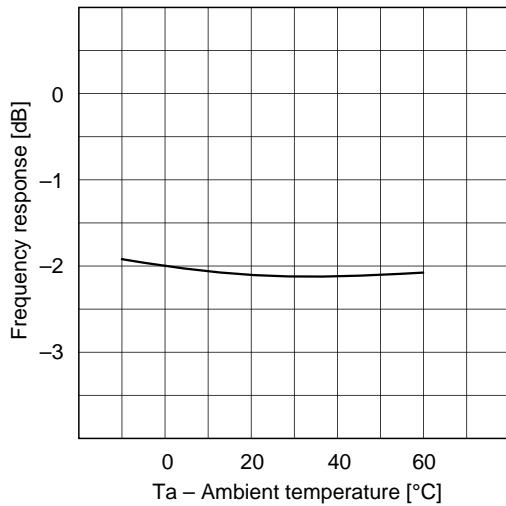
Low frequency gain vs. Ambient temperature



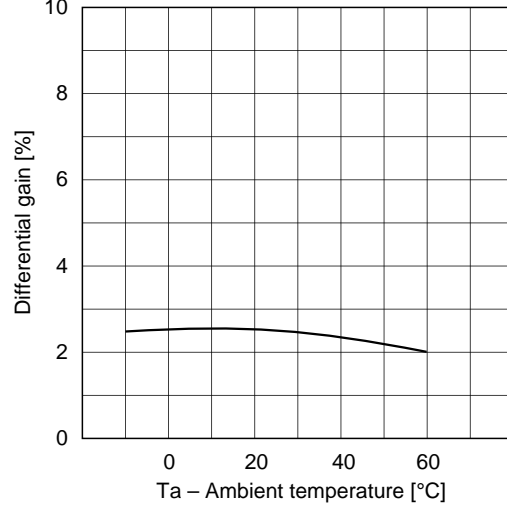
High frequency gain vs. Ambient temperature



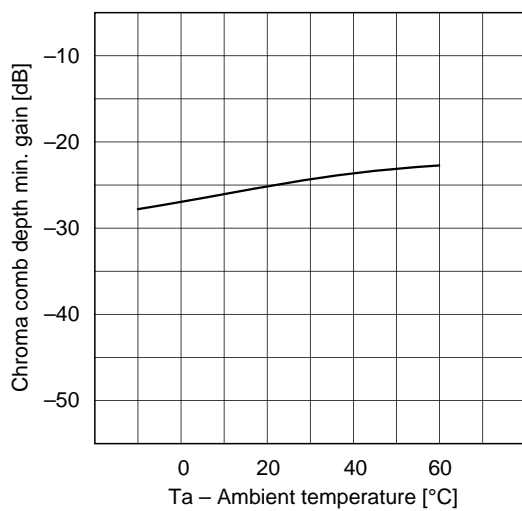
Frequency response vs. Ambient temperature



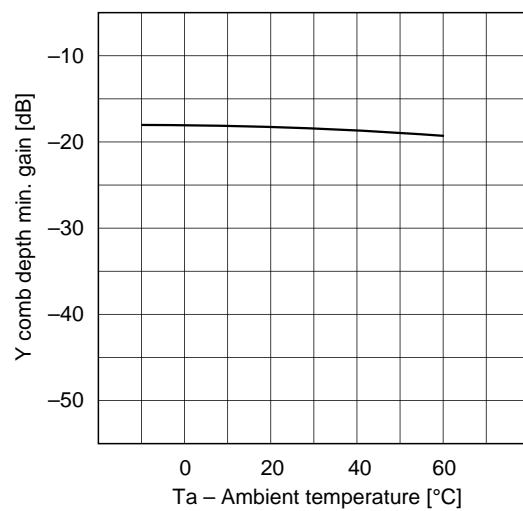
Differential gain vs. Ambient temperature



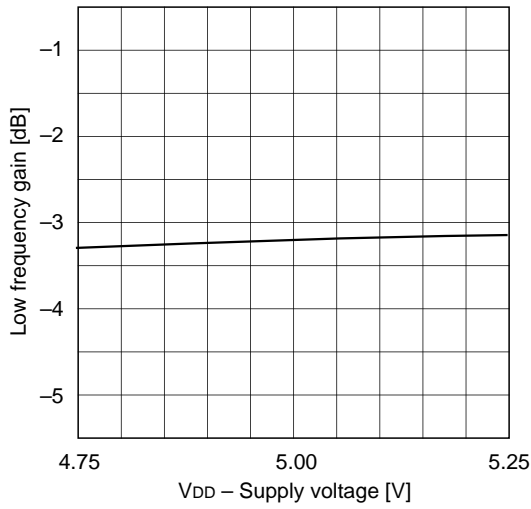
Chroma comb depth min. gain vs. Ambient temperature



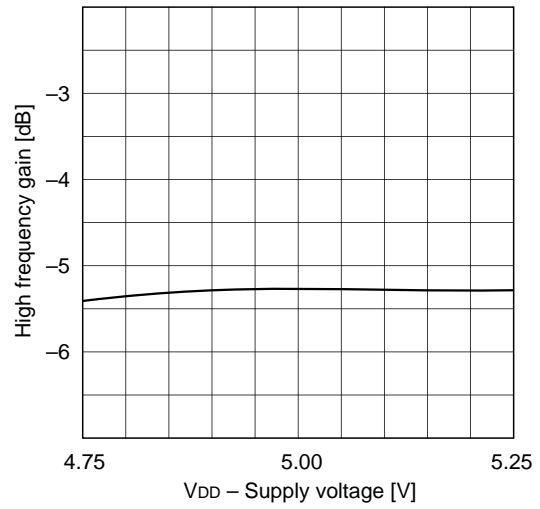
Y comb depth min. gain vs. Ambient temperature



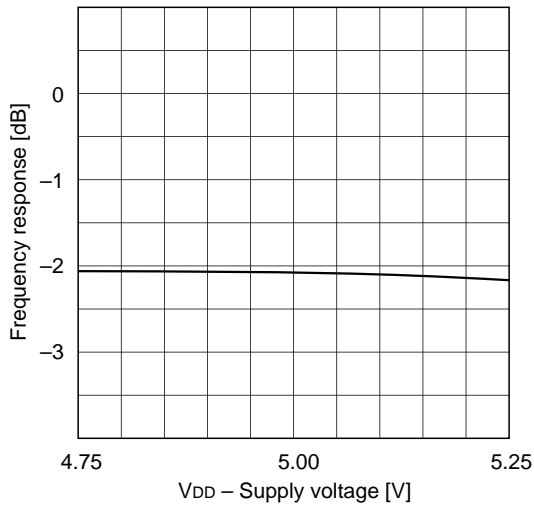
**Low frequency gain vs. Supply voltage**



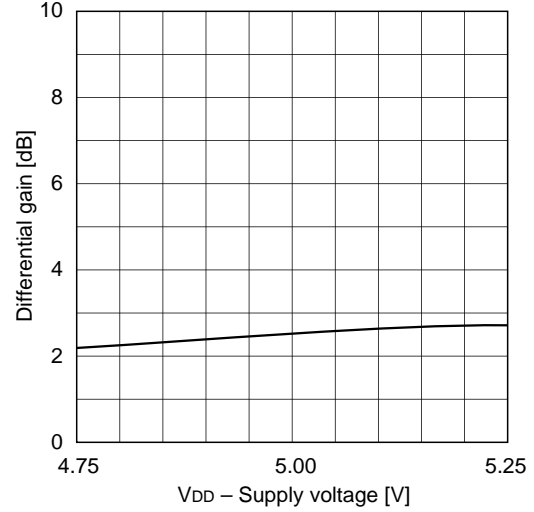
**High frequency gain vs. Supply voltage**



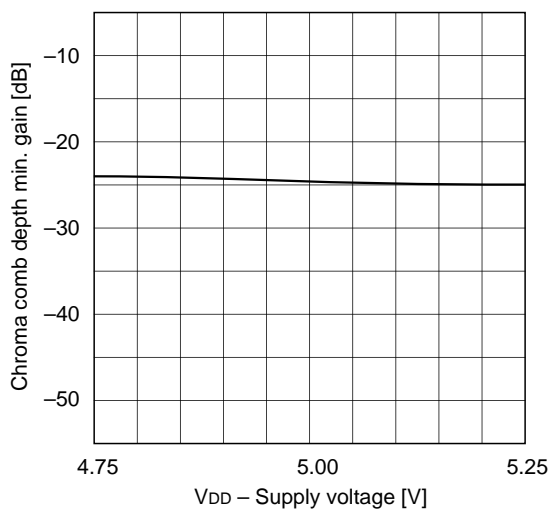
**Frequency response vs. Supply voltage**



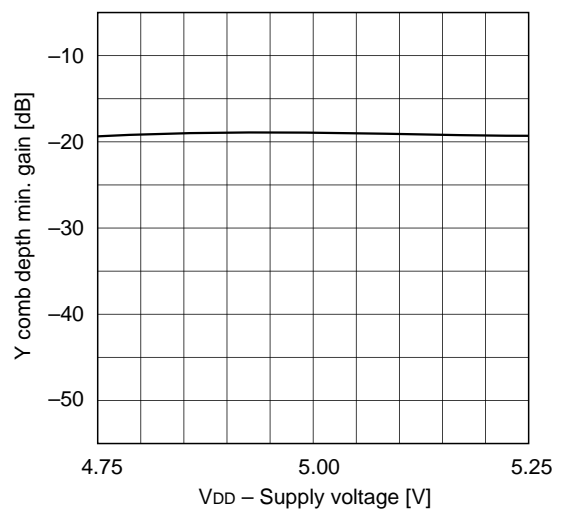
**Differential gain vs. Supply voltage**

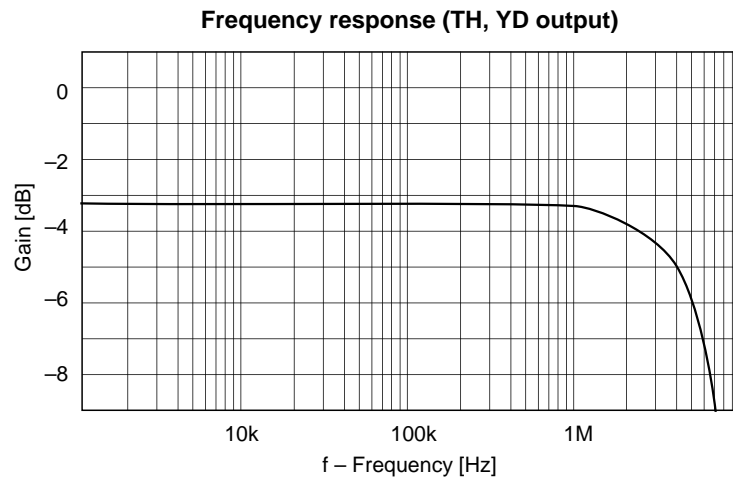
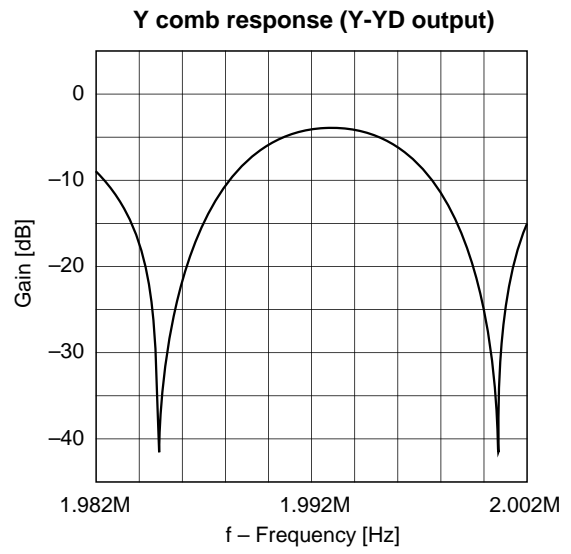
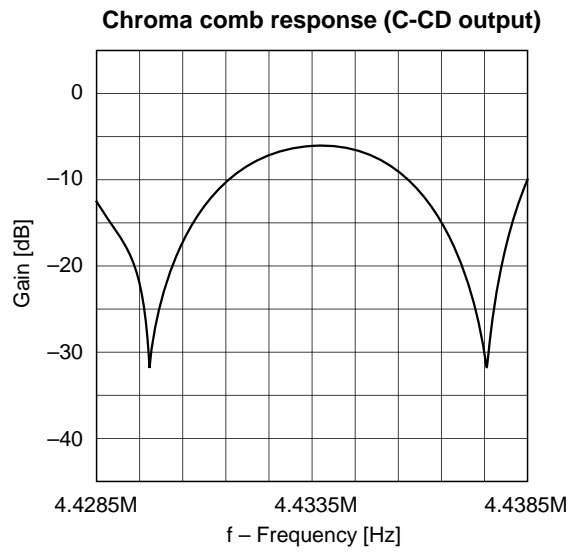


**Chroma comb depth min. gain vs. Supply voltage**



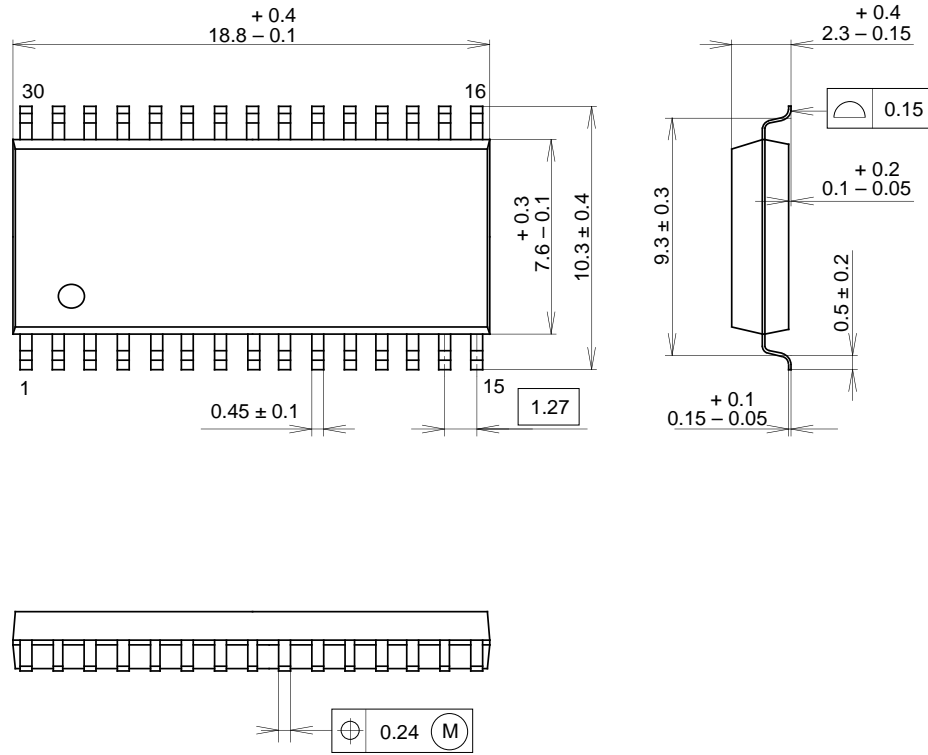
**Y comb depth min. gain vs. Supply voltage**





Package Outline Unit: mm

30PIN SOP (PLASTIC)



SONY CODE	SOP-30P-L01
EIAJ CODE	SOP030-P-0375
JEDEC CODE	_____

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.7g