

CMOS-CCD 1H Delay Line for PAL

Description

The CXL5505M/P are CMOS-CCD delay line ICs that provide 1H delay time for PAL signals including the external low-pass filter.

Features

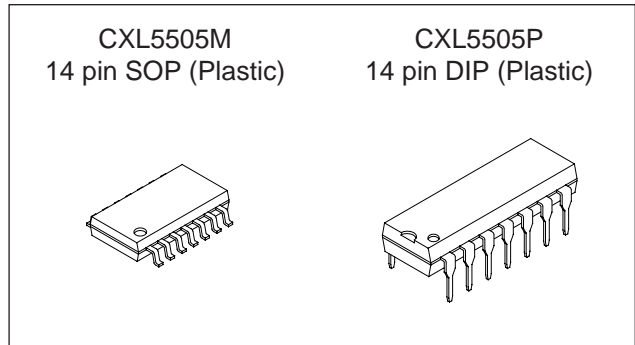
- Single 5V power supply
- Low power consumption 100mW (Typ.)
- Built-in peripheral circuits
- Built-in quadruple PLL circuit

Functions

- 1130-bit CCD register
- Clock driver
- Auto-bias circuit
- Input clamp circuit
- Sample-and-hold circuit
- PLL circuit

Structure

CMOS-CCD



Absolute Maximum Ratings (Ta = 25°C)

| | | | |
|-------------------------------|------------------|-------------|----|
| • Supply voltage | V _{DD} | 6 | V |
| • Operating temperature | T _{opr} | -10 to +60 | °C |
| • Storage temperature | T _{stg} | -55 to +150 | °C |
| • Allowable power dissipation | P _D | | |
| | CXL5505M | 400 | mW |
| | CXL5505P | 800 | mW |

Recommended Operating Condition (Ta = 25°C)

| | | | |
|----------------|-----------------|--------|---|
| Supply voltage | V _{DD} | 5 ± 5% | V |
|----------------|-----------------|--------|---|

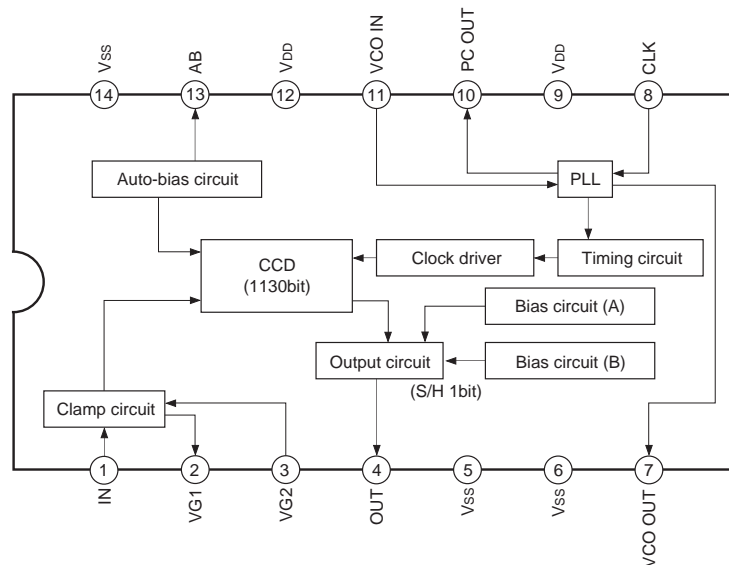
Recommended Clock Conditions (Ta = 25°C)

- Input clock amplitude V_{CLK} 0.3 to 1.0 V_{p-p}
(0.5V_{p-p} typ.)
- Clock frequency f_{CLK} 4.433619 MHz
- Input clock waveform Sine wave

Input Signal Amplitude

V_{SIG} 575mVp-p (Max.) (at internal clamp condition)

Block Diagram and Pin Configuration (Top View)



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Pin Description

| Pin No. | Symbol | I/O | Description | Impedance |
|---------|-----------------|-----|-------------------------|--------------------|
| 1 | IN | I | Signal input | > 10kΩ at no clamp |
| 2 | VG1 | O | Gate bias 1 DC output | |
| 3* | VG2 | I | Gate bias 2 DC input | |
| 4 | OUT | O | Signal output | 40 to 500Ω |
| 5 | V _{SS} | — | GND | |
| 6 | V _{SS} | — | GND | |
| 7 | VCO OUT | O | VCO output | |
| 8 | CLK | I | Clock input | > 10kΩ |
| 9 | V _{DD} | — | Power supply (5V) | |
| 10 | PC OUT | O | Phase comparator output | |
| 11 | VCO IN | I | VCO input | |
| 12 | V _{DD} | — | Power supply (5V) | |
| 13 | AB | O | Auto-bias DC output | 600 to 200kΩ |
| 14 | V _{SS} | — | GND (SUB) | |

* Description of Pin 3 (VG2)

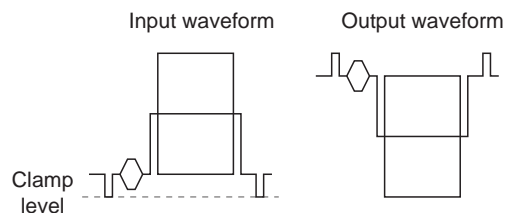
Control of input signal clamp condition

0V Sync tip clamp condition

5V Center bias condition

Center biased to approx. 2.1V by means of the IC internal resistance (approx. 10kΩ).

In this mode, the input signal is limited to APL 50% and the maximum input signal amplitude is 200mVp-p.



Electrical Characteristics

(Ta = 25°C, V_{DD} = 5V, f_{CLK} = 4.433619MHz, V_{CLK} = 500mVp-p, sine wave)

See "Electrical Characteristics Test Circuit"

| Item | Symbol | Test condition | SW condition | | | Min. | Typ. | Max. | Unit | Note |
|--------------------|-----------------|---|--------------|---|---|------|------|------|--------|------|
| | | | 1 | 2 | 3 | | | | | |
| Supply current | I _{DD} | — | a | a | — | 11 | 20 | 29 | mA | 1 |
| Low frequency gain | GL | 200kHz, 500mVp-p, sine wave | a | a | b | -2 | 0 | 2 | dB | 2 |
| Frequency response | f _R | 200kHz ↔ 4.43MHz, 150mVp-p, sine wave | b ↓ c | b | b | -2 | -1 | 0 | dB | 3 |
| Differential gain | DG | 5-staircase wave (See Note 4) | d | a | c | 0 | 3 | 5 | % | 4 |
| Differential phase | DP | 5-staircase wave (See Note 4) | d | a | c | 0 | 3 | 5 | degree | 4 |
| S/H pulse coupling | CP | No signal input | f | b | a | — | — | 350 | mVp-p | 5 |
| S/N ratio | SN | 50% white video signal (See Note 6) | e | a | d | 52 | 56 | — | dB | 6 |

Notes

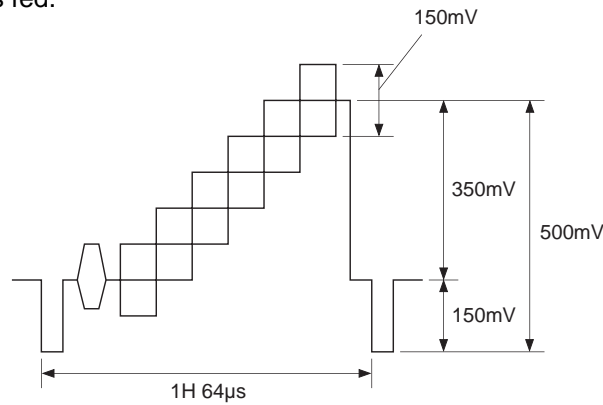
- (1) This is the IC supply current value during clock and signal input.
- (2) GL is the output gain of OUT pin when a 500mVp-p, 200kHz sine wave is fed to IN pin.

$$GL = 20 \log \frac{\text{OUT pin output voltage [mVp-p]}}{500 \text{ [mVp-p]}} \text{ [dB]}$$

- (3) Indicates the dissipation at 4.43MHz in relation to 200kHz.
From the output voltage at OUT pin when a 150mVp-p, 200kHz sine wave is fed to IN pin, and from the output voltage at OUT pin when a 150mVp-p, 4.43MHz sine wave is fed to same, calculation is made according to the following formula.

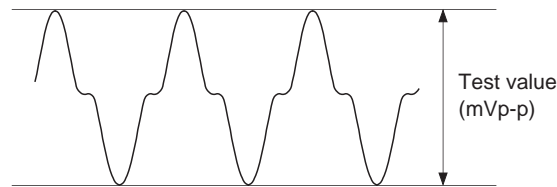
$$fR = 20 \log \frac{\text{OUT pin output voltage (4.43MHz) [mVp-p]}}{\text{OUT pin output voltage (200kHz) [mVp-p]}} \text{ [dB]}$$

- (4) In figure below, differential gain (DG) and differential phase (DP) are tested with a vector scope when the 5-staircase wave is fed.

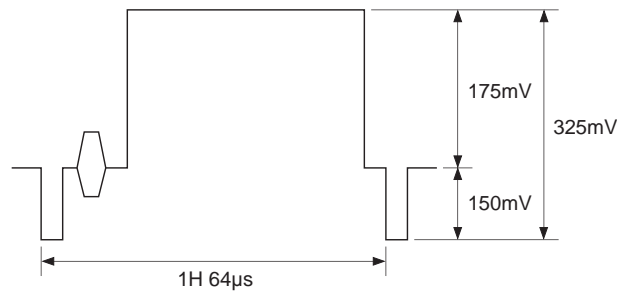


Input waveform

- (5) The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested.



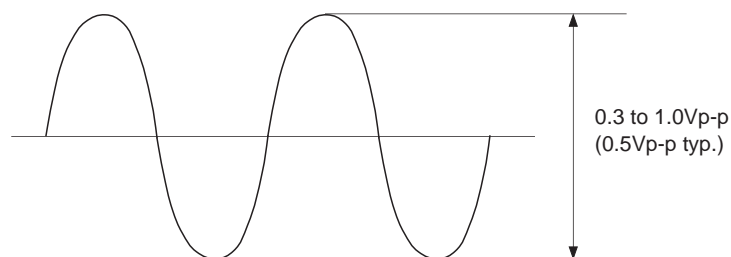
- (6) S/N ratio during a 50% white video signal input shown in figure below is tested at a video noise meter, in BPF 100kHz to 5MHz, Sub Carrier Trap mode.



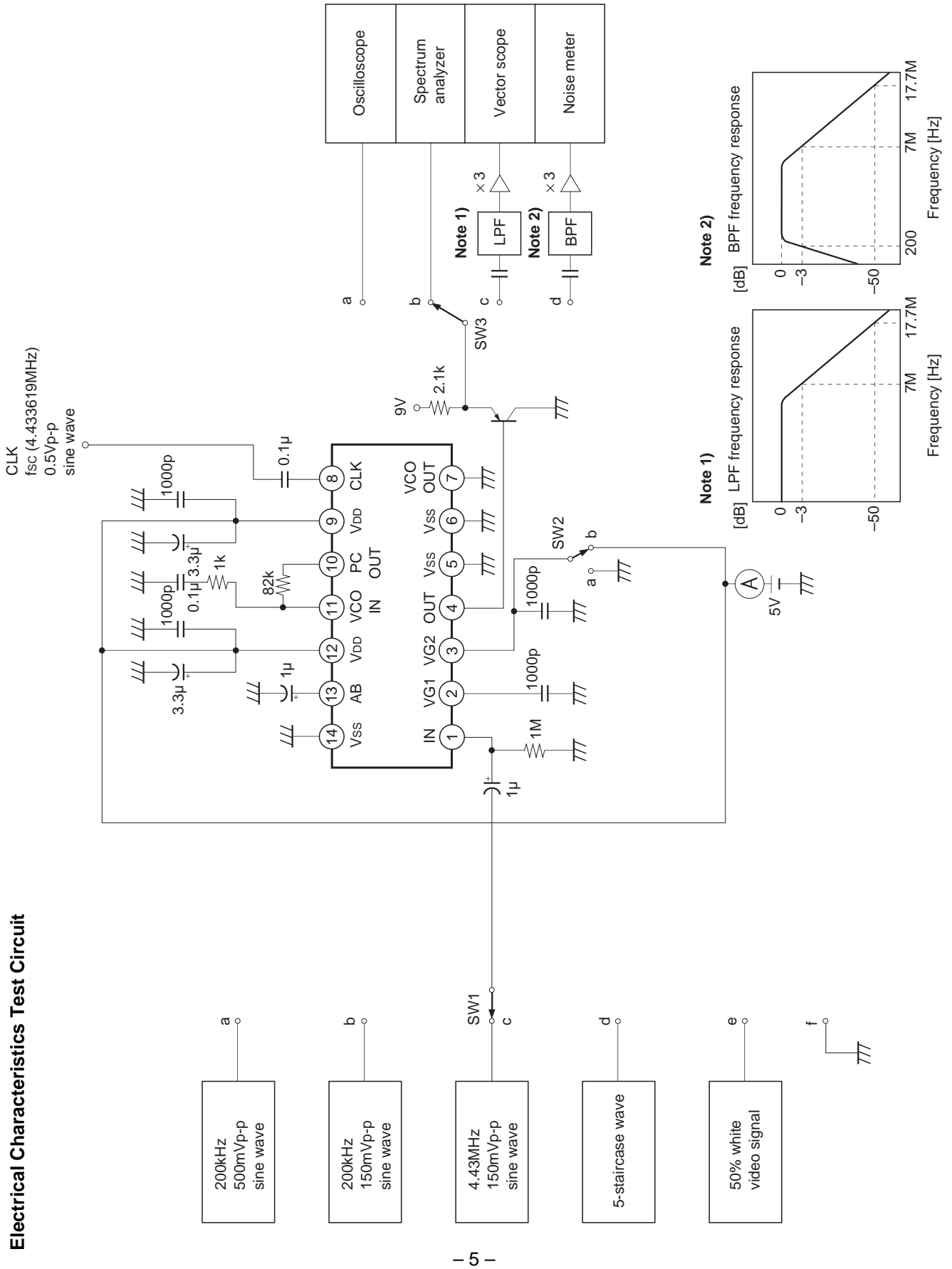
Input waveform

Clock

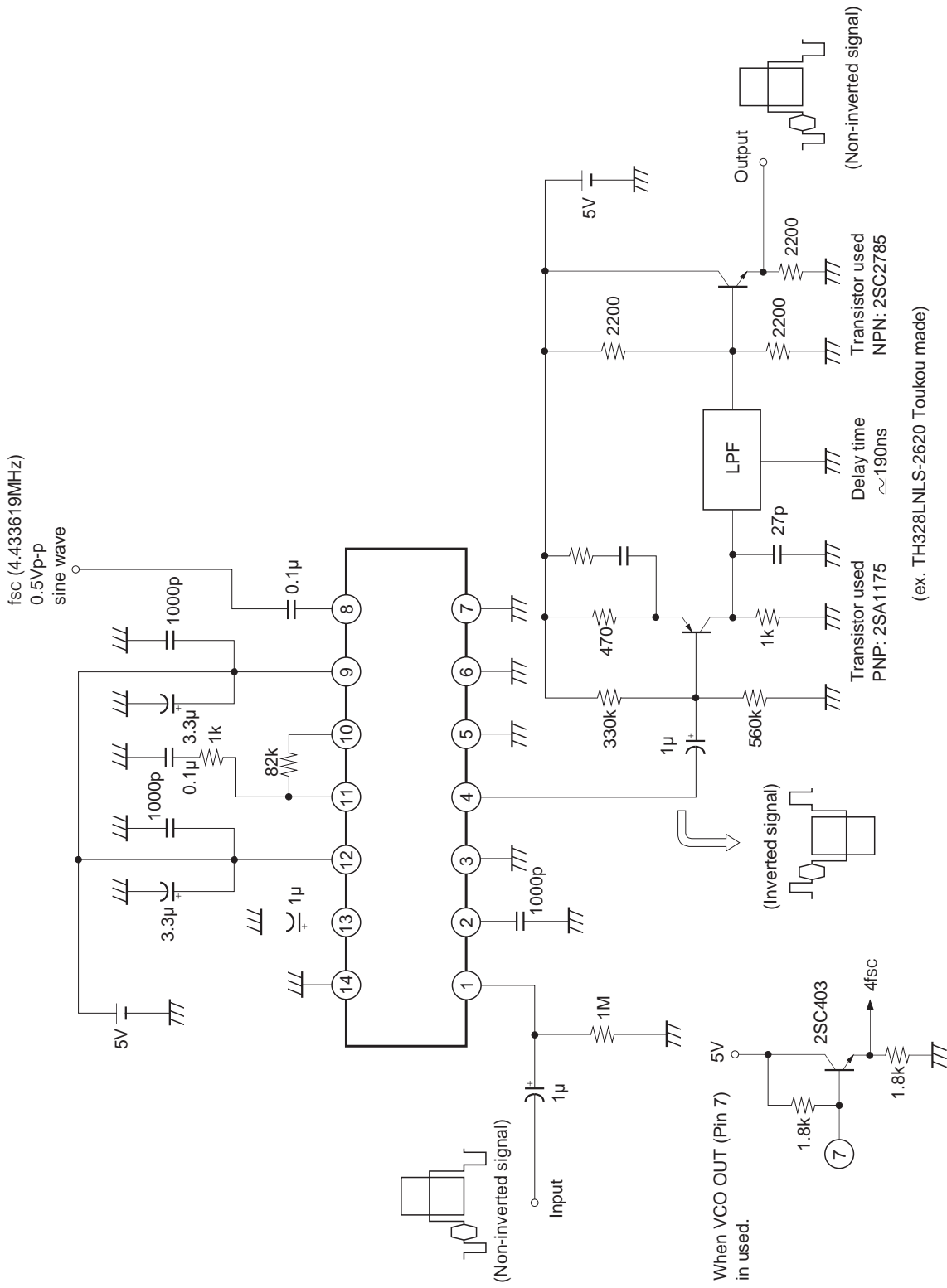
fsc (4.433619MHz) sine wave



Electrical Characteristics Test Circuit

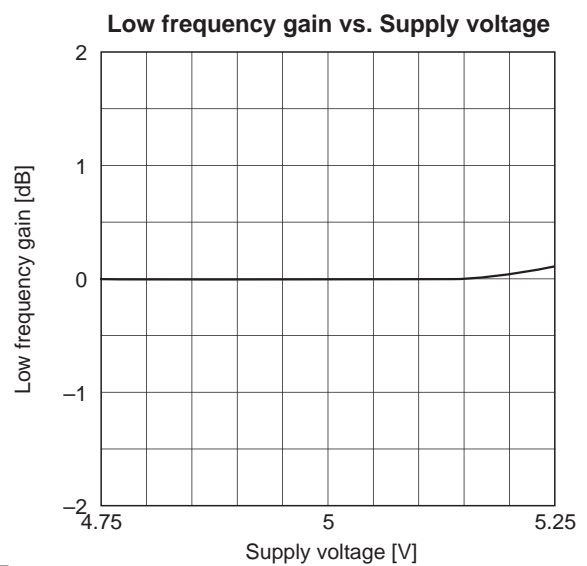
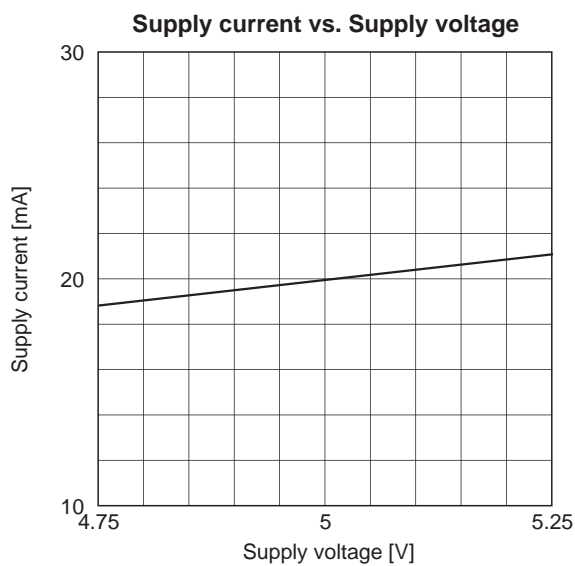
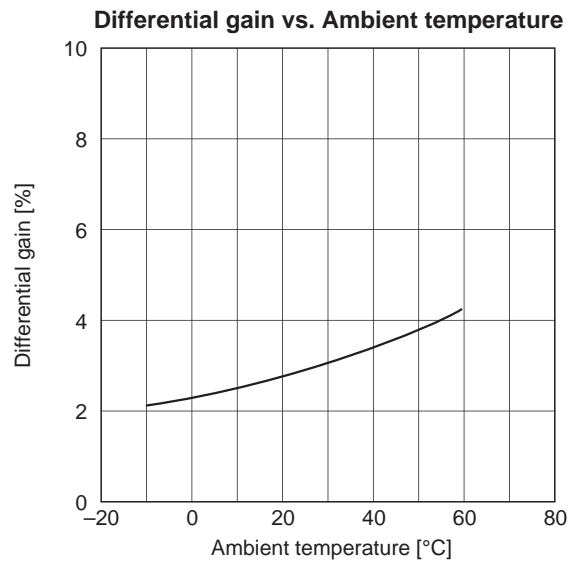
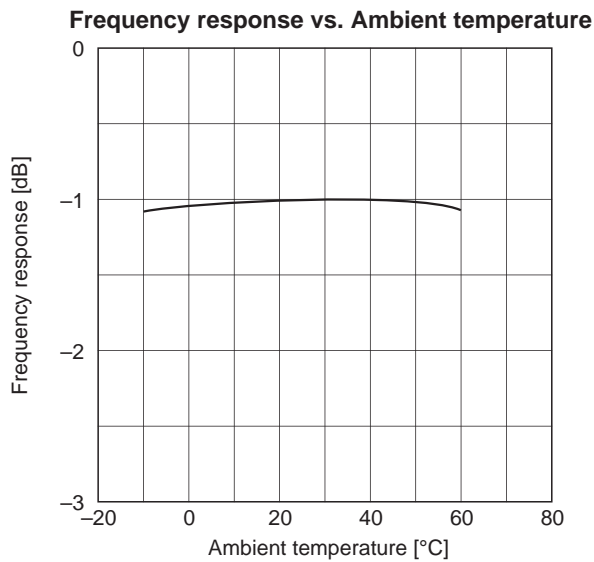
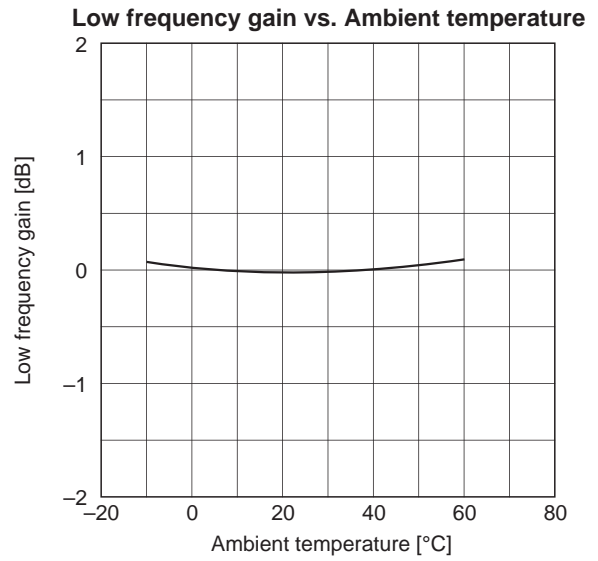
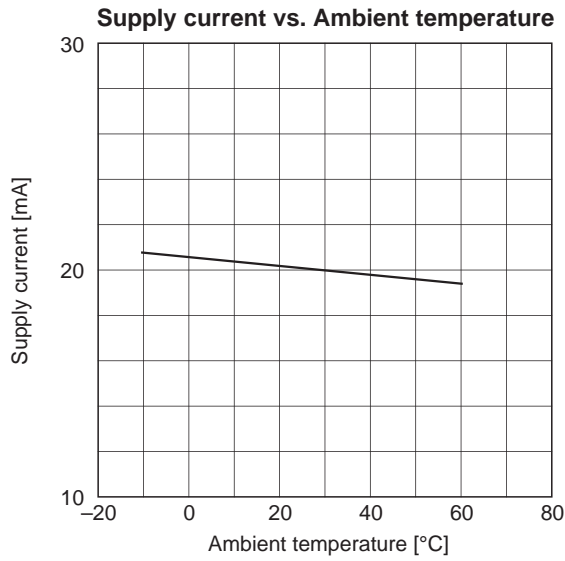


Application Circuit

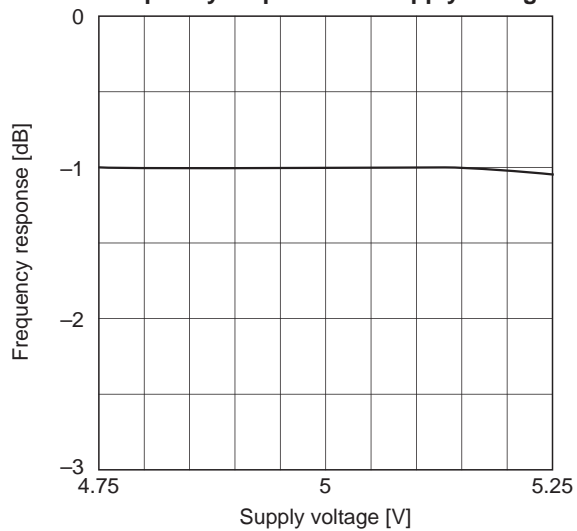


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

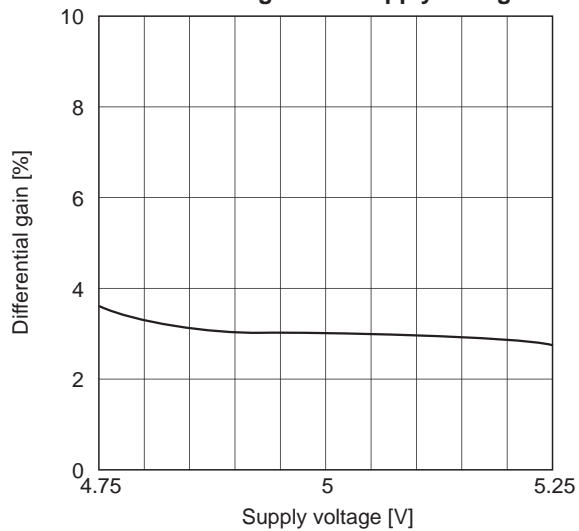
Example of Representative Characteristics



Frequency response vs. Supply voltage



Differential gain vs. Supply voltage



Frequency response

