

CMOS 16-bit Single Chip Microcomputer

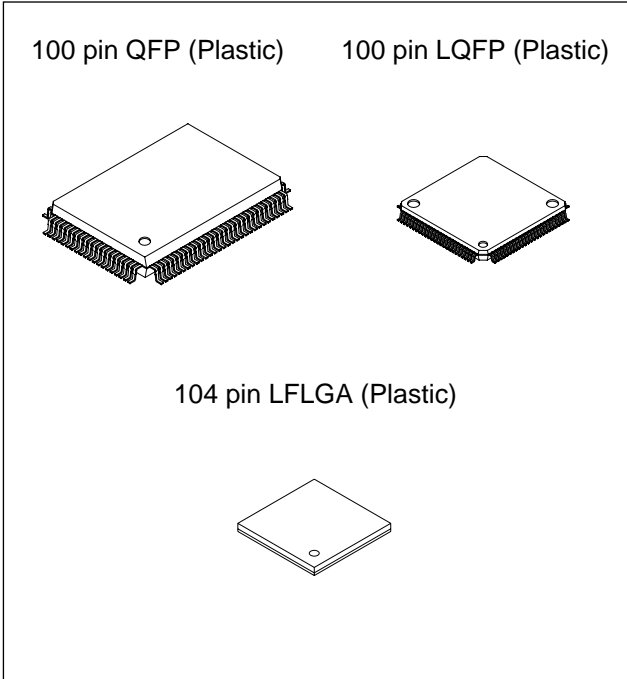
Description

The CXP972032/973032/973064 is a CMOS 16-bit microcomputer integrating on a single chip an A/D converter, serial interface, I²C bus interface, timer, PWM output circuit, programmable pattern generator, remote control receive circuit, parallel interface, as well as basic configurations like a 16-bit CPU, ROM, RAM, and I/O port.

This LSI also provides the sleep/stop functions that enable lower power consumption.

Features

- An efficient instruction set as a controller
 - Direct addressing, numerous abbreviated forms, multiplication and division instructions
- Instruction sets for C language and RTOS
 - Highly quadratic instruction system, general-purpose register of 16-bit × 8-pin × 16-bank configuration
- Minimum instruction cycle
 - 50ns at 40MHz operation (2.7 to 3.6V)
- Incorporated ROM capacity
 - 128K bytes (CXP972032/973032)
 - 256K bytes (CXP973064)
- Incorporated RAM capacity
 - 7.5K bytes (CXP972032)
 - 11.5K bytes (CXP973032/973064)
- Peripheral functions
 - A/D converter 8-bit 12-analog input, successive approximation system, 3-stage FIFO (Conversion time: 1.55μs at 40MHz)
 - Serial interface Asynchronous serial interface (UART)
 - I²C bus interface 128-byte buffer RAM, 3 channels
64-byte buffer RAM (supports master/slave and automatic transfer mode)
 - Timers 8-bit timer/counter, 2 channels (with timing output)
16-bit capture timer/counter (with timing output)
16-bit timer, 4 channels, watchdog timer
 - PWM output circuit 14-bit PWM, 4 channels
(2 channels of binary output switch function by PPG)
 - Programmable pattern generator 16-bit output, 64-byte buffer RAM, 1 channel
 - Remote control receive circuit 8-bit pulse measurement counter, 10-stage FIFO
 - Parallel interface External register interface (8-bit parallel bus), 4-chip select
- Interruption 33 factors, 33 vectors, multi-interruption and priority selection possible
- Standby mode Sleep/stop
- Package 100-pin plastic QFP (CXP972032/973032/973064)
100-pin plastic LQFP (CXP972032/973032/973064)
104-pin plastic LFLGA (CXP973064)
- Piggy/evaluation chip CXP971000
- FLASH EEPROM incorporated version CXP973F064

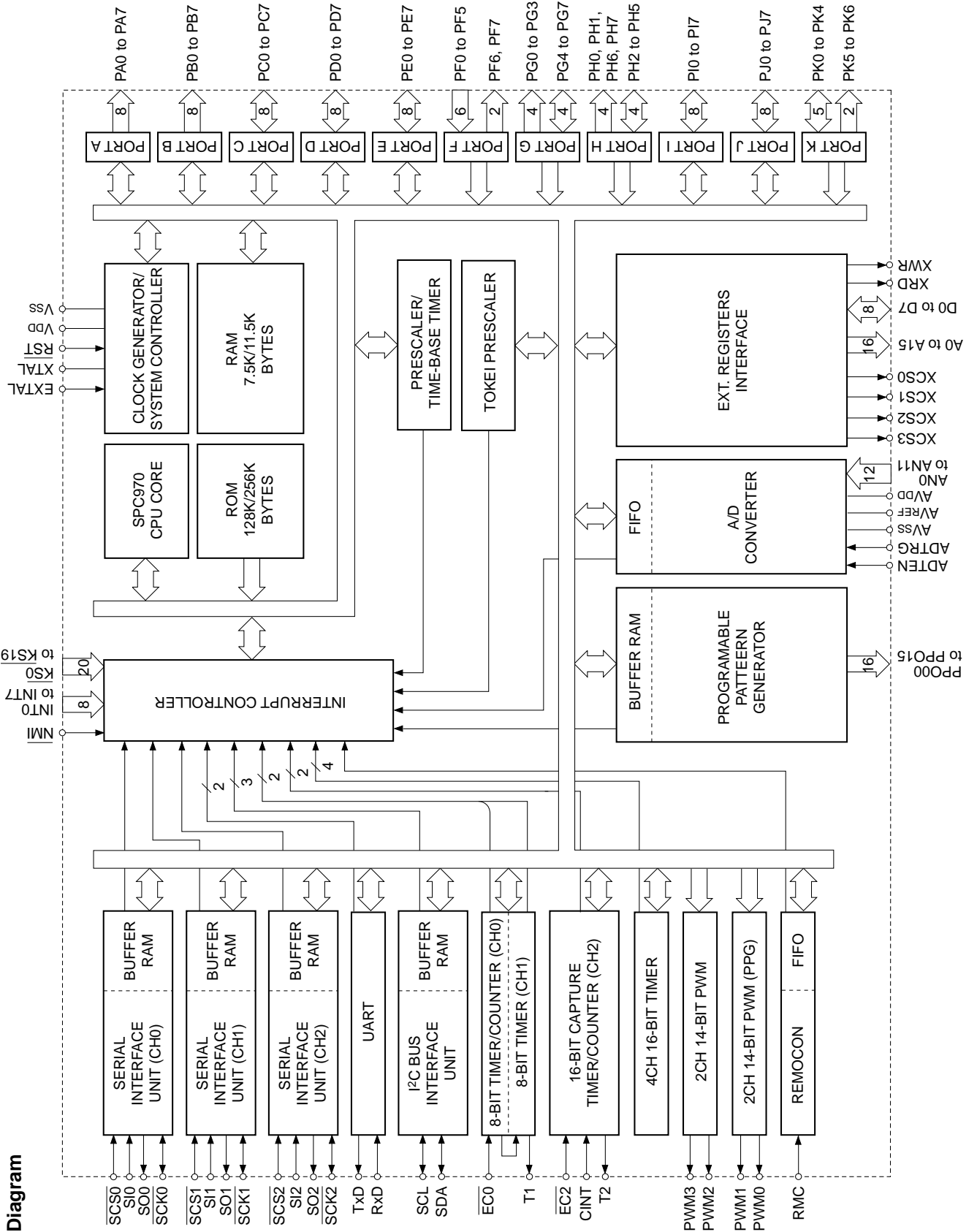


Structure

Silicon gate CMOS IC

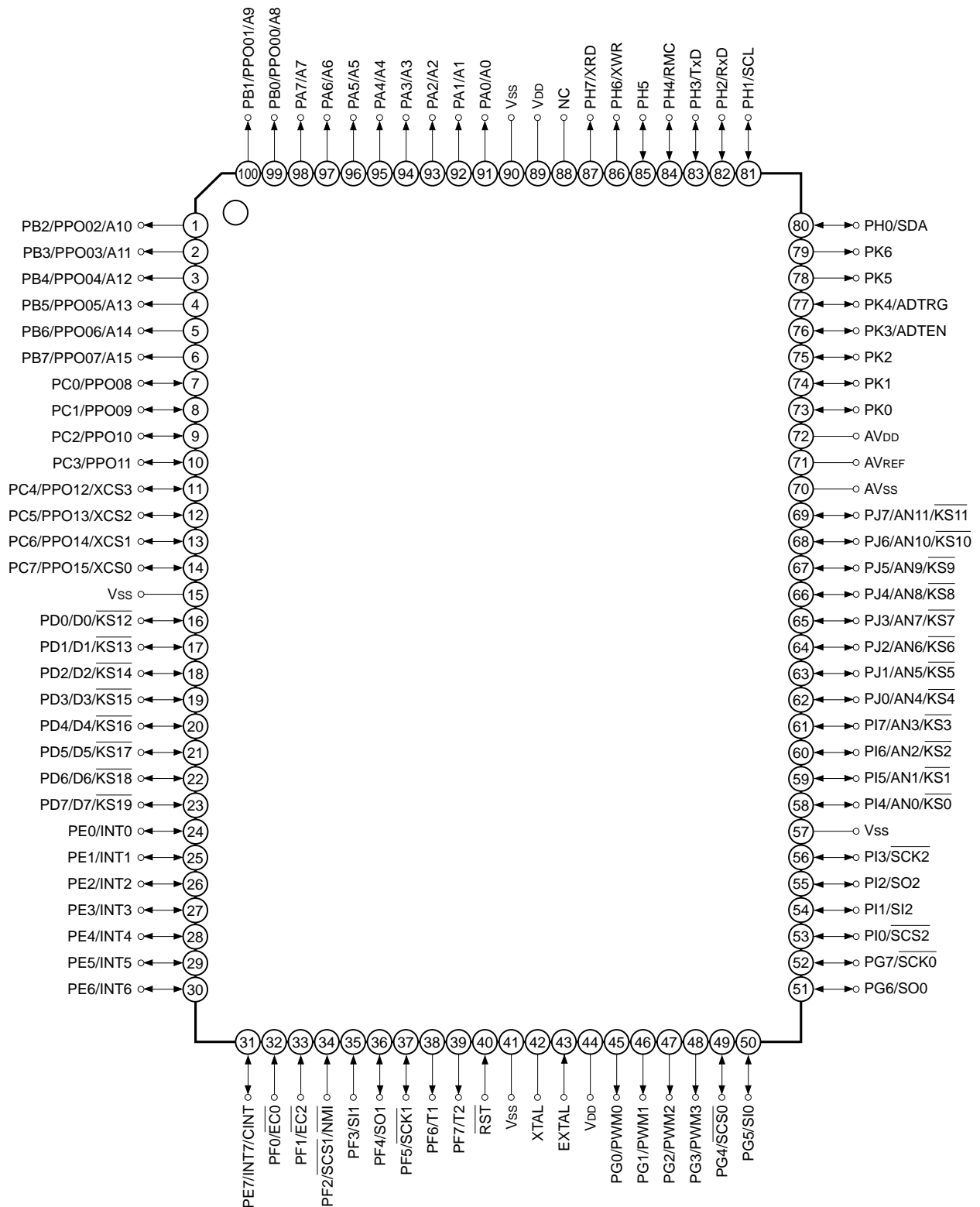
Purchase of Sony's I²C components conveys a licence under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.



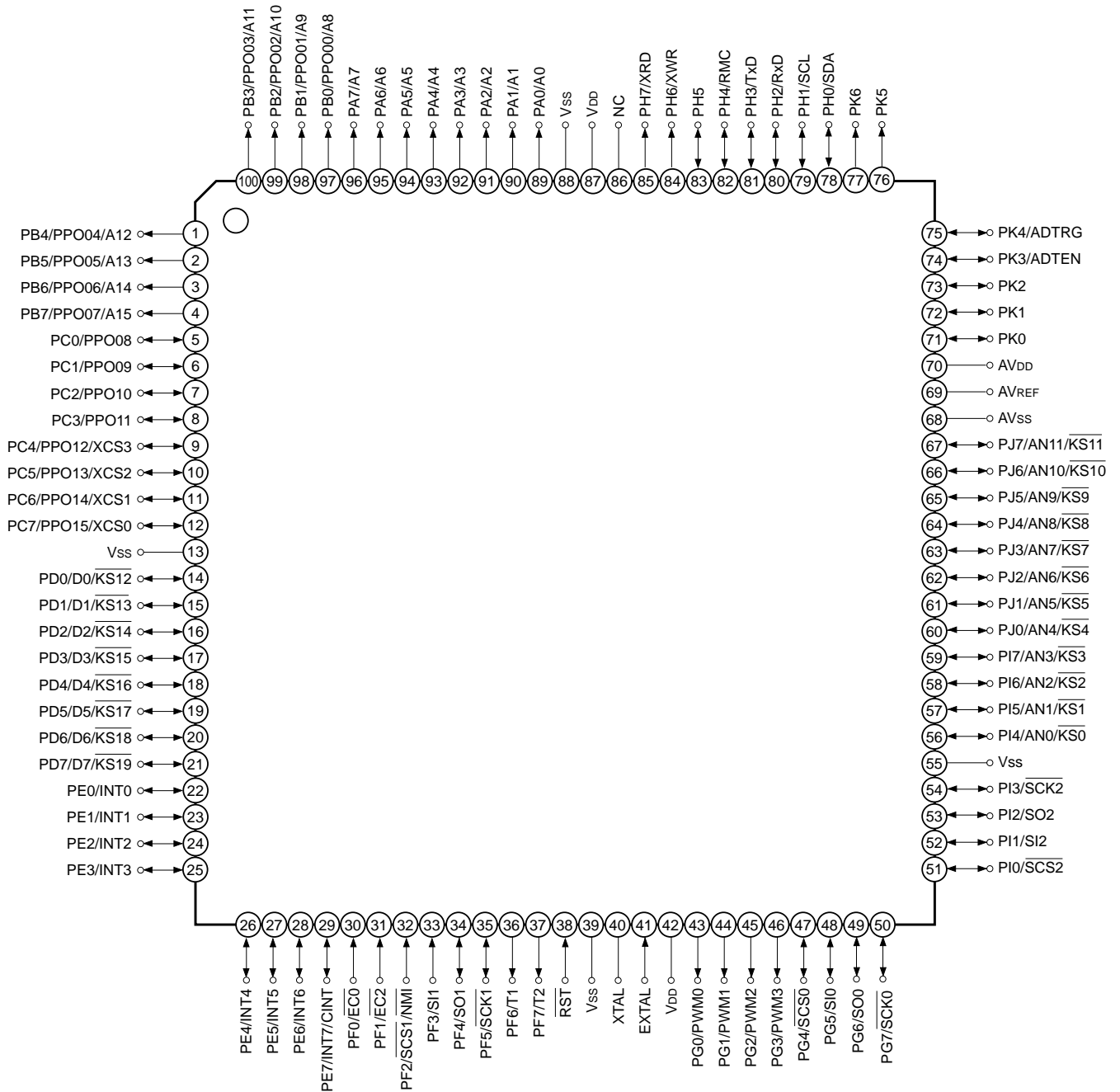
Block Diagram

Pin Assignment 1 (Top View) 100-pin QFP package



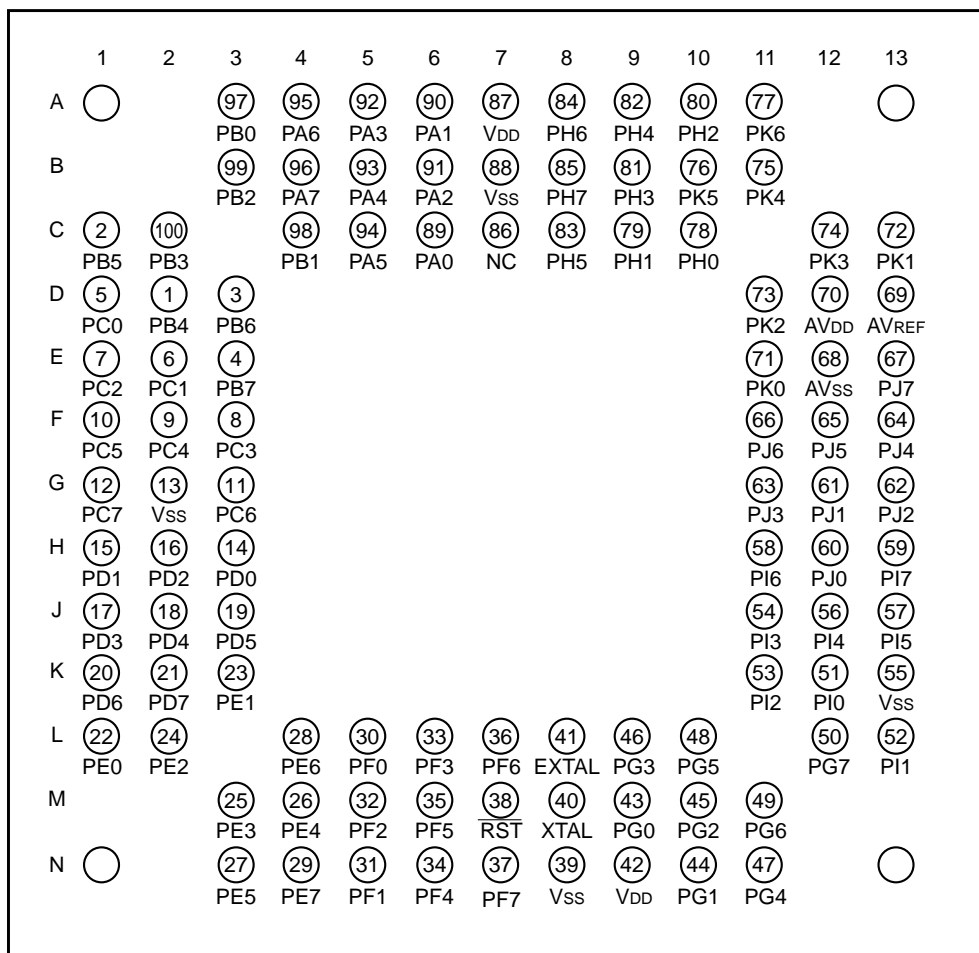
- Note** 1. NC (Pin 88) must be left open. However, use this pin for FLASH EEPROM incorporated version.
 2. Vss and AVss (Pins 15, 41, 57, 70 and 90) must be connected to GND.
 3. VDD and AVDD (Pins 44, 72 and 89) must be connected to VDD.

Pin Assignment 2 (Top View) 100-pin LQFP package



- Note** 1. NC (Pin 86) must be left open. However, use this pin for FLASH EEPROM incorporated version.
 2. Vss and AVss (Pins 13, 39, 55, 68 and 88) must be connected to GND.
 3. VDD and AVDD (Pins 42, 70 and 87) must be connected to VDD.

Pin Assignment 3 (Top View) 104-pin LFLGA package



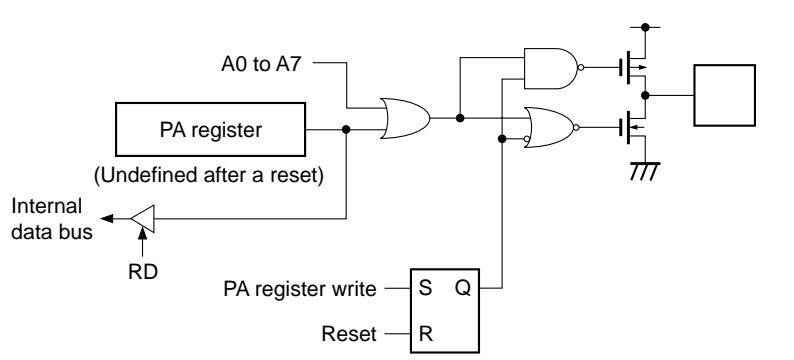
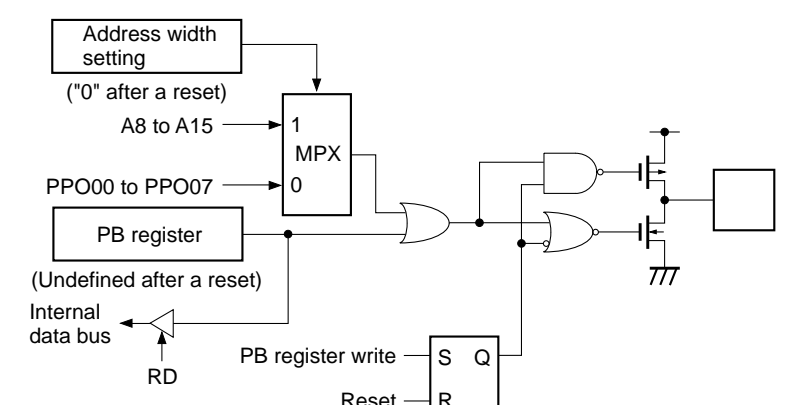
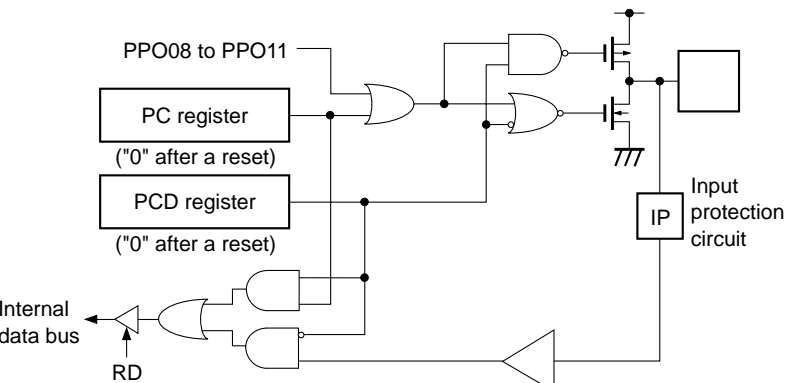
- Note)** 1. NC (Pin C7) must be left open. However, use this pin for FLASH EEPROM incorporated version.
2. V_{SS} and AV_{SS} (Pins B7, E12, G2, K13 and N8) must be connected to GND.
3. V_{DD} and AV_{DD} (Pins A7, D12 and N9) must be connected to V_{DD}.

Pin Functions

Symbol	I/O	Functions	
PA0/A0 to PA7/A7	Output / Output	(Port A) 8-bit output port. (8 pins)	External register interface address bus port output data value and OR output. (8 pins)
PB0/PPO00/A8 to PB7/PPO07/A15	Output / Output / Output	(Port B) 8-bit output port. PPO value and OR output. (8 pins)	External register interface address bus. Address width can be extended in 1-bit units. (8 pins)
PC0/PPO08 to PC3/PPO11	I/O / Output	(Port C) 8-bit I/O port. I/O can be specified in 1-bit units. PPO value and OR output. (8 pins)	Programmable pattern generator outputs. (16 pins)
PC4/PPO12/XCS3 to PC7/PPO15/XCS0	I/O / Output / Output		External register interface chip select signal. Chip select signal output function can be selected in 1-bit units. (4 pins)
PD0/D0/KS12 to PD7/D7/KS19	I/O / I/O / Input	(Port D) 8-bit I/O port. I/O can be specified in 1-bit units. (8 pins)	External register interface data bus. (8 pins) Standby release input function can be specified in 1-bit units. (8 pins)
PE0/INT0 to PE6/INT6	I/O / Input	(Port E) 8-bit I/O port. I/O can be specified in 1-bit units. (8 pins)	External interrupt inputs. (8 pins)
PE7/INT7/CINT	I/O / Input / Input		External capture input for 16-bit capture timer/counter.
PF0/ $\overline{EC0}$ PF1/ $\overline{EC2}$	Input / Input	(Port F) 8-bit port. Lower 6 bits are for input; upper 2 bits are for output. (8 pins)	External event inputs for 8-bit timer/counter. (2 pins)
PF2/ $\overline{SCS1}$ /NMI	Input / Input / Input		Serial chip select (CH1) input. Non-maskable external interrupt input.
PF3/SI1	Input / Input		Serial data (CH1) input.
PF4/SO1	Input / Output		Serial data (CH1) output.
PF5/ $\overline{SCK1}$	Input / I/O		Serial clock (CH1) I/O.
PF6/T1	Output / Output		8-bit timer/counter output.
PF7/T2	Output / Output		16-bit capture timer/counter timing output.
PG0/PWM0 to PG1/PWM1	Output / Output		(Port G) 8-bit port. Lower 4 bits are for output; upper 4 bits are for I/O. Upper 4 bits can be specified in 1-bit units. (8 pins)
PG2/PWM2 PG3/PWM3	Output / Output	14-bit PWM output. (2 pins)	
PG4/ $\overline{SCS0}$	I/O / Input	Serial chip select (CH0) input.	
PG5/SI0	I/O / Input	Serial data (CH0) input.	
PG6/SO0	I/O / Output	Serial data (CH0) output.	
PG7/ $\overline{SCK0}$	I/O / I/O	Serial clock (CH0) I/O.	

Symbol	I/O	Functions	
PH0/SDA	Output / I/O	(Port H) 8-bit port. Lower 2 bits are for large current N-ch open drain outputs; medium 4 bits are for I/O; upper 2 bits are for output. Medium 4 bits can be specified in 1-bit units. (8 pins)	I ² C bus interface data I/O.
PH1/SCL	Output / I/O		I ² C bus interface clock I/O.
PH2/RxD	I/O / Input		UART reception data input.
PH3/TxD	I/O / Output		UART transmission data output.
PH4/RMC	I/O / Input		Remote control receive circuit input.
PH5	I/O		
PH6/XWR	Output / Output		External register interface write signal.
PH7/XRD	Output / Output		External register interface read signal.
PI0/SCS2	I/O / Input	(Port I) 8-bit I/O port. I/O can be specified in 1-bit units. (8 pins)	Serial chip select (CH2) input.
PI1/SI2	I/O / Input		Serial data (CH2) input.
PI2/SO2	I/O / Output		Serial data (CH2) output.
PI3/SCK2	I/O / I/O		Serial clock (CH2) I/O.
PI4/AN0/ KS0 to PI7/AN3/ KS3	I/O / Input / Input		Analog input for A/D converter. (12 pins)
PJ0/AN4/ KS4 to PJ7/AN11/ KS11	I/O / Input / Input	(Port J) 8-bit I/O port. I/O can be specified in 1-bit units. (8 pins)	
PK0 to PK2	I/O	(Port K) 7-bit port. Lower 5 bits are for I/O; upper 2 bits are for output. Lower 5 bits can be specified in 1-bit units. (7 pins)	
PK3/ADTEN	I/O / Input		A/D converter operation enable input by external trigger.
PK4/ADTRG	I/O / Input		External trigger input for A/D converter.
PK5 PK6	Output		
EXTAL	Input	Connects a crystal for main clock oscillation. (When the clock is supplied externally, input it to EXTAL and input an opposite phase clock to XTAL.)	
XTAL			
RST	Input	System reset. Active at "L" level.	
AVDD		Positive power supply for A/D converter. (Must be the same voltage with V _{DD})	
AVREF	Input	Reference voltage input for A/D converter. (Must be the same voltage with V _{DD})	
AVss		GND for A/D converter.	
V _{DD}		Positive power supply. (Connect both V _{DD} pins to positive power supply.)	
V _{SS}		GND. (Connect all four V _{SS} pins to GND.)	
NC		NC. (NC is used for FLASH EEPROM incorporated version.)	

I/O Circuit Format for Pins

Pin	Circuit format	After a reset
<p>PA0/A0 to PA7/A7</p>		<p>Hi-Z</p>
<p>PB0/PPO0/A8 to PB7/PPO7/ A15</p>		<p>Hi-Z</p>
<p>PC0/PPO08 to PC3/PPO11</p>		<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PC4/PPO12/ XCS3 to PC7/PPO15/ XCS0</p>	<p>XCS output setting ("0" after a reset) XCS3 to XCS0 → 1 PPO12 to PPO15 → 0</p> <p>MPX</p> <p>PC register ("0" after a reset)</p> <p>PCD register ("0" after a reset)</p> <p>Internal data bus</p> <p>RD</p> <p>IP</p>	<p>Hi-Z</p>
<p>PD0/D0/KS12 to PD7/D7/ KS19</p>	<p>WR (external register area)</p> <p>Internal data bus → External register I/F</p> <p>External register operation enable</p> <p>CLR → PD register ("0" after a reset)</p> <p>CLR → PDD register ("0" after a reset)</p> <p>Internal data bus ← RD</p> <p>Standby release</p> <p>Internal data bus ← External register I/F</p> <p>RD (external register area)</p> <p>External register operation enable</p> <p>IP</p> <p>* Large current drive 5mA (V_{DD} = 2.7 to 3.6V)</p>	<p>Hi-Z</p>
<p>PE0/INT0 to PE7/INT7/ CINT</p>	<p>PE register (Undefined after a reset)</p> <p>PED register ("0" after a reset)</p> <p>Internal data bus ← RD</p> <p>INT0 to INT7/CINT</p> <p>CMOS Schmitt input</p> <p>IP</p>	<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PF0/$\overline{\text{EC0}}$ PF1/$\overline{\text{EC2}}$</p>		<p>Hi-Z</p>
<p>PF2/$\overline{\text{SCS1}}$/ NMI</p>		<p>Hi-Z</p>
<p>PF3/SI1</p>		<p>Hi-Z</p>
<p>PF4/SO1</p>		<p>Hi-Z</p>
<p>PF5/$\overline{\text{SCK1}}$</p>		<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PF6/T1</p>		<p>"H" level</p>
<p>PF7/T2</p>		<p>"H" level ("H" level at ON resistance of pull-up transistor by a reset.)</p>
<p>PG0/PWM0 to PG3/PWM3</p>		<p>Hi-Z</p>

Pin	Circuit format	After a reset
PG4/ $\overline{SCS0}$		Hi-Z
PG5/SI0		Hi-Z
PG6/SO0		Hi-Z

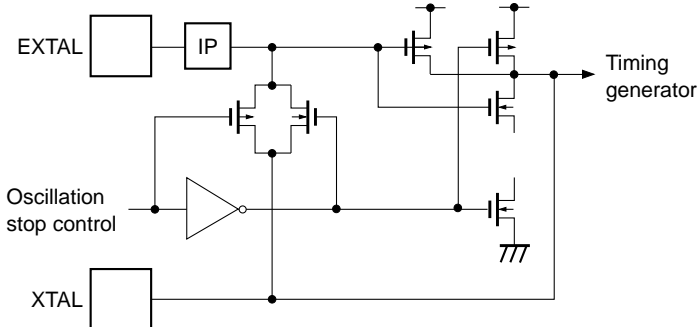
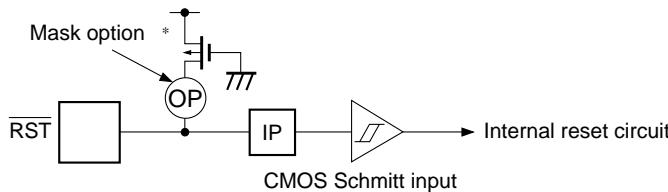
Pin	Circuit format	After a reset
<p>PG7/$\overline{\text{SCK0}}$</p>	<p> $\overline{\text{SCK0}}$ PG register (Undefined after a reset) PGSL register ("0" after a reset) $\overline{\text{SCK0}}$ output enable PGD register ("0" after a reset) Internal data bus RD $\overline{\text{SCK0}}$ CMOS Schmitt input IP </p>	<p>Hi-Z</p>
<p>PH0/SDA PH1/SCL</p>	<p> SDA, SCL PH register ("1" after a reset) PHSL register ("0" after a reset) Internal data bus RD SDA, SCL CMOS Schmitt input IP * Large current drive 5mA ($V_{DD} = 2.7$ to $3.6V$) </p>	<p>Hi-Z</p>
<p>PH2/RxD</p>	<p> PHL register (Undefined after a reset) PHD register ("0" after a reset) Internal data bus RD RxD CMOS Schmitt input IP </p>	<p>Hi-Z</p>

Pin	Circuit format	After a reset
PH3/TxD		Hi-Z
PH4/RMC		Hi-Z
PH5		Hi-Z
PH6/XWR PH7/XRD		Hi-Z

Pin	Circuit format	After a reset
<p>PI0/$\overline{\text{SCS2}}$</p>		<p>Hi-Z</p>
<p>PI1/SI2</p>		<p>Hi-Z</p>
<p>PI2/SO2</p>		<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PI3/$\overline{\text{SCK2}}$</p>		<p>Hi-Z</p>
<p>PI4/$\overline{\text{AN0/KS0}}$ to PI7/$\overline{\text{AN3/}}$ $\overline{\text{KS3}}$</p>		<p>Hi-Z</p>
<p>PJ0/$\overline{\text{AN4/KS4}}$ to PJ7/$\overline{\text{AN11/}}$ $\overline{\text{KS11}}$</p>		<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PK0 to PK2</p>		<p>Hi-Z</p>
<p>PK3/ADTEN PK4/ADTRG</p>		<p>Hi-Z</p>
<p>PK5</p>		<p>"H" level</p>
<p>PK6</p>	<p>* Pull-up transistor approximately 150kΩ (V_{DD} = 2.7 to 3.6V)</p>	<p>"H" level ("H" level at ON resistance of pull-up transistor by a reset.)</p>

Pin	Circuit format	After a reset
<p>XTAL EXTAL</p>	 <ul style="list-style-type: none"> • Diagram shows circuit configuration during oscillation. • Feedback resistor is removed during standby stop mode, and XTAL is driven at "H" level. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p>	 <p>* Pull-up transistor approximately 30kΩ (VDD = 2.7 to 3.6V)</p>	<p>"L" level (during a reset)</p>

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +4.6	V	
	AV _{DD}	AV _{SS} to +4.6* ¹	V	
	AV _{REF}	AV _{SS} to +4.6* ¹	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +4.6* ²	V	
Output voltage	V _{OUT}	-0.3 to +4.6* ²	V	
High level output current	I _{OH}	-5.0	mA	Output (value per pin)
High level total output current	ΣI _{OH}	-50	mA	Total for all output pins
Low level output current	I _{OL}	15.0	mA	All pins excluding large current output pins (value per pin)
	I _{OLC}	20.0	mA	Large current output pins* ³ (value per pin)
Low level total output current	ΣI _{OL}	130	mA	Total for all output pins
Operating temperature	T _{opr}	-30 to +85	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP-100P-L01
		380		LQFP-100P-L01
		500		LFLGA-104P-01

*¹ AV_{DD} and AV_{REF} must be the same voltage with V_{DD}.

*² V_{IN} and V_{OUT} excluding PH0 and PH1 must not exceed V_{DD} + 0.3V.

*³ The large current drive transistor is N-ch transistor of PD and PH0, PH1.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	2.7	3.6	V	
		2.0	3.6		Guaranteed data hold range during stop mode
	AV _{DD}	2.7	3.6	V	*1
	AV _{REF}	2.7	3.6	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS Schmitt input*3
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.2	V	EXTAL*4
Low level input voltage	V _{IL}	0	0.2V _{DD}	V	*2
	V _{ILS}	0	0.2V _{DD}	V	CMOS Schmitt input*3
	V _{ILEX}	-0.3	0.4	V	EXTAL*4
Operating temperature	T _{opr}	-30	+85	°C	

*1 AV_{DD} and AV_{REF} must be the same voltage with V_{DD}.

*2 PC, PD, PF4, PG6, PH3, PI2, PI4 to PI7, PJ, PK0 to PK2 for normal input port.

*3 $\overline{\text{RST}}$, PE, PF0 to PF3, PF5, PG4, PG5, PG7, PH0 to PH2, PH4, PH5, PI0, PI1, PI3, PK3 and PK4.

*4 Specified only during self-oscillation.

Electrical Characteristics

DC Characteristics 1

(Top = -30 to +85°C, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit		
High level output voltage	V _{OH}	PD to PE, PF6, PF7, PG0 to PG5, PH2, PH4, PH5, PI to PJ, PK0 to PK6	V _{DD} = 3.0V, I _{OH} = -0.15mA	2.70			V		
			V _{DD} = 2.7V, I _{OH} = -0.15mA	2.40					
		PA to PC, PF4, PF5, PG6, PG7, PH3, PH6, PH7, PI2, PI3	V _{DD} = 3.0V, I _{OH} = -0.5mA	2.30			V		
			V _{DD} = 2.7V, I _{OH} = -0.5mA	2.00					
		Low level output voltage	V _{OL}	PE, PF6, PF7, PG0 to PG5, PH2, PH4, PH5, PI0, PI1, PI4 to PI7, PJ, PK0 to PK6	I _{OL} = 1.2mA			0.30	V
					I _{OL} = 1.6mA			0.50	V
PA to PC, PF4, PF5, PG6, PG7, PH3, PH6, PH7, PI2, PI3	I _{OL} = 2.0mA					0.30	V		
	I _{OL} = 3.0mA					0.50	V		
PD, PH0, PH1	I _{OL} = 5.0mA					1.00	V		
Input current	I _{IHE}	EXTAL	V _{DD} = 3.6V, V _{IH} = 3.6V	0.3		61	μA		
	I _{I LE}		V _{DD} = 3.6V, V _{IL} = 0.3V	-0.3		-61	μA		
	I _{ILR}	RST*1	V _{DD} = 3.6V, V _{IL} = 0.3V	-0.9		-250	μA		
I/O leakage current	I _{Iz}	PA to PJ, PK0 to PK6, RST*1	V _{DD} = 3.6V, V _I = 0, 3.6V			±31	μA		
Open drain output leakage current (N-ch Tr. off state)	I _{LOH}	PH0, PH1	V _{DD} = 3.6V, V _{IH} = 3.6V			31	μA		

*1 $\overline{\text{RST}}$ specifies the input current when pull-up resistor has been selected; the leakage current when no resistor has been selected.

DC Characteristics 2 (CXP972032)

(Topr = -30 to +85°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*1	^{*2} IDD1	VDD, VSS	VDD = 3.3 ± 0.3V, fEX = fsrc = 40MHz, External clock operation A/D off state, PLL off state		32	40	mA
	^{*2} IDDS2	VDD, VSS	VDD = 3.3 ± 0.3V, fEX = fsrc = 40MHz, External clock operation A/D off state, PLL off state, sleep mode		8.0	10	mA
	IDDS3	VDD, VSS	VDD = 3.6V, stop mode	85°C or less		25	μA
	75°C or less			13			
	50°C or less			5			

*1 When all output pins are open.

*2 When the upper two bits (PCK1, PCK0) of the clock control register (CLC: 0002FEh) are set to "00" and the LSI is operated in high-speed mode (2 frequency dividing clock).

DC Characteristics 2 (CXP973032/973064)

(Topr = -30 to +85°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*1	^{*2} IDD1	VDD, VSS	VDD = 3.3 ± 0.3V, fEX = fsrc = 40MHz, External clock operation A/D off state, PLL off state		35	44	mA
	^{*2} IDDS2	VDD, VSS	VDD = 3.3 ± 0.3V, fEX = fsrc = 40MHz, External clock operation A/D off state, PLL off state, sleep mode		8.8	11	mA
	IDDS3	VDD, VSS	VDD = 3.6V, stop mode	85°C or less		25	μA
	75°C or less			13			
	50°C or less			5			

*1 When all output pins are open.

*2 When the upper two bits (PCK1, PCK0) of the clock control register (CLC: 0002FEh) are set to "00" and the LSI is operated in high-speed mode (2 frequency dividing clock).

I/O Capacitance

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	PF0 to PF3, EXTAL, RST	Clock 1MHz, 0V for all pins excluding measured pins		10	20	pF
Output capacitance	C _{OUT}	PA to PB, PF6, PF7, PG0 to PG3, PH6, PH7, PK5, PK6, XTAL	Clock 1MHz, 0V for all pins excluding measured pins		10	20	pF
I/O capacitance	C _{I/O}	PC to PE, PF4, PF5, PG4 to PG7, PH0 to PH5, PI to PJ, PK0 to PK4	Clock 1MHz, 0V for all pins excluding measured pins		10	20	pF

AC Characteristics

(1) Clock timing

(Topr = -30 to +85°C, VDD = 2.7 to 3.6 V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Main clock base oscillation frequency	fEX	EXTAL, XTAL	Fig.1, Fig.2 Mask option Selection less than 40MHz	4.76	33.86	40.5	MHz
			Fig.1, Fig.2 Mask option Selection less than 20MHz	4.76	20.0	20.5	MHz
Main clock base oscillation input pulse width	tXH	EXTAL, XTAL	fEX = 40.0MHz Fig.1, Fig.2 External clock drive	4.0			ns
	tXL						
	tXH		fEX = 33.86MHz Fig.1, Fig.2 External clock drive	4.0			ns
	tXL						
	tXH		fEX = 20.0MHz Fig.1, Fig.2 External clock drive	11			ns
	tXL						
Main clock base oscillation input rise time, fall time	tXR	EXTAL, XTAL	fEX = 40.0MHz Fig.1, Fig.2 External clock drive			8.5	ns
	tXF						
	tXR		fEX = 33.86MHz Fig.1, Fig.2 External clock drive			10.5	ns
	tXF						
	tXR		fEX = 20.0MHz Fig.1, Fig.2 External clock drive			14	ns
	tXF						
Main clock duty	duty	XTAL	Fig.1, Fig.2 1/2 VDD point	40	50	60	%

Note) tsys indicates the four values below according to the upper two bits (PCK1, PCK0) of the clock control register (CLC: 0002FEh).

$$t_{sys} [ns] = 2/f_{EX} \text{ (PCK1, PCK0 = 00)}, 4/f_{EX} \text{ (PCK1, PCK0 = 01)}, 8/f_{EX} \text{ (PCK1, PCK0 = 10)}, 16/f_{EX} \text{ (PCK1, PCK0 = 11)}$$

(2) Main clock multiplier circuit

(Topr = -30 to +85°C, VDD = 2.7 to 3.6 V, Vss = 0V reference)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Main clock multiplier frequency	fSRC	*1	22.0		40.5	MHz
		-20 to +85°C	19.9		40.5	
Lock-up time	tLOCK			1	5	ms

*1 When the degree of input frequency of the main clock base oscillation frequency fEX is 10.0 ± 0.1MHz, quadruple setting is 40.0 ± 0.4MHz.

Note) Main clock multiplier frequency fSRC generates the value set from 1.5 times to 4 times of the main clock base oscillation frequency fEX internally according to the Bits 10 to 8 (CMN2 to CMN0) of PLL setting register (PLL: 0002FCh).

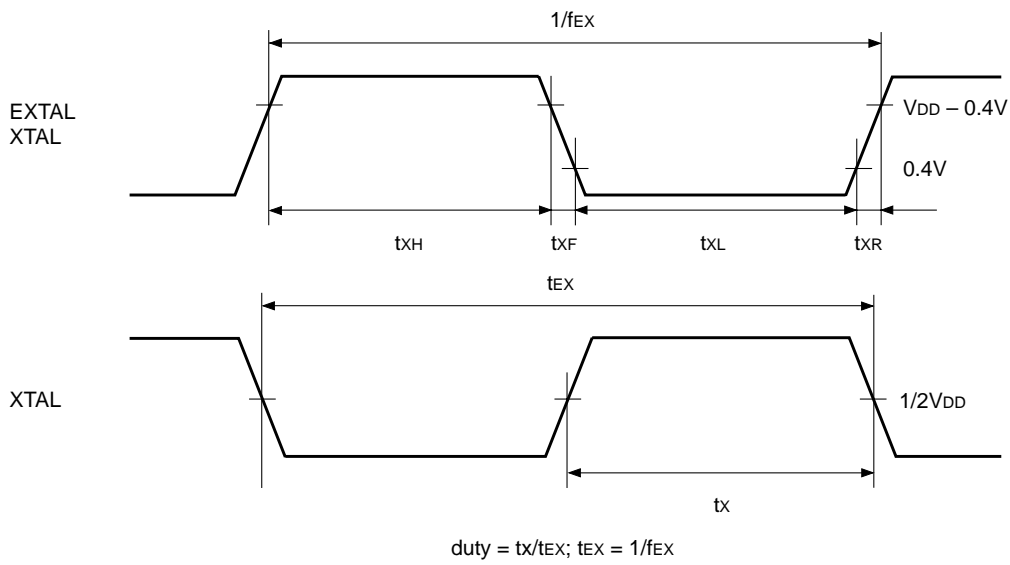


Fig. 1. Clock timing

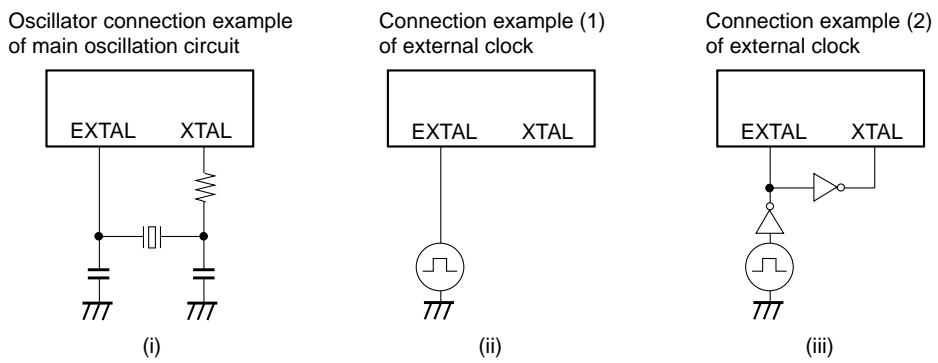


Fig. 2. Oscillator connection and clock applied conditions

(3) Event count input

(Topr = -30 to +85°C, VDD = 2.7 to 3.6V, VSS = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
Event count input clock pulse width	t _{EH} , t _{EL}	$\overline{EC0}$, $\overline{EC2}$	Fig. 3	t _{sys} + 100		ns

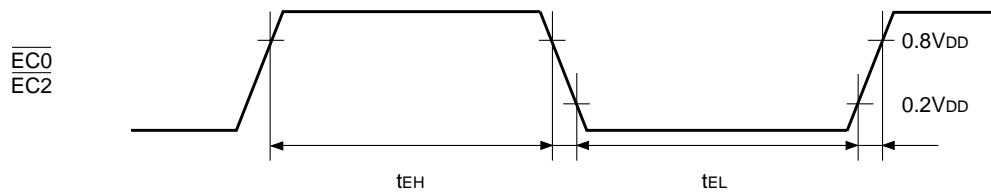


Fig. 3. Event count input timing

(4) Interruption and reset input

(Topr = -30 to +85°C, VDD = 2.7 to 3.6V, VSS = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption high, low level width	t _{IH} , t _{IL}	\overline{NMI} , INT0 to INT7, KS0 to KS19	Main mode Sleep mode Fig. 4	t _{sys} + 100		ns
			Noise filter selected Fig. 4			
		INT4 to INT7	PS4	32/f _{EX} + 100		
			PS6	128/f _{EX} + 100		
Reset input low level width	t _{RST}	\overline{RST}	Fig. 5	50/f _{EX}		ns

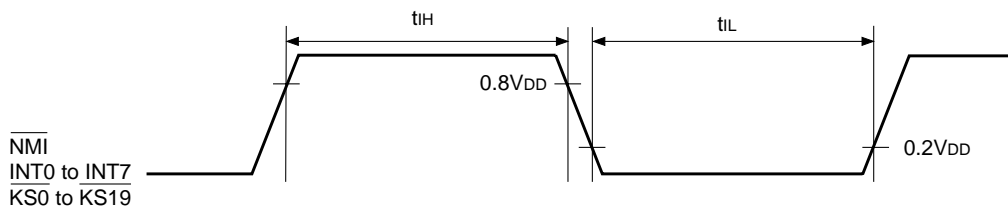


Fig. 4. Interruption input timing

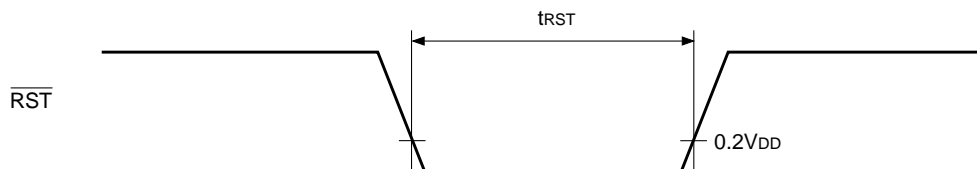


Fig. 5. Reset input timing

(5) A/D converter characteristics

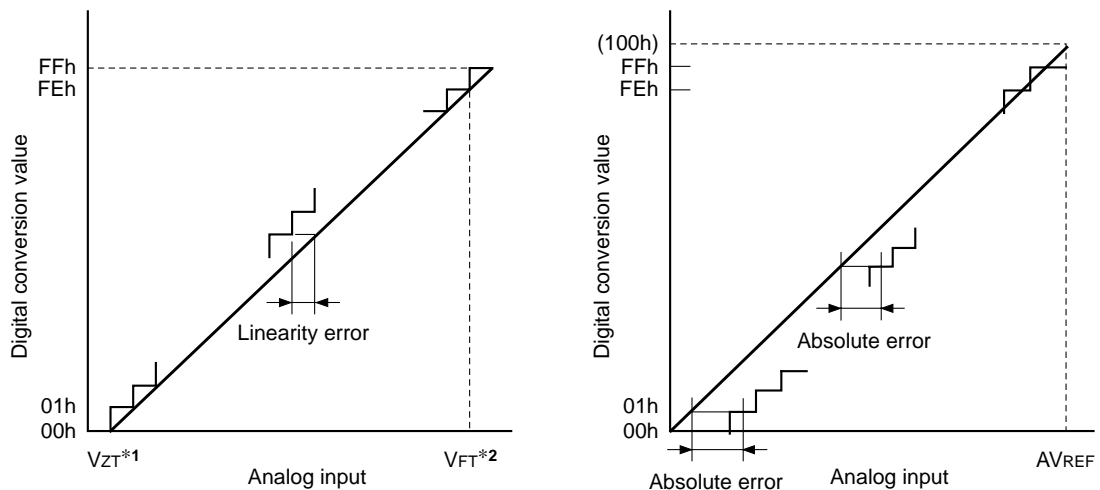
(Topr = -30 to +85°C, VDD = AVDD = AVREF = 2.7 to 3.6V, VSS = AVSS = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			VDD = AVDD = AVREF = 3.0V			±1	LSB
Absolute error						±3	LSB
Conversion time	tCONV			34tsys			ns
			*1	62tsys			ns
Sampling time	tSAMP			10tsys			ns
			*1	20tsys			ns
Reference input voltage	VREF	AVREF	VDD = AVDD = AVREF	2.7		3.6	V
Analog input voltage		AN0 to AN11		0		AVREF	V
AVREF current	IREF	AVREF	Main mode	VDD = 3.3 ± 0.3V fsRC = 40MHz	1.5	2.1	mA
				VDD = 3.3 ± 0.3V fsRC = 20MHz	1.2	1.7	mA
	IREFS		ADC off state*2 Stop mode			12	µA

*1 When Bit 6 (ADCK) of A/D control status register (ADCS: 000132h) is specified to "1".

*2 When Bit 5 (ADPC) of A/D control status register (ADCS: 000132h) is specified to "1".

Note) AVDD and AVREF must be the same voltage with VDD.



*1 VZT: Value at which the digital conversion value changes from 00h to 01h and vice versa.

*2 VFT: Value at which the digital conversion value changes from FEh to FFh and vice versa.

Fig. 6. Definition of A/D converter terms

(6) Serial transfer (CH0, CH1, CH2) (Topr = -30 to +85°C, VDD = 2.7 to 3.6V, VSS = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit		
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$, $\overline{SCK1}$, $\overline{SCK2}$	External start transfer mode (SCK = output mode)	VDD = 3.3 ± 0.3V		1.5tsys + 200	ns	
				VDD = 3.0 ± 0.3V		1.5tsys + 210	ns	
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ float delay time	t_{DSKF}	$\overline{SCK0}$, $\overline{SCK1}$, $\overline{SCK2}$		VDD = 3.3 ± 0.3V		1.5tsys + 200	ns	
				VDD = 3.0 ± 0.3V		1.5tsys + 210	ns	
$\overline{CS} \downarrow \rightarrow SO$ delay time	t_{DCSO}	SO0, SO1, SO2	External start transfer mode	VDD = 3.3 ± 0.3V		1.5tsys + 200	ns	
				VDD = 3.0 ± 0.3V		1.5tsys + 210	ns	
$\overline{CS} \uparrow \rightarrow SO$ float delay time	t_{DCSOF}	$\overline{SCS0}$, $\overline{SCS1}$, $\overline{SCS2}$		VDD = 3.3 ± 0.3V		1.5tsys + 200	ns	
				VDD = 3.0 ± 0.3V		1.5tsys + 210	ns	
\overline{CS} high level width	t_{WHCS}	$\overline{SCS0}$, $\overline{SCS1}$, $\overline{SCS2}$	External start transfer mode	VDD = 3.3 ± 0.3V	tsys + 100		ns	
				VDD = 3.0 ± 0.3V	tsys + 110		ns	
\overline{SCK} cycle time	t_{KCY}	$\overline{SCK0}$, $\overline{SCK1}$, $\overline{SCK2}$		Input mode	VDD = 3.3 ± 0.3V	2tsys + 200		ns
					VDD = 3.0 ± 0.3V	2tsys + 210		ns
			Output mode	VDD = 3.3 ± 0.3V	16/fEX		ns	
				VDD = 3.0 ± 0.3V	16/fEX		ns	
\overline{SCK} high, low pulse width	t_{KH} , t_{KL}	$\overline{SCK0}$, $\overline{SCK1}$, $\overline{SCK2}$	Input mode	VDD = 3.3 ± 0.3V	tsys + 100		ns	
				VDD = 3.0 ± 0.3V	tsys + 110		ns	
			Output mode	VDD = 3.3 ± 0.3V	8/fEX - 100		ns	
				VDD = 3.0 ± 0.3V	8/fEX - 110		ns	
SI input data setup time (for $\overline{SCK} \uparrow$)	t_{SIK}	SI0, SI1, SI2	\overline{SCK} input mode	VDD = 3.3 ± 0.3V	100		ns	
				VDD = 3.0 ± 0.3V	110		ns	
			\overline{SCK} output mode	VDD = 3.3 ± 0.3V	200		ns	
				VDD = 3.0 ± 0.3V	210		ns	
SI input data hold time (for $\overline{SCK} \uparrow$)	t_{KSI}	SI0, SI1, SI2	\overline{SCK} input mode	VDD = 3.3 ± 0.3V	2tsys + 100		ns	
				VDD = 3.0 ± 0.3V	2tsys + 110		ns	
			\overline{SCK} output mode	VDD = 3.3 ± 0.3V	100		ns	
				VDD = 3.0 ± 0.3V	110		ns	
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t_{KSO}	SO0, SO1, SO2	\overline{SCK} input mode	VDD = 3.3 ± 0.3V		2tsys + 150	ns	
				VDD = 3.0 ± 0.3V		2tsys + 160	ns	
			\overline{SCK} output mode	VDD = 3.3 ± 0.3V		100	ns	
				VDD = 3.0 ± 0.3V		110	ns	
Minimum interval time	t_{INT}	$\overline{SCK0}$, $\overline{SCK1}$, $\overline{SCK2}$	\overline{SCK} input mode	VDD = 3.3 ± 0.3V	3tsys + 100		ns	
				VDD = 3.0 ± 0.3V	3tsys + 110		ns	
			\overline{SCK} output mode	VDD = 3.3 ± 0.3V	8/fEX - 100		ns	
				VDD = 3.0 ± 0.3V	8/fEX - 110		ns	

Note) The load condition for the \overline{SCK} output mode and SO output delay time is 100pF.

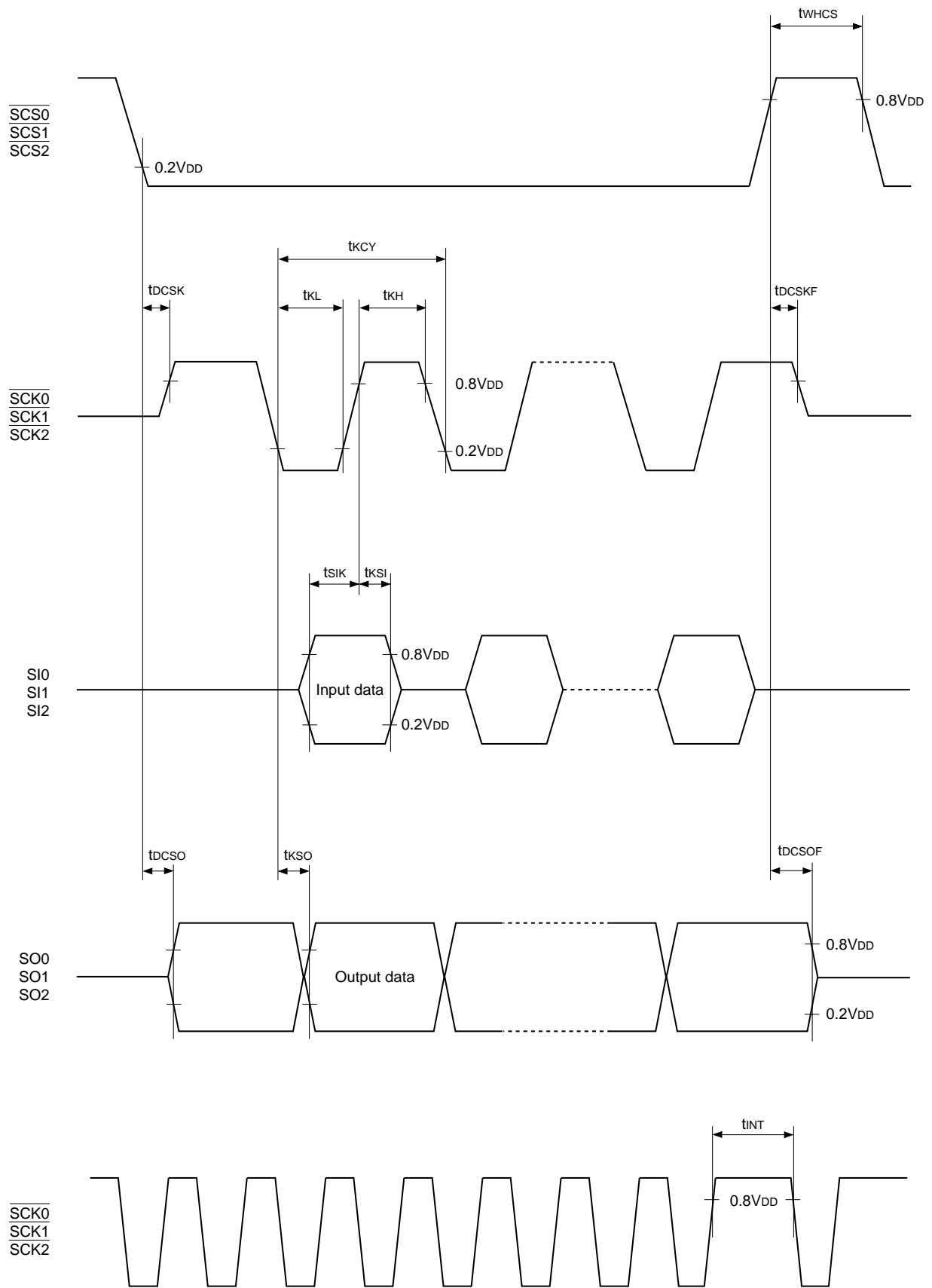


Fig. 7. Serial transfer CH0, CH1, CH2 timing

(7) I²C bus

(Topr = -30 to +85°C, V_{DD} = 2.7 to 3.6V, V_{SS} = 0V reference)

Item	Symbol	Pins	Standard mode		High-speed mode		Unit
			Min.	Max.	Min.	Max.	
SCK clock frequency	t _{SCL}	SCL		100		400	kHz
Bus free time between stop and start conditions	t _{BUF}	SDA	4.7		1.3		μs
Hold time under (resend) start condition	t _{HD;STA}	SDA, SCL	4.0		0.6		μs
Hold time in SCL clock low state	t _{Low}	SCL	4.7		1.3		μs
Hold time in SCL clock high state	t _{High}	SCL	4.0		0.6		μs
Setup time under (resend) start condition	t _{SU;STA}	SDA, SCL	4.7		0.6		μs
Data hold time	t _{HD;DAT}	SDA, SCL	0		0	0.9	μs
Data setup time	t _{SU;DAT}	SDA, SCL	250		100		ns
SCL, SDA signal output rise time	t _{Rd} , t _{Rc}	SDA, SCL		1000	20 + α*1	300	ns
SCL, SDA signal output fall time	t _{Fd} , t _{Fc}	SDA, SCL		300	20 + α*1	300	ns
Setup time under stop condition	t _{SU;STO}	SDA, SCL	4.0		0.6		μs

*1 Due to the total capacitance of the bus.

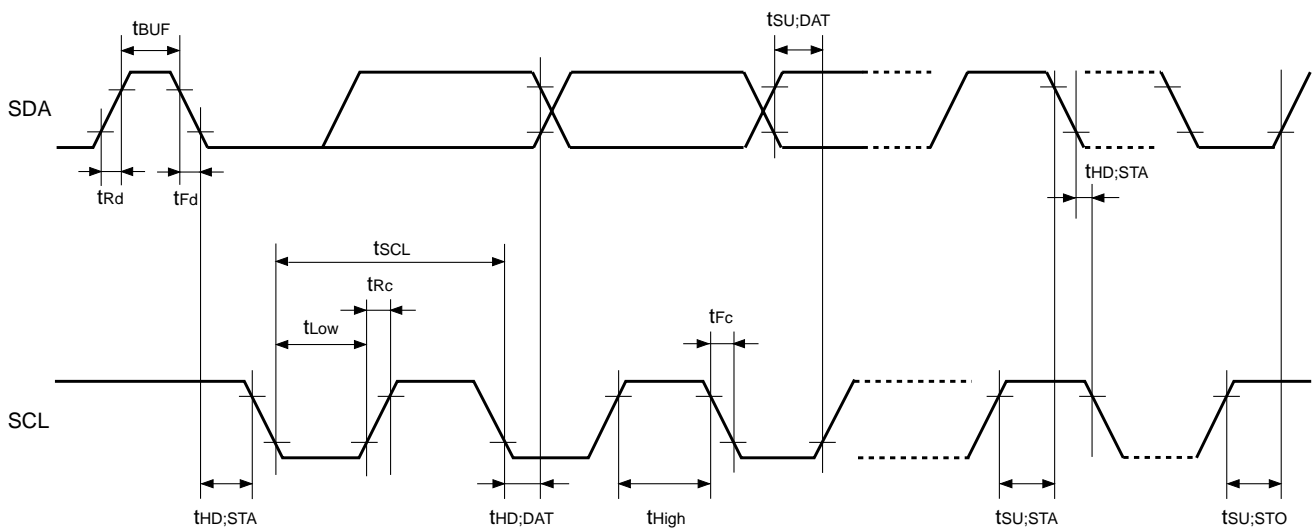


Fig. 8. I²C bus timing

(8) Remote control reception

(Topr = -30 to +85°C, V_{DD} = 2.7 to 3.6V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Typ.	Max.	Unit	
Remote control receive high, low level width	t _{RMC}	RMC	Main mode	PS5 selected		ns	
				PS7 selected	128/f _{EX} + 100		
				PS9 selected	512/f _{EX} + 100		2048/f _{EX} + 100

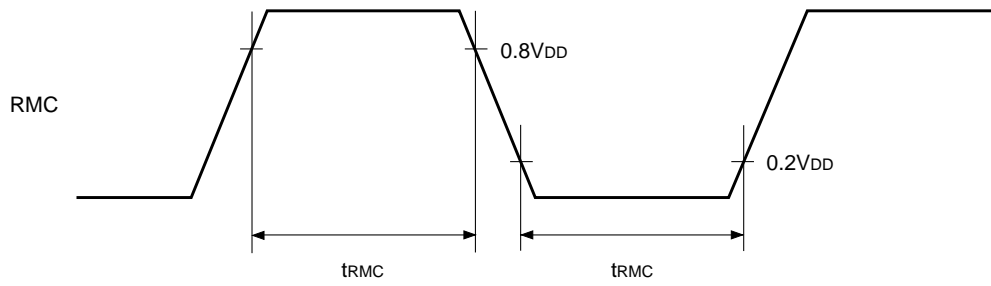


Fig. 9. Remote control signal input timing

(9) External register interface

(V_{SS} = 0V reference)

Item	Symbol	3.3 ± 0.3V T _{opr} = -20 to +75°C		3.3 ± 0.3V T _{opr} = -30 to +85°C		3.0 ± 0.3V T _{opr} = -30 to +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Chip select pulse width 1	t _{CS1}	1.5t _{sys} -20	1.5t _{sys}	1.5t _{sys} -20	1.5t _{sys}	1.5t _{sys} -30	1.5t _{sys}	ns
Chip select pulse width 2	t _{CS2}	2.5t _{sys} -20	16.5t _{sys}	2.5t _{sys} -20	16.5t _{sys}	2.5t _{sys} -30	16.5t _{sys}	ns
Chip select pulse width 3	t _{CS3}	2.5t _{sys} -20	32.5t _{sys}	2.5t _{sys} -20	32.5t _{sys}	2.5t _{sys} -30	32.5t _{sys}	ns
Chip select pulse width 4	t _{CS4}	3.5t _{sys} -20	33.5t _{sys}	3.5t _{sys} -20	33.5t _{sys}	3.5t _{sys} -30	33.5t _{sys}	ns
Chip select pulse width 5	t _{CS5}	2.5t _{sys} -20	17.5t _{sys}	2.5t _{sys} -20	17.5t _{sys}	2.5t _{sys} -30	17.5t _{sys}	ns
Chip select pulse width 6	t _{CS6}	3.5t _{sys} -20	18.5t _{sys}	3.5t _{sys} -20	18.5t _{sys}	3.5t _{sys} -30	18.5t _{sys}	ns
Chip select pulse width 7	t _{CS7}	4.5t _{sys} -20	34.5t _{sys}	4.5t _{sys} -20	34.5t _{sys}	4.5t _{sys} -30	34.5t _{sys}	ns
Read/write strobe pulse width 1	t _{RW1}	t _{sys} - 25	t _{sys}	t _{sys} - 25	t _{sys}	t _{sys} - 35	t _{sys}	ns
Read/write strobe pulse width 2	t _{RW2}	2t _{sys} - 25	16t _{sys}	2t _{sys} - 25	16t _{sys}	2t _{sys} - 35	16t _{sys}	ns
Read/write strobe pulse width 3	t _{RW3}	2t _{sys} - 25	32t _{sys}	2t _{sys} - 25	32t _{sys}	2t _{sys} - 35	32t _{sys}	ns
Address setting time 1	t _{AS1}	t _{sys} /2 -25	t _{sys} /2	t _{sys} /2 -25	t _{sys} /2	t _{sys} /2 -35	t _{sys} /2	ns
Address setting time 2	t _{AS2}	1.5t _{sys} -25	1.5t _{sys}	1.5t _{sys} -25	1.5t _{sys}	1.5t _{sys} -35	1.5t _{sys}	ns
Address hold time	t _{AH}	t _{sys} /2 -25	—	t _{sys} /2 -25	—	t _{sys} /2 -35	—	ns
Read data setting request time	t _{DS1}	15	—	15	—	20	—	ns
Read data hold request time	t _{DH1}	0	—	0	—	0	—	ns
Write data setting time 1	t _{DS2}	1.5t _{sys} -25	1.5t _{sys}	1.5t _{sys} -25	1.5t _{sys}	1.5t _{sys} -35	1.5t _{sys}	ns
Write data setting time 2	t _{DS3}	2.5t _{sys} -25	16.5t _{sys}	2.5t _{sys} -25	16.5t _{sys}	2.5t _{sys} -35	16.5t _{sys}	ns
Write data hold time	t _{DH2}	t _{sys} /2 -25	t _{sys} /2 +30	t _{sys} /2 -25	t _{sys} /2 +30	t _{sys} /2 -35	t _{sys} /2 +30	ns

Read Timing

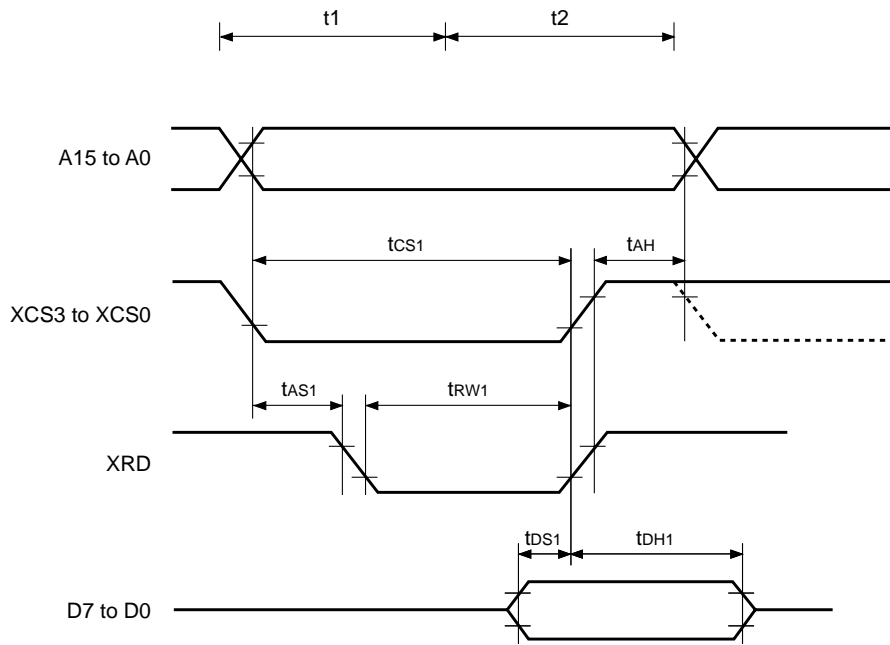


Fig. 10. Byte read (without programmable wait)

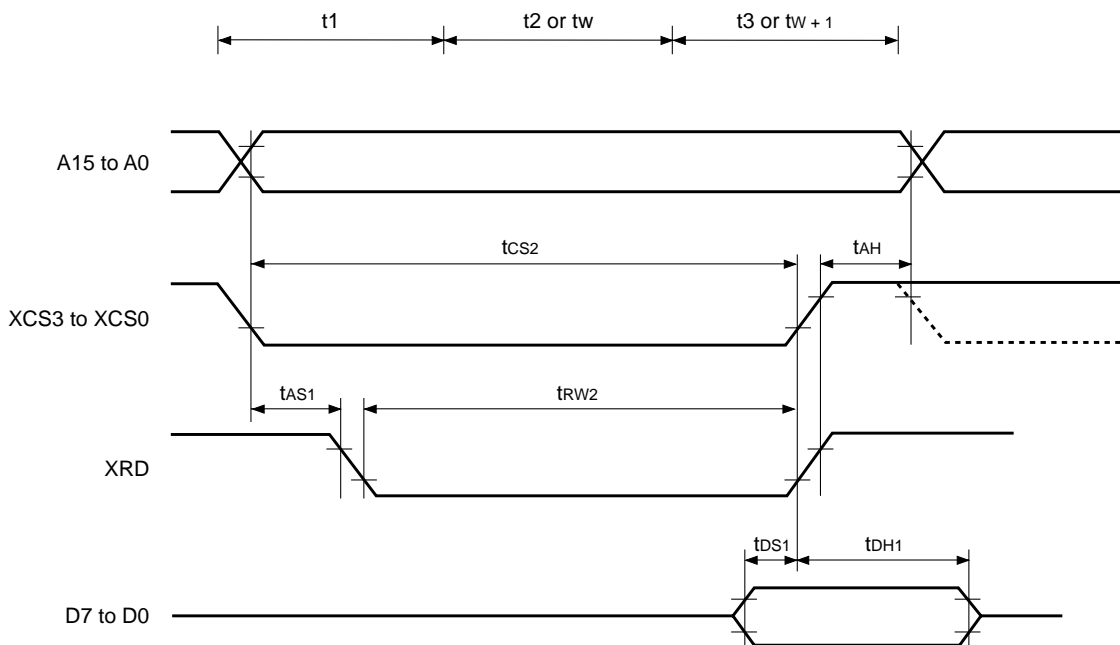


Fig. 11. Byte read (with programmable wait)

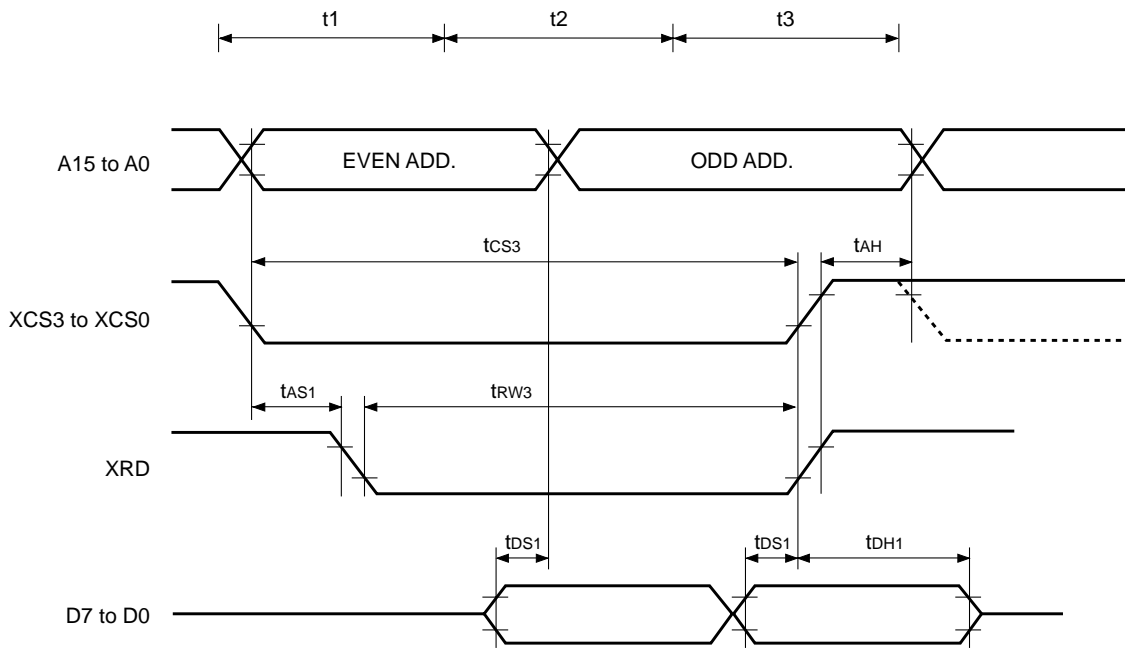


Fig. 12. Word read (no strobe mode, without programmable wait)

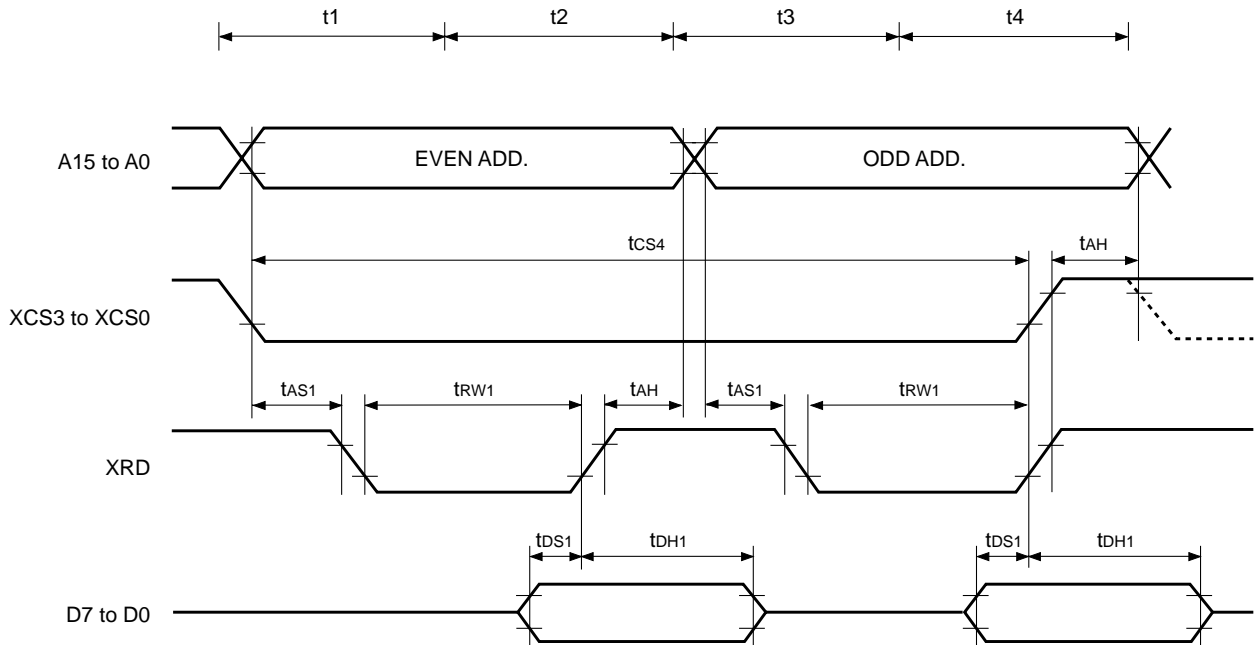


Fig. 13. Word read (strobe mode, without programmable wait)

Write Timing

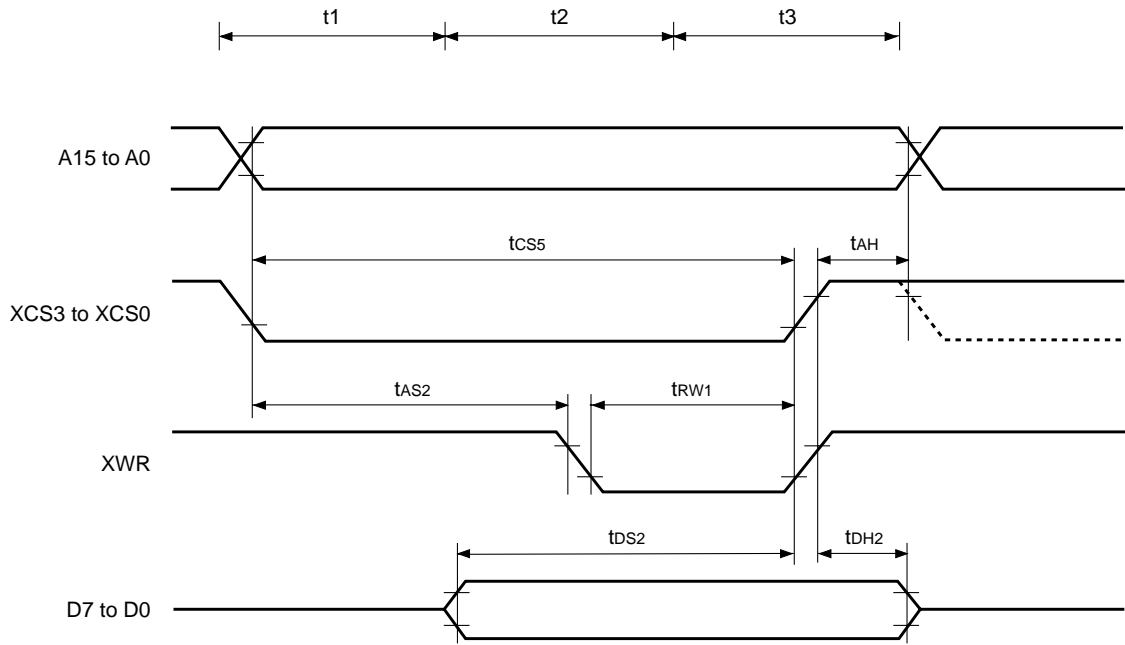


Fig. 14. Byte write (without programmable wait)

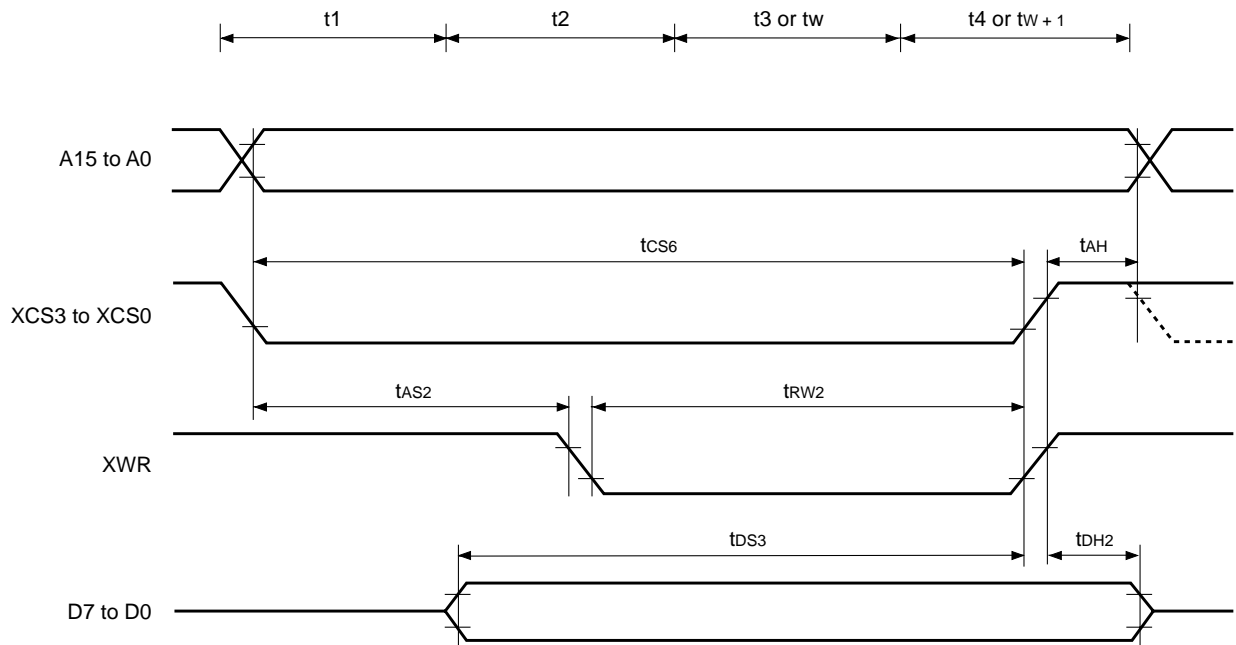


Fig. 15. Byte write (with programmable wait)

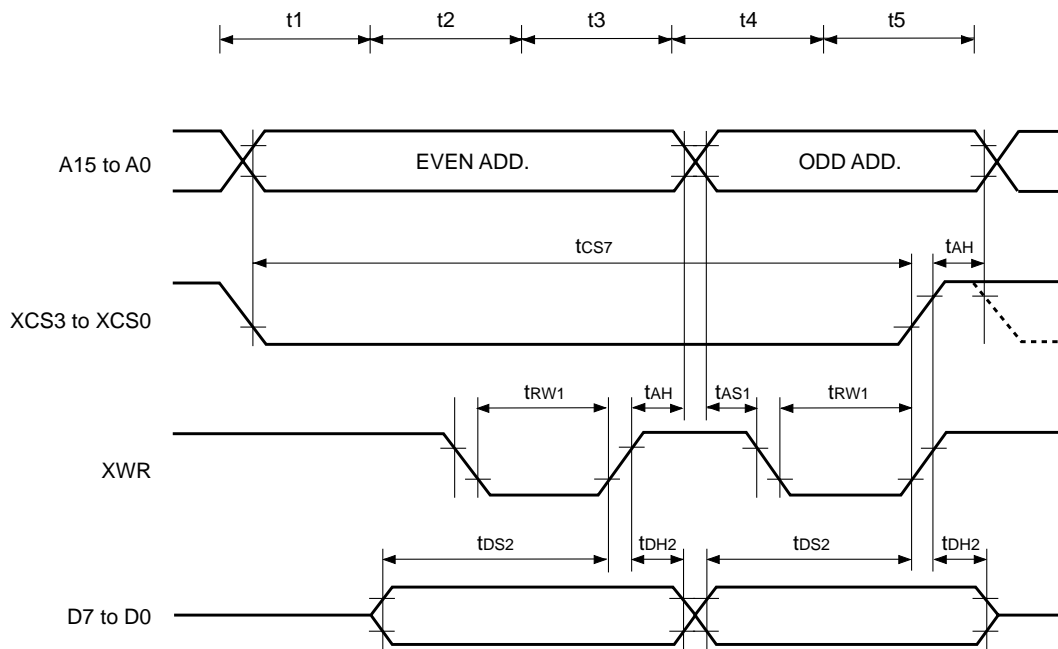


Fig. 16. Word write (without programmable wait)

Appendix

SPC970 Series recommended oscillation circuit and oscillator

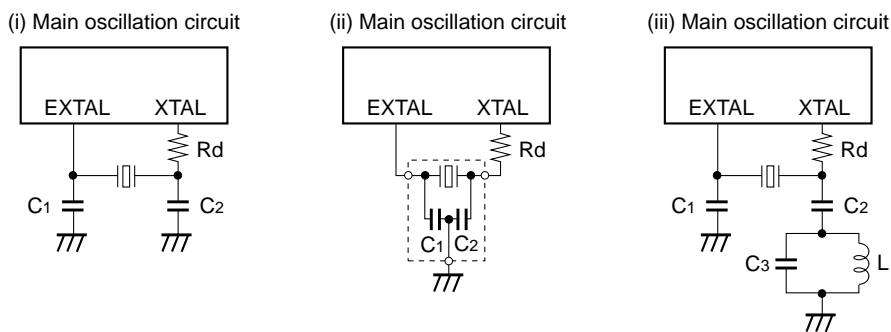


Fig. 17. Recommended oscillation circuit

Manufacturer	Model	fEX (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example	Remarks
MURATA MFG CO., LTD.	CSA6.00MG040	6.0	100	100	0	(i)	
	CSA8.00MTZ	8.0	30	30	0		
	CSA10.0MTZ	10.0	30	30	0		
	CSA12.0MTZ	12.0	30	30	0		
	CSA16.00MXZ040	16.0	15	15	0		
	CSA20.00MXZ040	20.0	10	10	0		
	CSA24.00MXZ040	24.0	7	7	0		
MURATA MFG CO., LTD.	CST6.00MGW040*	6.0	100	100	0	(ii)	
	CST8.00MTW*	8.0	30	30	0		
	CST10.0MTW*	10.0	30	30	0		
	CST12.0MTW*	12.0	30	30	0		
	CST16.00MXW0C3*	16.0	15	15	0		
RIVER ELETEC CO., LTD.	HC-49/U03	6.0	18	18	560	(i)	CL = 13.5pF
		8.0	15	15	330		CL = 12pF
		10.0	10	10	330		CL = 9.5pF
		12.0	10	10	220		CL = 10pF

* Indicates types with on-chip grounding capacitor (C1, C2).

CL: Load capacitor

Manufacturer	Model	f _{EX} (MHz)	C ₁ (pF)	C ₂ (pF)	R _d (Ω)	Circuit example	Remarks
KINSEKI LTD.	HC-49/U-S	6.0	15	15	5.6k	(i)	CL = 16pF
		8.0	15	15	3.0k		
		10.0	10	10	1.8k		
		12.0	12	12	1.0k		
		16.0	12	12	470		
		20.0	12	12	390		
		24.0	12	12	200		
	28.0	1	1	100	(iii)	C3 = 10pF, L = 2.7μH	
	HC-49/U	32.0	3	0.01μF		0	C3 = 5pF, L = 2.7μH
		36.0	3	0.01μF		0	C3 = 3pF, L = 3.3μH
TDK Corporation	CCR6.0MC5*	6.0	36 (±20%)	36 (±20%)	0	(ii)	
	CCR12.0MSC5*	12.0	20 (±20%)	20 (±20%)	0		
	CCR16.0MSC6*	16.0	10 (±20%)	10 (±20%)	0		
	CCR28.0MSC6*	28.0	10 (±20%)	10 (±20%)	0		
	CCR40.0MS6	40.0	5	5	0	(i)	

* Indicates types with on-chip grounding capacitor (C₁, C₂).

CCR***: Surface mounted type ceramic oscillator

CL: Load capacitor

Product List

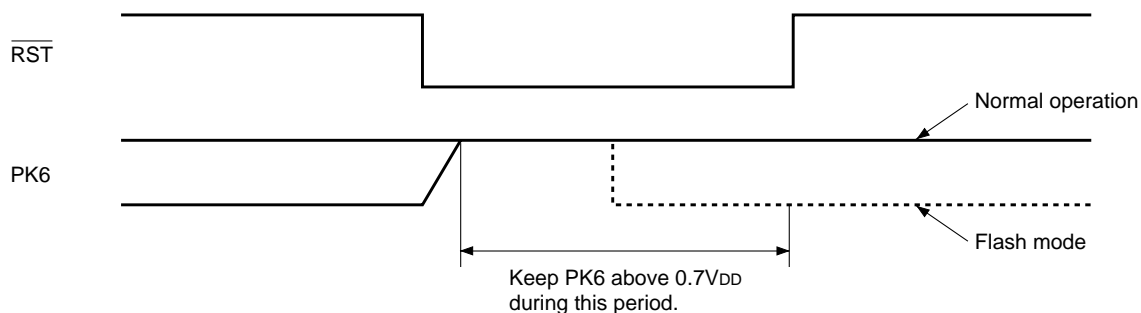
Type	Mask ROM		
Product name	CXP973064	CXP973032	CXP972032
ROM capacitance	256K byte	128K byte	128K byte
RAM capacitance	11.5K byte	11.5K byte	7.5K byte
Package	100-pin plastic QFP, 100-pin plastic LQFP, 104-pin plastic LFLGA	100-pin plastic QFP, 100-pin plastic LQFP	
Main clock base oscillation frequency*1	Less than 40MHz, Less than 20MHz		
Reset pin pull-up resistor	Existent/Non-existent		

*1 When the main clock base oscillation frequency is specified below 20MHz, operation is not performed even though higher external oscillation and higher external input frequency than the upper limit of clock timing specification are applied.

Notes on PK6 Usage

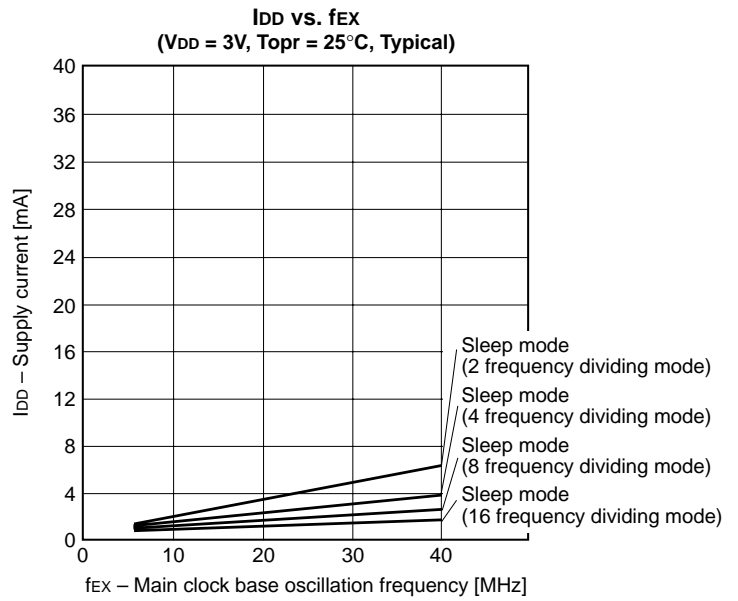
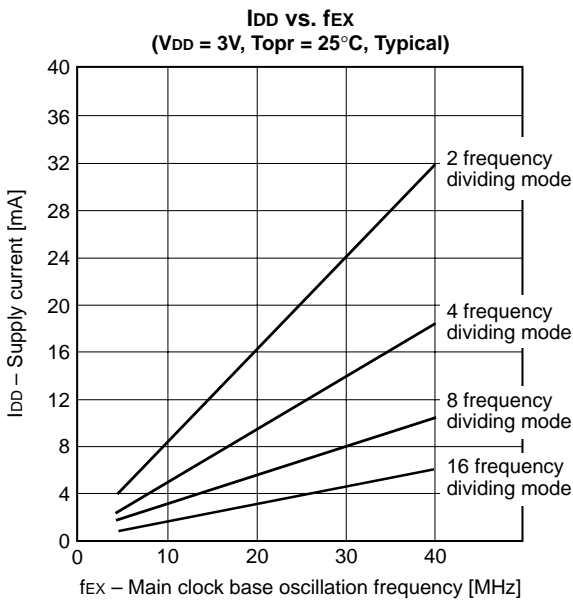
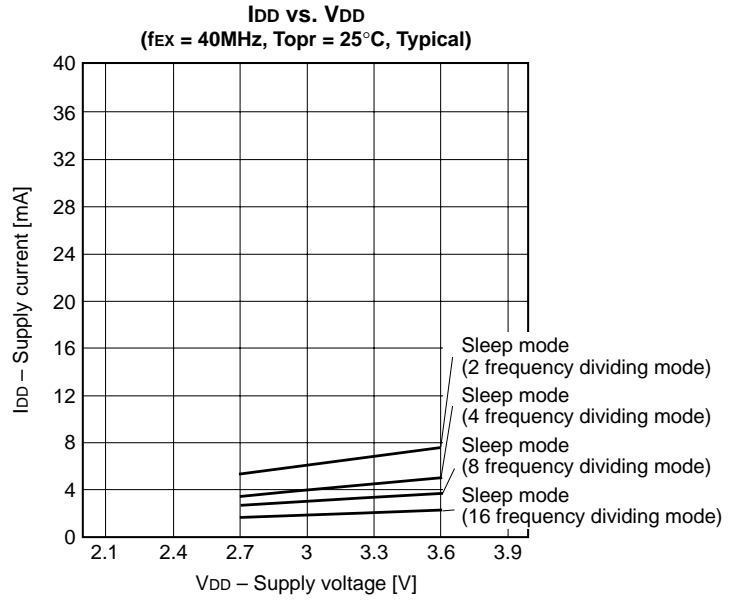
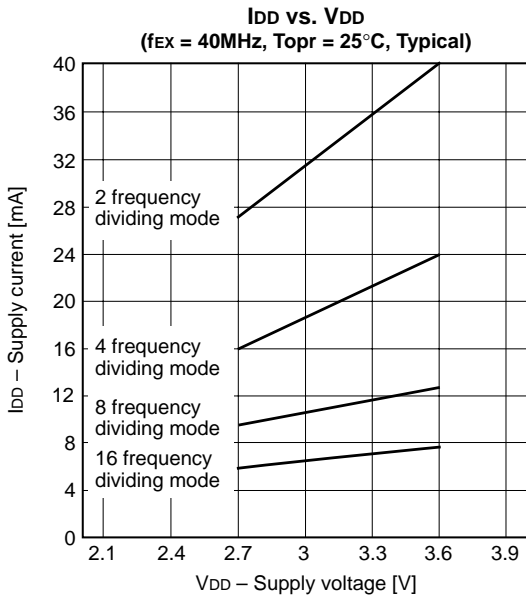
FLASH EEPROM incorporated PK6 is also used as flash mode setting function. Note the followings:

1. "H" is output to PK6 during a reset. That is driven at comparatively high impedance (approximately 150k Ω), and take care that V_{OH} should not fall under $0.7V_{DD}$ by the partial pressure with external circuit load impedance.
2. When using software reset functions, PK6 may not rise enough during a reset. Switching PK6 to "H" output prior to software reset execution or connecting pull-up resistor is recommended.

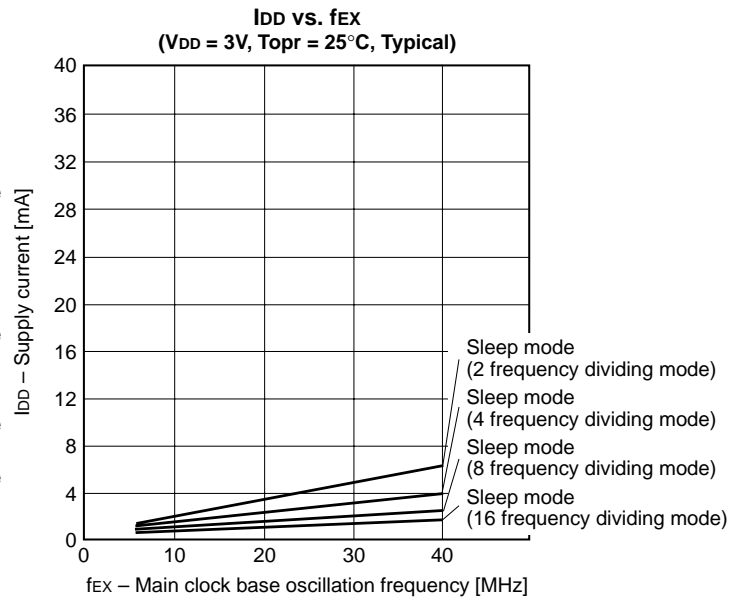
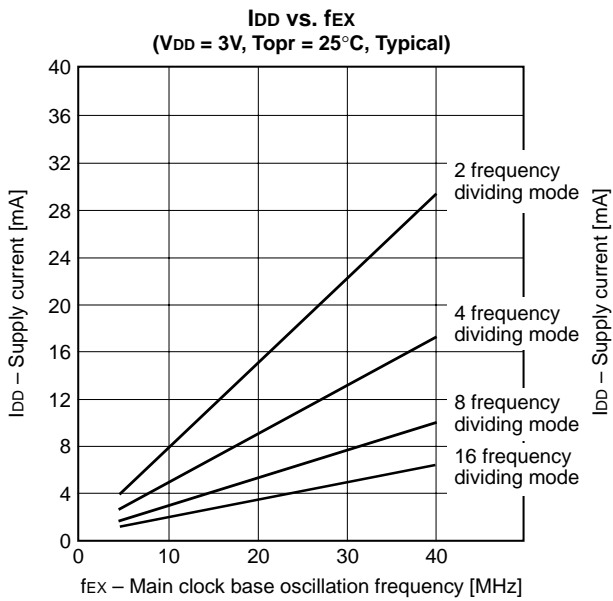
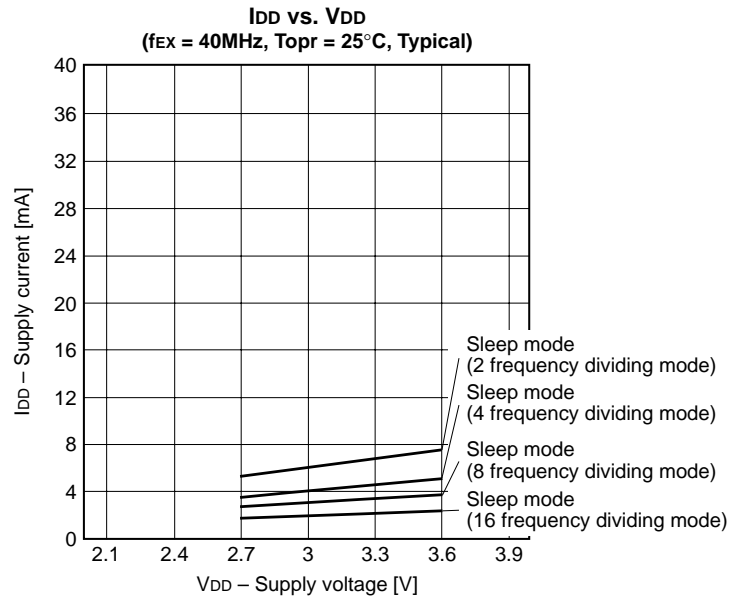
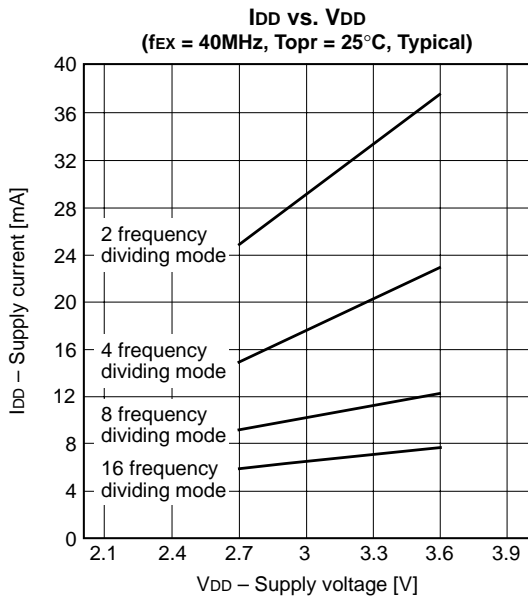


Mask ROM and piggy/evaluation chip do not have flash mode setting function. Considering that FLASH EEPROM incorporated version is used, above countermeasure should be performed.

Characteristics Curve (CXP973032/973064)



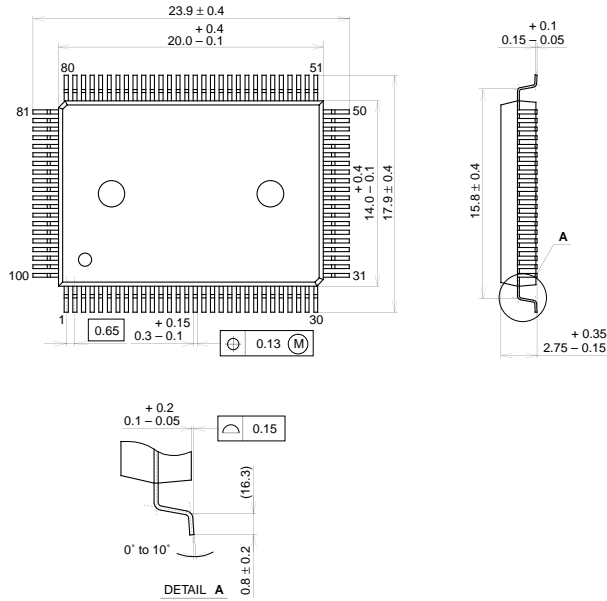
Characteristics Curve (CXP972032)



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

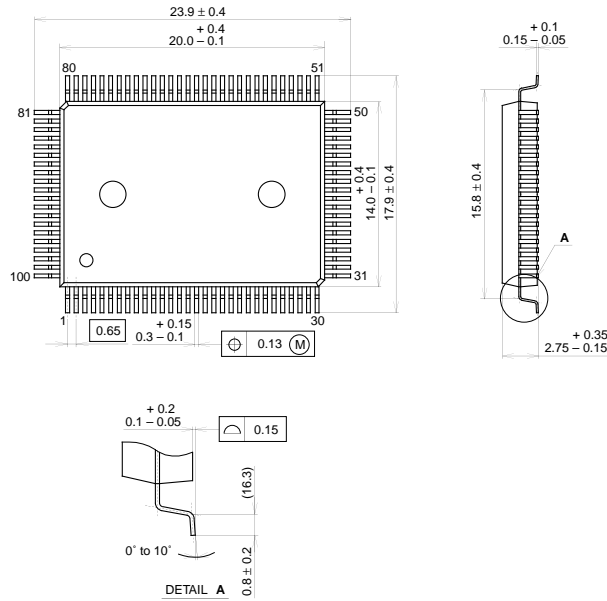


PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

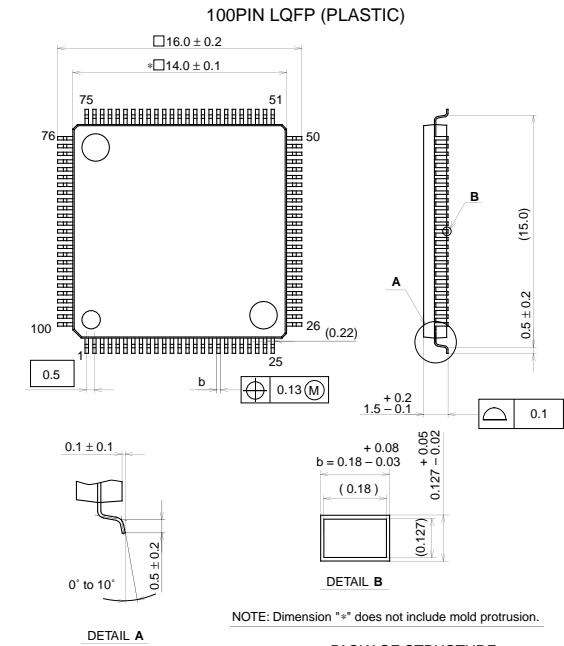
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm

Package Outline

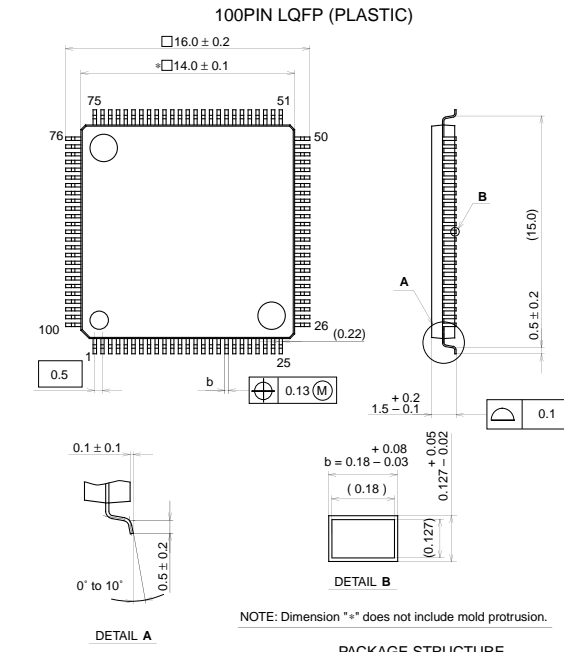
Unit: mm



SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	_____

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g



SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	_____

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g

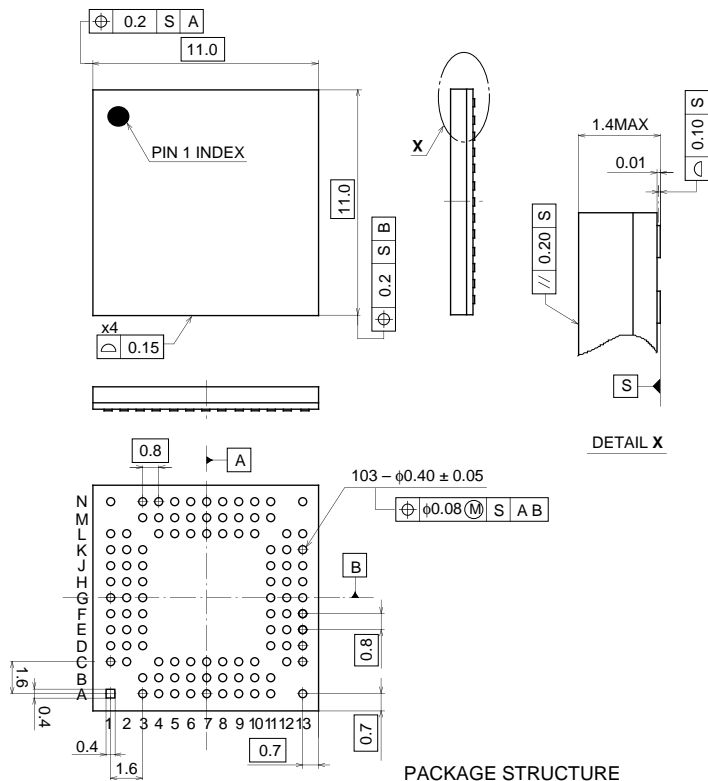
LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm

Package Outline

Unit: mm

104PIN LFLGA



PACKAGE STRUCTURE

SONY CODE	LFLGA-104P-01
EIAJ CODE	P-LFLGA104-11x11-0.8
JEDEC CODE	—

PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	GOLD PLATING
TERMINAL MATERIAL	NICKEL PLATING
PACKAGE MASS	0.3g