ESS Technology, Inc.

ES4428/ES4427
Web/DVD Set-Top Box Solution
Product Brief

DESCRIPTION

The ES4428/ES4427 Web/DVD Internet set-top box chipset seamlessly combines both Web browser technology and DVD technology into a highly integrated, low-cost solution for the next generation of Internet set-top boxes for home use.

The ES4428, which is based on ESS's Programmable Multimedia Processor (PMP) device architecture, includes a programmable internal RISC processor core that makes it adaptable for use in embedded systems applications such as set-top boxes. The ES4427 companion chip supplies proper video sync capabilities and performs NTSC- and PAL-based video encoding and decoding as necessary to provide broadcast quality video to the television screen.

The ES4428 DVD processor integrates MPEG-based audio and video data stream decoding for DVD/VCD/SuperVCD playback, DVD system navigation and Dolby AC-3 decoding into a single device. The ES4428 demuxes the incoming DVD audio and video data streams from the DVD loader using its glueless 8/16-bit parallel interface, which is hardware-compatible with many DVD loaders. The ES4428 also supports both 8- and 16-bit Flash/Read-Only Memory (ROM) and 8- and 16-bit Synchronous DRAM (SDRAM) memory I/O operations.

The ES4428 controls data I/O transactions to and from the ES4427 companion chip through its 8-bit Device Serial Connect (DSC) parallel bus interface. The ES4428 also provides a 16-bit wide hardware interface with V.90-compatible modem subsystems incorporated into the set-top box design.

The ES4427 incorporates a multi-standard TV encoder that supports both the NTSC and PAL formats and CCIR-601 non-square operations. Two microphone ADCs and PLL clock synthesizers are incorporated in the ES4427 device architecture. The ES4427 includes an I/O-mapped auxiliary expansion port that interfaces with the ES4428. Four pins of the port can be configured as edge-triggered interrupts, supporting critical functions, such as handling remote control and modem interrupt requests, DVD/VCD loader resets and modem board resets.

Command and register accesses are issued through the DSC interface from the ES4428 DVD processor to the ES4427 through the device serial communication (DSC) interface for accessing the internal registers of the ES4427. The DSC interface port is comprised of three interface signals, the strobe (DSC_S), data (DSC_D), and clock (DSC_C).

The DSC port is selected when the DSC strobe goes high and latches the data at the rising edge of the clock. Each 16-bit DSC transfer is comprised of an address followed by data.

The ES4428 is available in an industry-standard 208-pin Plastic Quad Flat Pack (PQFP) package, while the ES4427 is available in an industry-standard 100-pin PQFP package.

ES4428 FEATURES

- On-chip hardware interface with V.90 data/fax/voice modem subsystem implemented
- 640 x 480 NTSC and 640 x 576 PAL television video formats supported
- Configurable for browser/DVD applications
- Hardware support for infrared remote control and/or wireless keyboard
- On-chip MPEG audio/video decoder and system parser
- On-chip on-screen display (OSD) controller supports 4-bit blending.
- On-chip subpicture unit (SPU) decoder supports karaoke lyric, subtitle and closed captioning functions.
- VideoCD 1.1 and 2.0, Interactive 3.0, Super VCD and Audio CD compatibility available with Video CD / Super VCD player configuration
- VideoCD 1.1 and 2.0, Interactive 3.0, Super VCD, Audio CD and MP3 compatibility available with Super VCD / DVD player configuration
- DTS audio decoding supported
- Programmable multimedia processor architecture
- ISO/IEC 13818-2 MPEG-2 compliant
- ISO/IEC 11172 MPEG-1 compliant

ES4427 FEATURES

- 8-bit DSC parallel bus interface generates edge-triggered interupts for data read/write interfacing with ES4428
- Dual microphone and vocal assist hardware support provided
- PLL clock synthesizer based on 27 MHz crystal input generates required clocks for video encoder, video DACs and video processor

SOFTWARE SUPPORT

- Software stack support for the POP3, SMTP and SNMP Internet e-mail protocols defined by RFC 821, RFC 1157and RFC 2449
- Software stack support provided for the HTTP Web browsing protocol defined by RFC 1945, RFC 2068 and RFC 2616
- Software stack support provided for the TCP/IP Internet protocols defined by RFC 791 and RFC 793
- Software stack support provided for RTP payload format for MPEG-1/2 and H.261 video streaming protocols defined by RFC 2032, RFC 2038 and RFC 2250
- Software support for HTML 1.0, 2.0 and 3.2, *.aiff, *.au and *.wav audio file formats and *.gif, *.jpg and *.xbm graphic file formats, JavaScript 1.1, SSL 2.0 and SSL 3.0
- Character generation and software support for English, Big 5/GB Chinese and Japanese fonts
- Software support for infrared remote control and wireless keyboard

ES4428 PINOUT

Figure 1 shows the ES4428 device pinout.

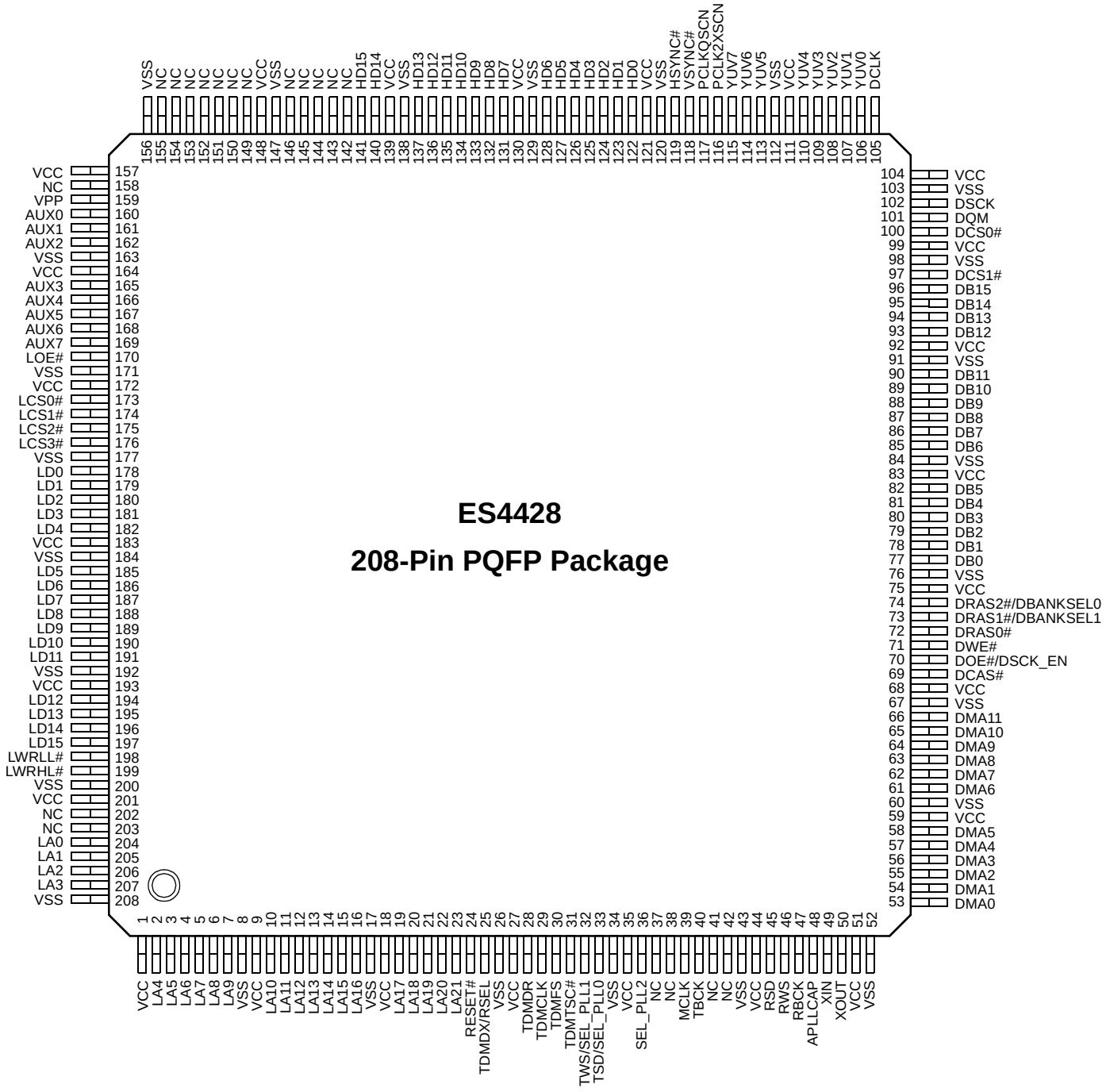


Figure 1 ES4428 Device Pinout

ES4428 PIN DESCRIPTION

Table 1 lists the pin descriptions for the ES4428.

Table 1 ES4428 Pin Descriptions

<table>
<tr><th>Name</th><th>Number</th><th>I/O</th><th>Definition</th></tr>
<tr><td>VCC</td><td>1, 9, 18, 27, 35, 44, 51, 59, 68, 75, 83, 92, 99, 104, 111, 121, 130, 139, 148, 157, 164, 172, 183, 193, 201</td><td>I</td><td>3.3V power supply.</td></tr>
<tr><td>VSS</td><td>8, 17, 26, 34, 43, 52, 60, 67, 76, 84, 91, 98, 103, 112, 120, 129, 138, 147, 156, 163, 171, 177, 184, 192, 200, 208</td><td>I</td><td>Ground.</td></tr>
<tr><td>LA[21:0]</td><td>23:19,16:10,7:2,207:204</td><td>O</td><td>Device address output.</td></tr>
<tr><td>RESET#</td><td>24</td><td>I</td><td>Reset.</td></tr>
<tr><td>TDMDX</td><td rowspan="2">25</td><td>O</td><td>TDM transmit data output.</td></tr>
<tr><td>RSEL</td><td>I</td><td>ROM Select.
<table>
<tr><th>RSEL</th><th>Selection</th></tr>
<tr><td>0</td><td>16-bit ROM</td></tr>
<tr><td>1</td><td>8-bit ROM</td></tr>
</table></td></tr>
<tr><td>TDMDR</td><td>28</td><td>I</td><td>TDM receive data input.</td></tr>
<tr><td>TDMCLK</td><td>29</td><td>I</td><td>TDM clock input.</td></tr>
<tr><td>TDMFS</td><td>30</td><td>I</td><td>TDM frame sync.</td></tr>
<tr><td>TDMTSC#</td><td>31</td><td>O</td><td>TDM output enable.</td></tr>
<tr><td>TWS</td><td rowspan="2">32</td><td>O</td><td>Audio transmit frame sync output.</td></tr>
<tr><td>SEL_PLL1</td><td></td><td>System and DSCK output clock frequency selection at reset time. The matrix below lists the available clock frequencies and their respective PLL bit settings..
<table>
<tr><th>SEL_PLL2</th><th>SEL_PLL1</th><th>SEL_PLL0</th><th>Clock Output</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>VCO doesn’t work.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>27 MHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Bypass mode</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>54 MHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>121.5 MHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>81 MHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>94.5 MHz</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>108 MHz</td></tr>
</table></td></tr>
<tr><td>TSD</td><td rowspan="2">33</td><td>O</td><td>Audio transmit serial data output.</td></tr>
<tr><td>SEL_PLL0</td><td>I</td><td>Refer to the description and matrix for SEL_PLL1 pin 32.</td></tr>
<tr><td>SEL_PLL2</td><td>36</td><td>I</td><td>Refer to the description and matrix for SEL_PLL1 pin 32.</td></tr>
<tr><td>NC</td><td>37, 38, 41, 42, 146:142, 155:149, 158, 203:202</td><td>—</td><td>No connect. Leave open.</td></tr>
<tr><td>MCLK</td><td>39</td><td>I/O</td><td>Audio master clock for audio DAC.</td></tr>
<tr><td>TBCK</td><td>40</td><td>I/O</td><td>Audio transmit bit clock output.</td></tr>
<tr><td>RSD</td><td>45</td><td>I</td><td>Audio receive serial data input.</td></tr>
<tr><td>RWS</td><td>46</td><td>I</td><td>Audio receive frame sync input.</td></tr>
<tr><td>RBCK</td><td>47</td><td>I</td><td>Audio receive bit clock input.</td></tr>
<tr><td>APLLCAP</td><td>48</td><td>I</td><td>Analog PLL capacitor input.</td></tr>
</table>

Table 1 ES4428 Pin Descriptions (Continued)

Name	Number	I/O	Definition
XIN	49	I	Crystal input.
XOUT	50	O	Crystal output.
DMA[11:0]	66:61, 58:53	O	DRAM address bus [11:0].
DCAS#	69	O	DRAM column address strobe.
DOE#	70	O	DRAM output enable.
DSCK_EN		O	DRAM clock enable.
DWE#	71	O	DRAM write enable.
DRAS0#	72	O	DRAM row address strobe 0.
DRAS1#	73	O	DRAM row address strobe 1 (active-low).
DBANKSEL1		O	DRAM address bus select 1 output. Only active in 64Mb SDRAM mode.
DRAS2#	74	O	DRAM row address strobe 2 output.
DBANKSEL0		O	DRAM address bus select 0 output. Only active in 64Mb SDRAM mode.
DB[15:0]	96:93, 90:85, 82:77	I/O	DRAM data bus [15:0].
DCS[1:0]#	97, 100	O	SDRAM chip select [1:0].
DQM	101	O	Data input/output mask.
DSCK	102	O	Output clock to SDRAM.
DCLK	105	I	27 MHz clock input to PLL.
YUV[7:0]	115:113, 110:106	O	8-bit YUV output.
PCLK2XSCN	116	I/O	2X pixel clock.
PCLKQSCN	117	I/O	Pixel clock.
VSYNC#	118	I/O	Vertical sync.
HSYNC#	119	I/O	Horizontal sync.
HD[15:0]	141:140, 137:131, 128:122	I/O	Host data bus
VPP	159	I	5.0V power supply.
AUX[7:0]	169:165,162:160	I/O	Auxiliary ports.
LOE#	170	O	EPROM device output enable.
LCS[3:0]#	176:173	O	EPROM chip select [3:0].
LD[15:0]	197:194, 191:185, 182:178	I/O	EPROM device data bus.
LWRLL#	198	O	Device write enable.
LWRHL#	199	O	Device write enable (active-low).

ES4427 PINOUT

Figure 2 shows the ES4427 device pinout.

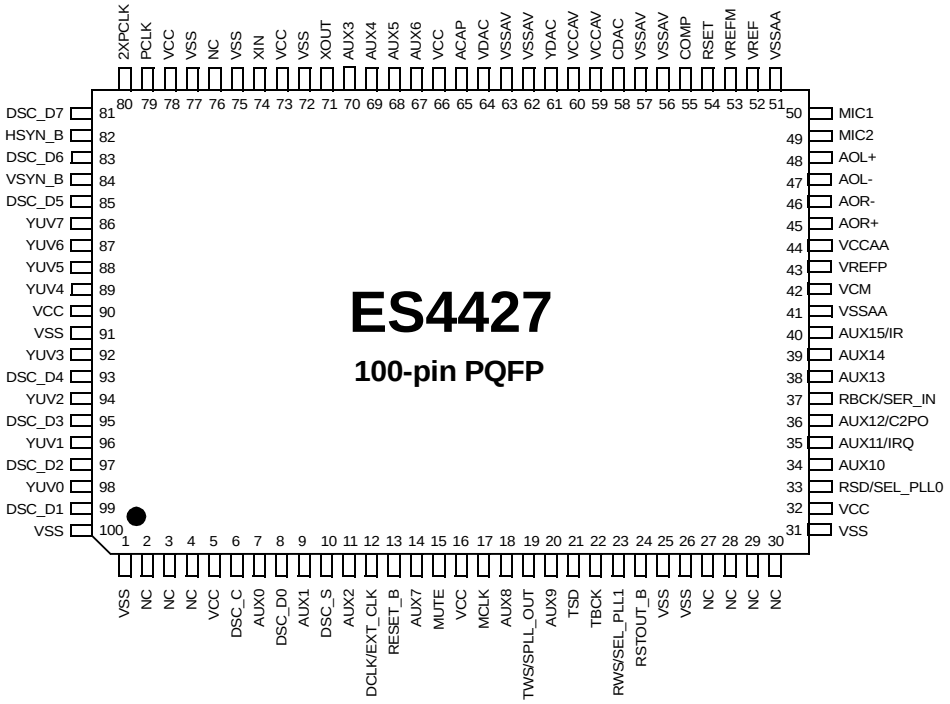


Figure 2 ES4427 Device Pinout

ES4427 PIN DESCRIPTION

Table 2 lists the pin descriptions for the ES4427.

Table 2 ES4427 Pin Descriptions

Name	Number	I/O	Definition
VSS	1, 25:26, 31, 72, 75, 77, 91, 100	I	Ground.
NC	2:4, 27:30, 76		No connect.
VCC	5, 16, 32, 66, 73, 78, 90	I	5.0V power supply.
DSC_C	6	I	Clock for programming to access internal registers.
AUX0	7	I/O	General purpose I/O.
DSC_D[7:0]	8, 81, 83, 85, 93, 95, 97, 99	I/O	Data for programming to access internal registers.
AUX1	9	I/O	General purpose I/O.
DSC_S	10	I	Strobe for programming to access internal registers.
AUX2	11	I/O	General purpose I/O.
DCLK	12	O	MPEG decoder output clock.
EXT_CLK		I	EXT_CLK is the external clock EXT_CLK is an input during bypass PLL mode.
RESET#	13	I	Reset.
AUX7	14	I/O	General purpose I/O.
MUTE	15	O	Audio mute.
MCLK	17	I	Audio master clock.

Table 2 ES4427 Pin Descriptions (Continued)

Name	Number	I/O	Definition
AUX8	18	I/O	General purpose I/O.
TWS	19	I	Transmit audio frame sync.
SPLL_OUT		O	SPLL_OUT is the select PLL output.
AUX9	20	I/O	General purpose I/O.
TSD	21	I	Transmit audio data input.
TBCK	22	I	Transmit audio bit clock.
RWS	23	O	Receive audio frame sync.
SEL_PLL1		I	System and DSCK output clock frequency selection at reset time. The matrix below lists the available clock frequencies and their respective PLL bit settings..

SEL_PLL1	SEL_PLL0	DCLK
0	0	Bypass PLL (input mode)
0	1	27 MHz (output mode) Default
1	0	32.4 MHz (output mode)
1	1	40.5 MHz (output mode)

RSTOUT#	24	O	Reset output.
RSD	33	O	Receive audio data input.
SEL_PLL0		I	Refer to the description and matrix for SEL_PLL1 pin 23.
AUX10	34	I/O	General purpose I/O.
AUX11	35	I/O	Interrupt output to ES4428.
AUX12	36	I/O	CD loader C2PO.
RBCK	37	O	Receive audio bit output clock.
SER_IN		I	SER_IN is the serial input DSC mode. 1 = Serial DSC mode. 0 = Parallel DSC mode.
AUX13	38	I/O	General purpose I/O.
AUX14	39	I/O	Interrupt input from Modem DSP.
AUX15	40	I/O	IR interrupt Input.
VSSAA	41,51	I	Audio analog ground.
VCM	42	I	ADC Common Mode Reference (CMR) buffer output. CMR is approximately 2.25 V. Bypass to analog ground with 47 µF electrolytic in parallel with 0.1 µF.
VREFP	43	I	DAC and ADC maximum reference. Bypass to VCMR with 10 µF in parallel with 0.1 µF.
VCCAA	44	I	5.0V analog audio power supply.
AOR+, AOR-	45, 46	O	Right channel output.
AOL-, AOL+	47, 48	O	Left channel output.
MIC2	49	I	Microphone input 2.
MIC1	50	I	Microphone input 1.
VREF	52	I	Internal resistor divider generates Common Mode Reference (CMR) voltage. Bypass to analog ground with 0.1 µF.
VREFM	53	I	DAC and ADC minimum reference. Bypass to VCMR with 10 µF in parallel with 0.1 µF.
RSET	54	I	Full scale DAC current adjustment.
COMP	55	I	Compensation pin.
VSSAV	56:57, 62:63	I	Video analog ground
CDAC	58	O	Modulated chrominance output.
VCCAV	59, 60	I	Video VCC, 5 V

Table 2 ES4427 Pin Descriptions (Continued)

Name	Number	I/O	Definition
YDAC	61	O	Y luminance data bus for screen video port.
VDAC	64	O	Composite video output.
ACAP	65	I	Audio CAP
AUX6	67	I/O	General purpose I/O.
AUX5	68	I/O	General purpose I/O.
AUX4	69	I/O	Modem DSP reset.
AUX3	70	I/O	CD loader reset.
XOUT	71	O	Crystal output.
XIN	74	I	27 MHz crystal input.
PCLK	79	I/O	13.5 MHz pixel clock.
2XPCLK	80	I/O	27 MHz doubled pixel clock.
HSYNC#	82	O	Horizontal sync.
VSYNC#	84	O	Vertical sync.
YUV[7:0]	86:89, 92, 94, 96, 98	I	YUV data bus for screen video port.

SYSTEM BLOCK DIAGRAM

Figure 3 shows a sample system block diagram of an ESS-based Web/DVD system.

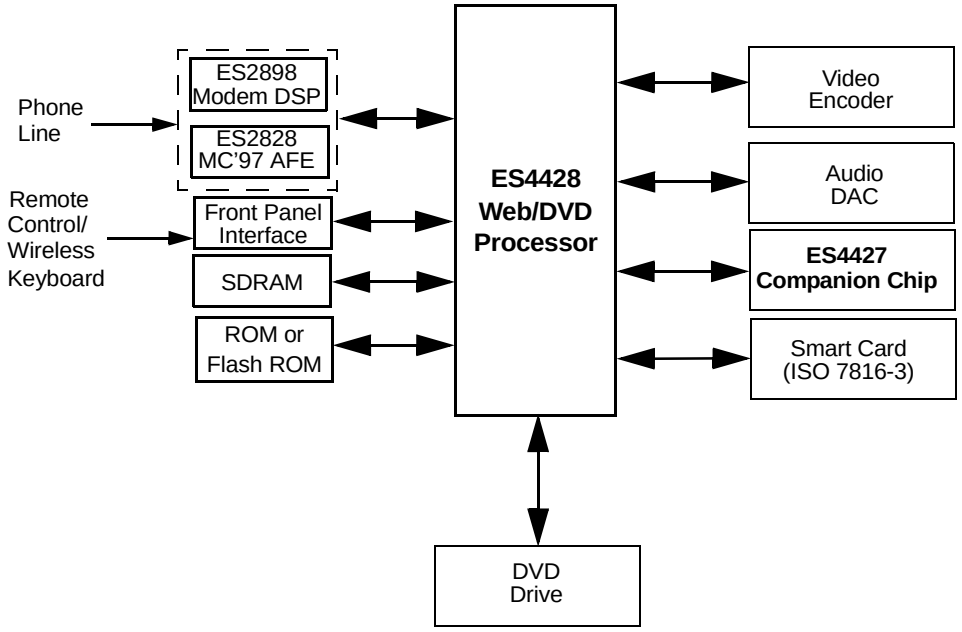
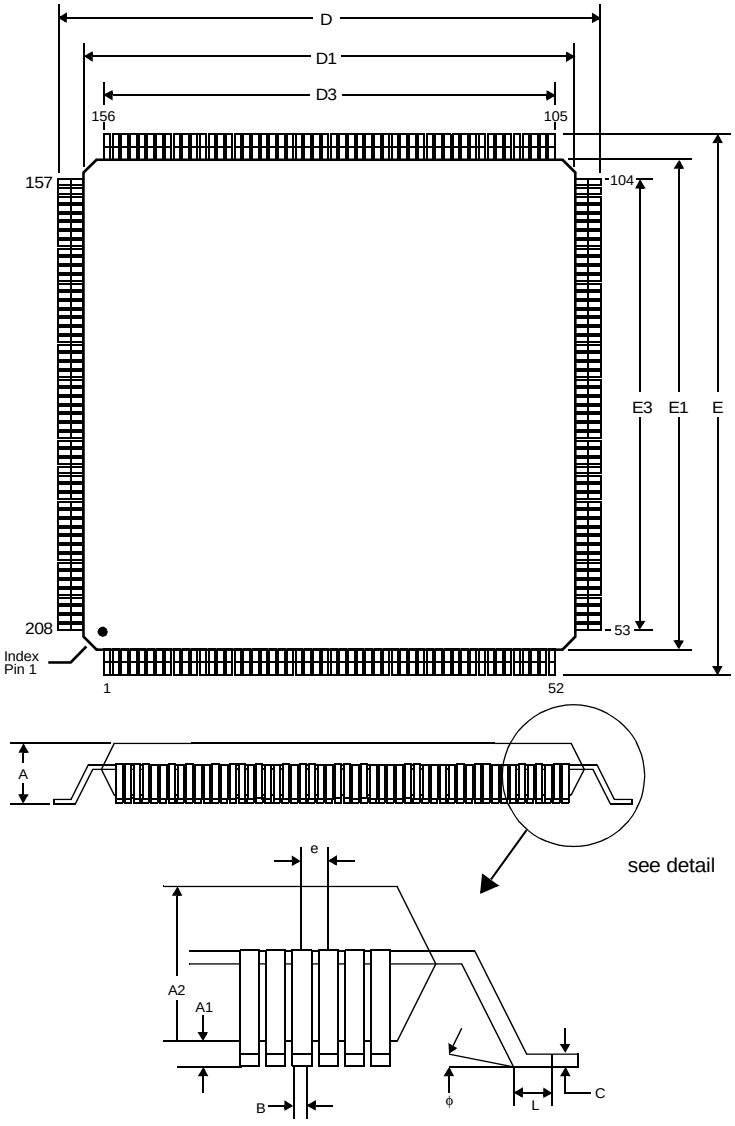


Figure 3 ES4428/ES4427 System Block Diagram

MECHANICAL DIMENSIONS, ES4428

Figure 4 shows the mechanical dimensions of the ES4428.



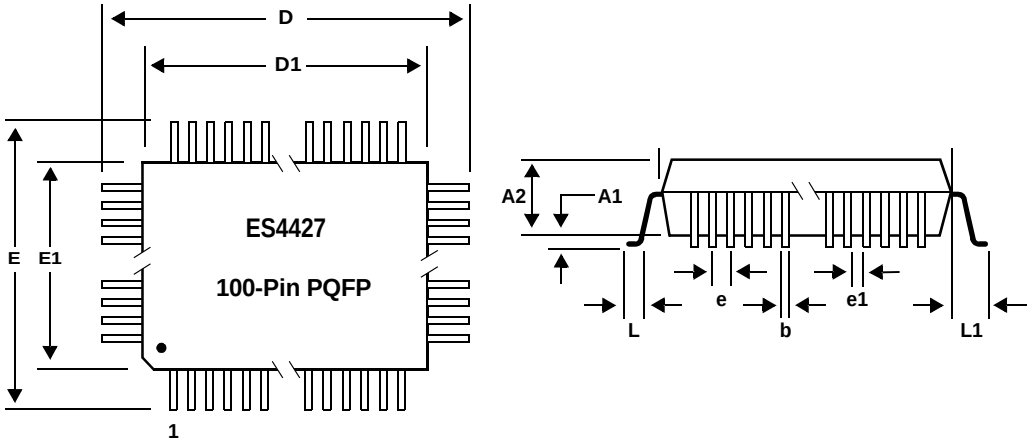
Note:
1. All dimensions are in inches (millimeters).
2. Actual package used has millimeter native dimensions – take care with rounding from metric to imperial.

Symbol	Min	Nom	Max
A	–	–	0.165
A1	0.010 (0.25)	–	–
A2	0.130 (3.30)	0.134 (3.40)	0.138 (3.50)
B	0.007 (0.18)	0.009 (0.23)	0.011 (0.28)
C	0.005 (0.12)	0.006 (0.16)	0.008 (0.20)
D	1.195 (30.35)	1.205 (30.60)	1.215 (30.85)
D1	1.098 (27.90)	1.102 (28.00)	1.106 (28.10)
D3	1.004 (25.50) REF		
e	0.0197 (0.50) BASIC		
E	1.195 (30.35)	1.205 (30.60)	1.215 (30.85)
E1	1.098 (27.90)	1.102 (28.00)	1.106 (28.10)
E3	1.004 (25.50) REF		
L	0.016 (0.40)	0.020 (0.50)	0.024 (0.60)
ϕ	0 i	2.5 i	5.0 i

Figure 4 ES4428 Mechanical Dimensions

MECHANICAL DIMENSIONS, ES4427

Figure 5 shows the mechanical dimensions of the ES4427.



Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-axis	23.65	23.90	24.15
D1	Package's outside, X-axis	19.90	20.00	20.10
E	Lead to lead, Y-axis	17.65	17.90	18.15
E1	Package's outside, Y-axis	13.90	14.00	14.10
A1	Board standoff	0.10	0.25	0.36
A2	Package thickness	2.57	2.71	2.87
b	Lead width	0.20	0.30	0.40
e	Lead pitch	-	0.65	-
e1	Lead gap	0.24	-	-
L	Foot length	0.65	0.80	0.95
L1	Lead length	1.88	1.95	2.02
-	Foot angle	0°	-	7°
-	Coplanarity	-	-	0.102
-	Leads in X-axis	-	30	-
-	Leads in Y-axis	-	20	-
-	Total leads	-	100	-
-	Package type	-	PQFP	-

Figure 5 ES4427 Mechanical Dimensions

ORDERING INFORMATION

Part Number	Description	Package
ES4428	Web DVD Processor	208-pin PQFP
ES4427	Companion Chip	100-pin PQFP

ESS Technology, Inc.
48401 Fremont Blvd.
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