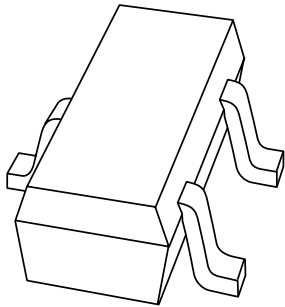


# DATA SHEET



## **PDTC114EE** NPN resistor-equipped transistor

Product specification  
Supersedes data of 1998 Nov 26

1999 May 18

# NPN resistor-equipped transistor

# PDTC114EE

### FEATURES

- Built-in bias resistors R1 and R2 (typ. 10 kΩ each)
- Simplification of circuit design
- Reduces number of components and board space.

### APPLICATIONS

- Especially suitable for space reduction in interface and driver circuits
- Inverter circuit configurations without use of external resistors.

### DESCRIPTION

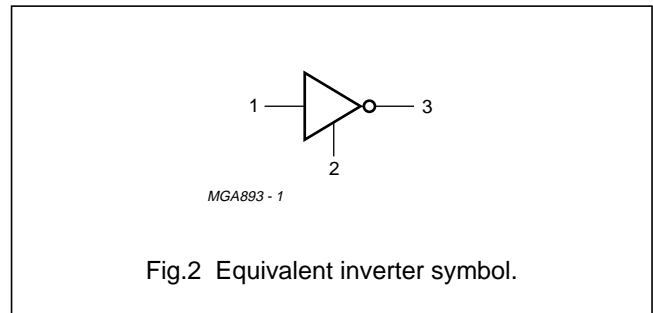
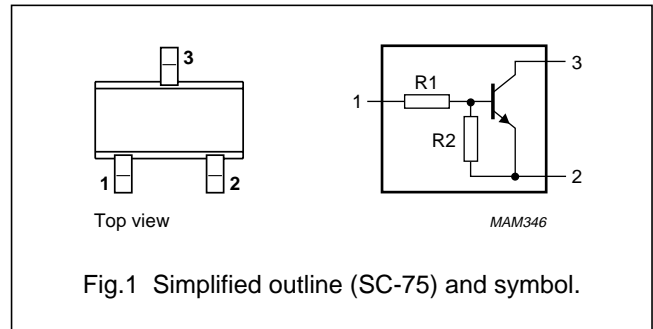
NPN resistor-equipped transistor in an SC-75 plastic package. PNP complement: PDTA114EE.

### MARKING

TYPE NUMBER	MARKING CODE
PDTC114EE	09

### PINNING

PIN	DESCRIPTION
1	base/input
2	emitter/ground
3	collector/output



### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	50	V
$V_{CEO}$	collector-emitter voltage	open base	–	50	V
$V_{EBO}$	emitter-base voltage	open collector	–	10	V
$V_i$	input voltage		–	+40	V
			–	–10	V
$I_o$	output current (DC)		–	100	mA
$I_{CM}$	peak collector current		–	100	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$ ; note 1	–	150	mW
$T_{stg}$	storage temperature		–65	+150	$^\circ\text{C}$
$T_j$	junction temperature		–	150	$^\circ\text{C}$
$T_{amb}$	operating ambient temperature		–65	+150	$^\circ\text{C}$

### Note

1. Transistor mounted on an FR4 printed-circuit board.

## NPN resistor-equipped transistor

## PDTC114EE

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	833	K/W

## Note

1. Transistor mounted on an FR4 printed-circuit board.

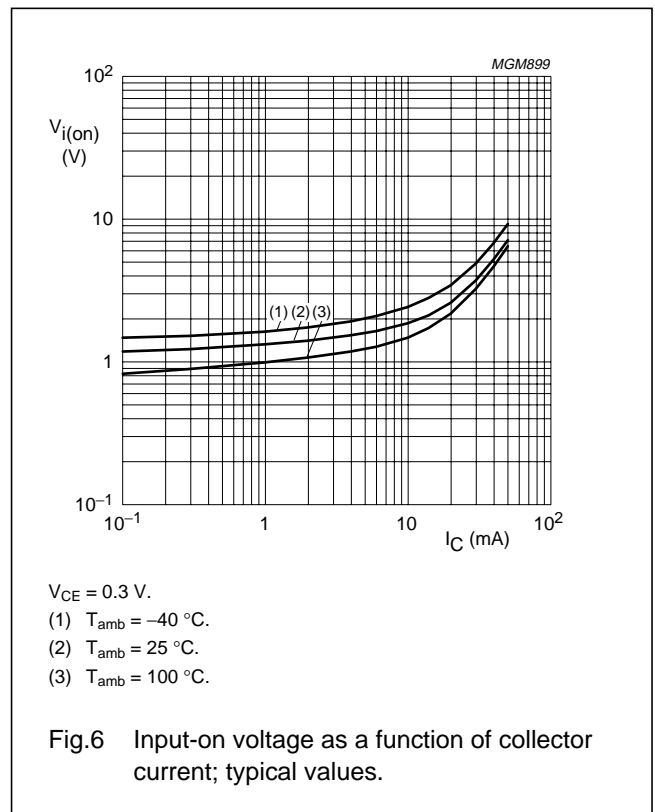
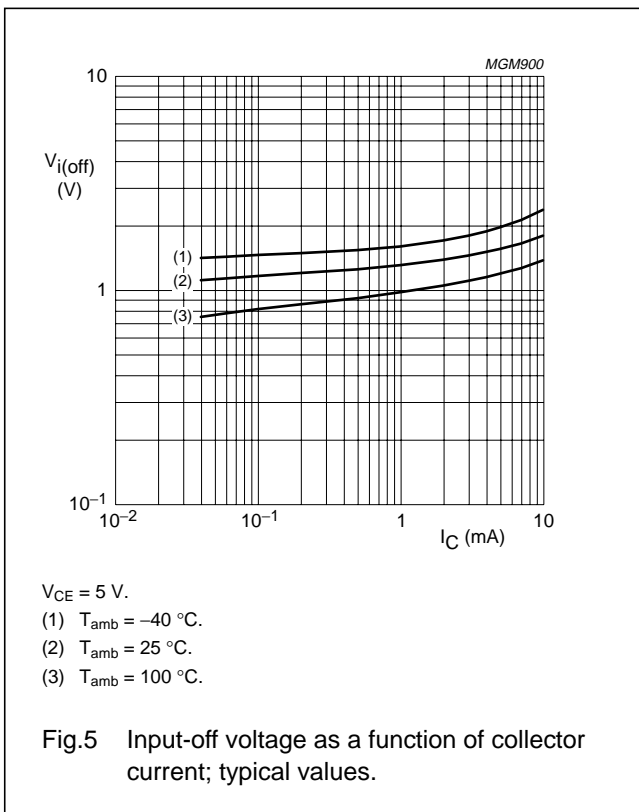
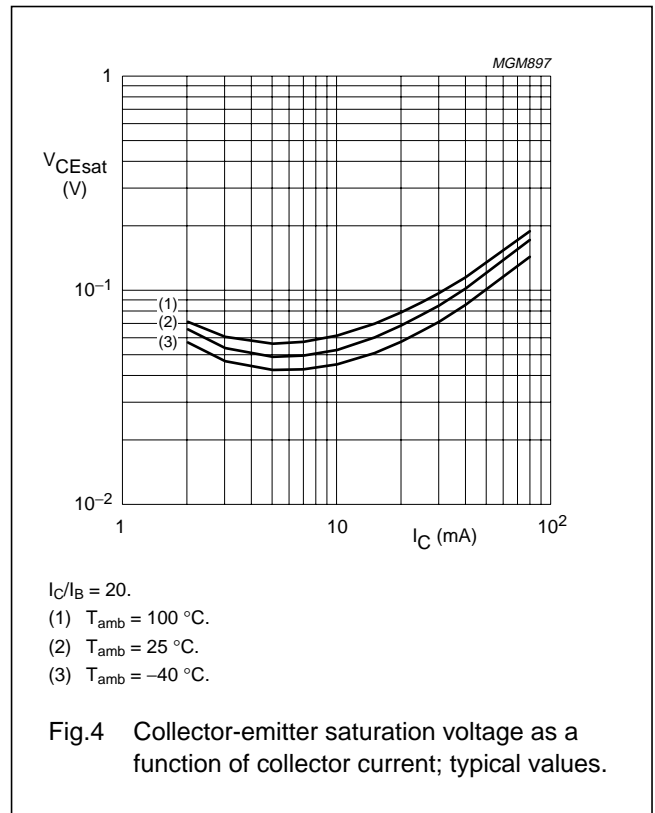
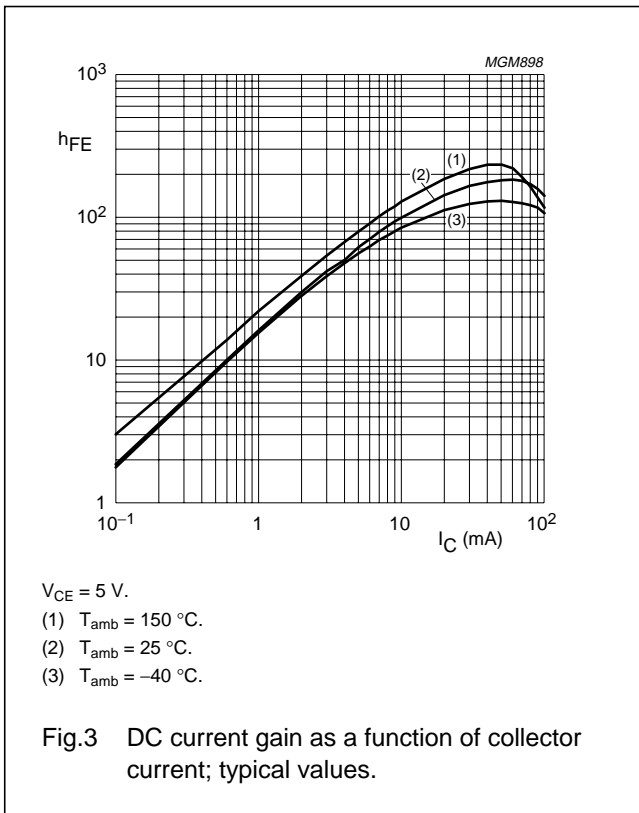
## CHARACTERISTICS

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CBO}$	collector cut-off current	$I_E = 0; V_{CB} = 50\text{ V}$	–	–	100	nA
$I_{CEO}$	collector cut-off current	$I_B = 0; V_{CE} = 30\text{ V}$	–	–	1	$\mu\text{A}$
		$I_B = 0; V_{CE} = 30\text{ V}; T_j = 150\text{ °C}$	–	–	50	$\mu\text{A}$
$I_{EBO}$	emitter cut-off current	$I_C = 0; V_{EB} = 5\text{ V}$	–	–	400	$\mu\text{A}$
$h_{FE}$	DC current gain	$I_C = 5\text{ mA}; V_{CE} = 5\text{ V}$	30	–	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$	–	–	150	mV
$V_{i(off)}$	input-off voltage	$I_C = 100\text{ }\mu\text{A}; V_{CE} = 5\text{ V}$	–	1.1	0.8	V
$V_{i(on)}$	input-on voltage	$I_C = 10\text{ mA}; V_{CE} = 0.3\text{ V}$	2.5	1.8	–	V
R1	input resistor		7	10	13	k $\Omega$
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
$C_c$	collector capacitance	$I_E = I_e = 0; V_{CB} = 10\text{ V}; f = 1\text{ MHz}$	–	–	2.5	pF

NPN resistor-equipped transistor

PDTC114EE



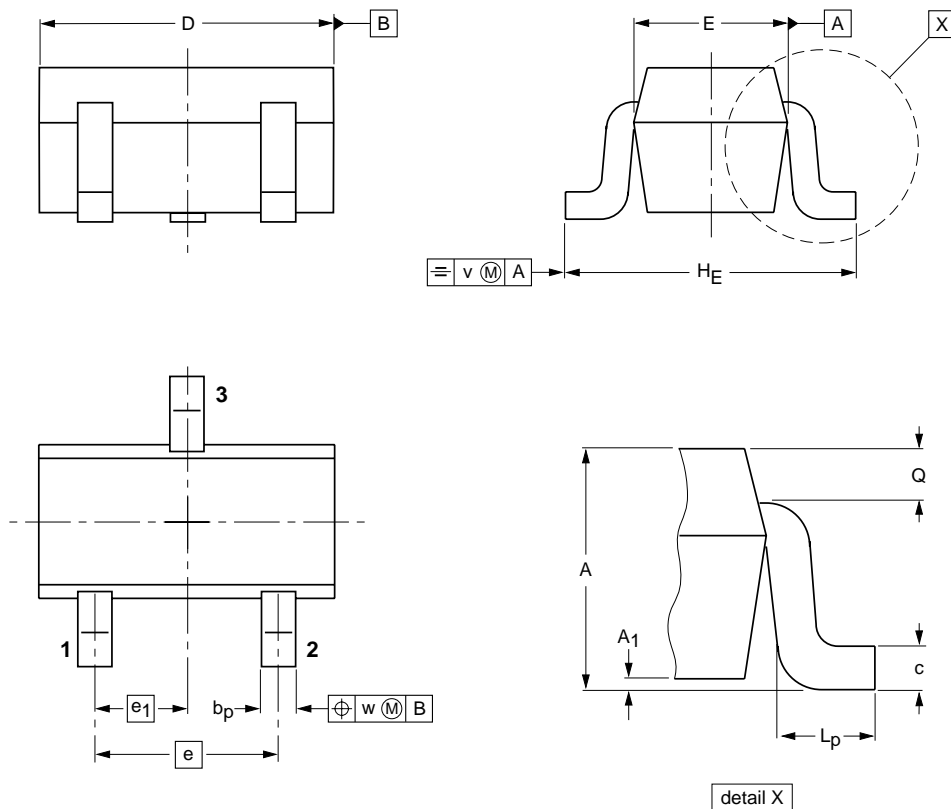
NPN resistor-equipped transistor

PDTC114EE

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT416



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	0.95 0.60	0.1	0.30 0.15	0.25 0.10	1.8 1.4	0.9 0.7	1	0.5	1.75 1.45	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT416			SC-75			97-02-28

## NPN resistor-equipped transistor

PDTC114EE

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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NPN resistor-equipped transistor

PDTC114EE

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