

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
V _B	High Side Floating Supply Voltage	-0.3	625	V
V _S	High Side Floating Supply Offset Voltage	V _B - 25	V _B + 0.3	
V _{HO}	High Side Floating Output Voltage	V _S - 0.3	V _B + 0.3	
V _{CC}	Low Side Fixed Supply Voltage	-0.3	25	
V _{LO}	Low Side Output Voltage	-0.3	V _{CC} + 0.3	
V _{DD}	Logic Supply Voltage	-0.3	V _{SS} + 25	
V _{SS}	Logic Supply Offset Voltage	V _{CC} - 25	V _{CC} + 0.3	
V _{IN}	Logic Input Voltage (HIN, LIN & SD)	V _{SS} - 0.3	V _{DD} + 0.3	
dV _S /dt	Allowable Offset Supply Voltage Transient (Figure 2)	—	50	V/ns
P _D	Package Power Dissipation @ T _A ≤ +25°C (14 Lead DIP)	—	1.6	W
	(14 Lead DIP w/o Lead 4)	—	1.5	
	(16 Lead DIP w/o Leads 5 & 6)	—	1.6	
	(16 Lead SOIC)	—	1.25	
R _{θJA}	Thermal Resistance, Junction to Ambient (14 Lead DIP)	—	75	°C/W
	(14 Lead DIP w/o Lead 4)	—	85	
	(16 Lead DIP w/o Leads 5 & 6)	—	75	
	(16 Lead SOIC)	—	100	
T _J	Junction Temperature	—	150	°C
T _S	Storage Temperature	-55	150	
T _L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figures 36 and 37.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
V _B	High Side Floating Supply Absolute Voltage	V _S + 10	V _S + 20	V
V _S	High Side Floating Supply Offset Voltage	Note 1	600	
V _{HO}	High Side Floating Output Voltage	V _S	V _B	
V _{CC}	Low Side Fixed Supply Voltage	10	20	
V _{LO}	Low Side Output Voltage	0	V _{CC}	
V _{DD}	Logic Supply Voltage	V _{SS} + 5	V _{SS} + 20	
V _{SS}	Logic Supply Offset Voltage	-5	5	
V _{IN}	Logic Input Voltage (HIN, LIN & SD)	V _{SS}	V _{DD}	
T _A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

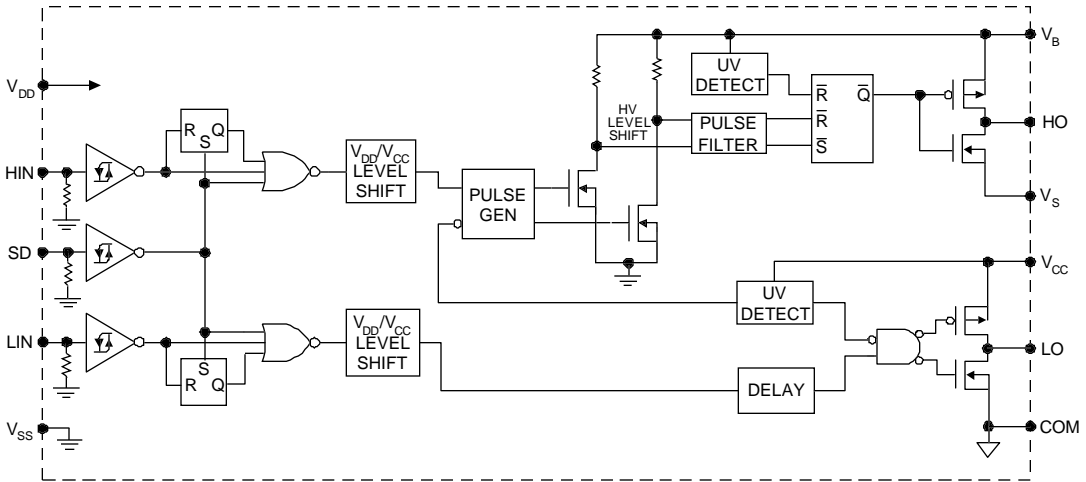
Symbol	Parameter Definition	Figure	Value			Units	Test Conditions
			Min.	Typ.	Max.		
t_{on}	Turn-On Propagation Delay	7	—	125	180	ns	$V_S = 0V$
t_{off}	Turn-Off Propagation Delay	8	—	105	160		$V_S = 600V$
t_{sd}	Shutdown Propagation Delay	9	—	105	160		$V_S = 600V$
t_r	Turn-On Rise Time	10	—	80	130		
t_f	Turn-Off Fall Time	11	—	40	65		
MT	Delay Matching, HS & LS Turn-On/Off	—	—	—	30		

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter Definition	Figure	Value			Units	Test Conditions
			Min.	Typ.	Max.		
V_{IH}	Logic "1" Input Voltage	12	9.5	—	—	V	
V_{IL}	Logic "0" Input Voltage	13	—	—	6.0		
V_{OH}	High Level Output Voltage, $V_{BIAS} - V_O$	14	—	—	100	mV	$I_O = 0A$
V_{OL}	Low Level Output Voltage, V_O	15	—	—	100		$I_O = 0A$
I_{LK}	Offset Supply Leakage Current	16	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} Supply Current	17	—	25	60		$V_{IN} = 0V$ or V_{DD}
I_{QCC}	Quiescent V_{CC} Supply Current	18	—	80	180		$V_{IN} = 0V$ or V_{DD}
I_{QDD}	Quiescent V_{DD} Supply Current	19	—	2.0	5.0		$V_{IN} = 0V$ or V_{DD}
I_{IN+}	Logic "1" Input Bias Current	20	—	20	40		$V_{IN} = V_{DD}$
I_{IN-}	Logic "0" Input Bias Current	21	—	—	1.0		$V_{IN} = 0V$
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	22	7.4	8.5	9.6	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	23	7.0	8.1	9.2		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	24	7.6	8.6	9.6		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	25	7.2	8.2	9.2		
I_{O+}	Output High Short Circuit Pulsed Current	26	200	250	—	A	$V_O = 0V, V_{IN} = V_{DD}$ $PW \leq 10 \mu s$
I_{O-}	Output Low Short Circuit Pulsed Current	27	420	500	—		$V_O = 15V, V_{IN} = 0V$ $PW \leq 10 \mu s$

Functional Block Diagram



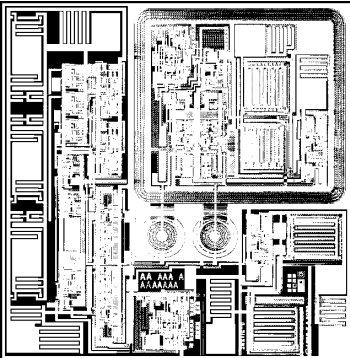
Lead Definitions

Symbol	Description
VDD	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
VSS	Logic ground
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return
VCC	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

<p>14 Lead DIP</p>	<p>14 Lead DIP w/o Lead 4</p>	<p>16 Lead DIP w/o Leads 4 & 5</p>	<p>16 Lead SOIC (Wide Body)</p>
IR2112	IR2112-1	IR2112-2	IR2112S
Part Number			

Device Information

Process & Design Rule		HVDCMOS 4.0 μ m
Transistor Count		220
Die Size		100 X 117 X 26 (mil)
Die Outline		
Thickness of Gate Oxide		800Å
Connections	Material	Poly Silicon
	First Layer	Width Spacing Thickness
		4 μ m 6 μ m 5000Å
Second Layer	Material	Al - Si (Si: 1.0% \pm 0.1%)
	Width	6 μ m
	Spacing	9 μ m
	Thickness	20,000Å
Contact Hole Dimension		8 μ m X 8 μ m
Insulation Layer	Material	PSG (SiO ₂)
	Thickness	1.5 μ m
Passivation	Material	PSG (SiO ₂)
	Thickness	1.5 μ m
Method of Saw		Full Cut
Method of Die Bond		Ablebond 84 - 1
Wire Bond	Method	Thermo Sonic
	Material	Au (1.0 mil / 1.3 mil)
Leadframe	Material	Cu
	Die Area	Ag
	Lead Plating	Pb : Sn (37 : 63)
Package	Types	14 & 16 Lead PDIP / 16 Lead SOIC
	Materials	EME6300 / MP150 / MP190
Remarks:		

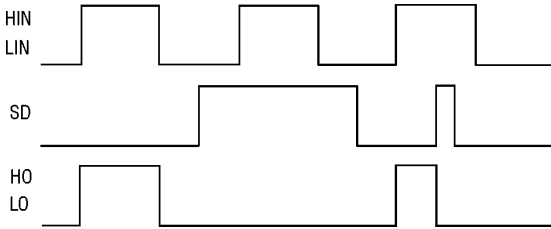


Figure 1. Input/Output Timing Diagram

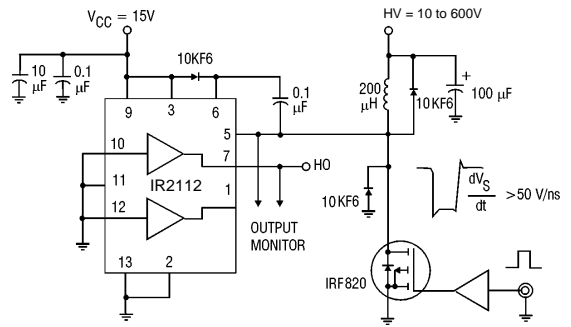


Figure 2. Floating Supply Voltage Transient Test Circuit

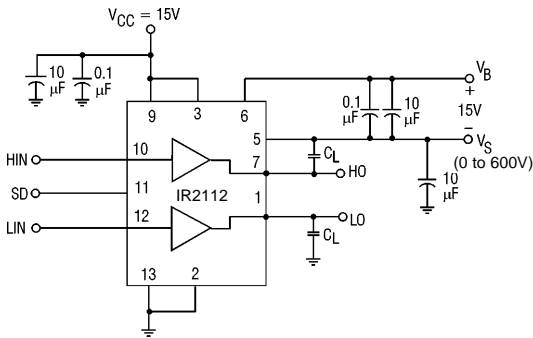


Figure 3. Switching Time Test Circuit

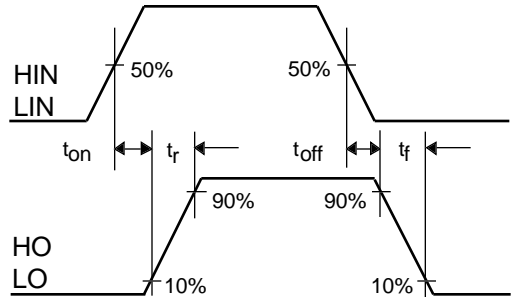


Figure 4. Switching Time Waveform Definition

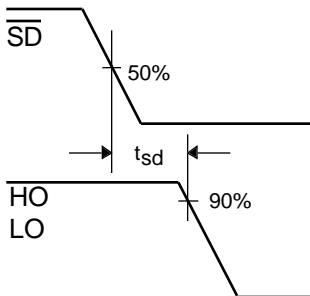


Figure 3. Shutdown Waveform Definitions

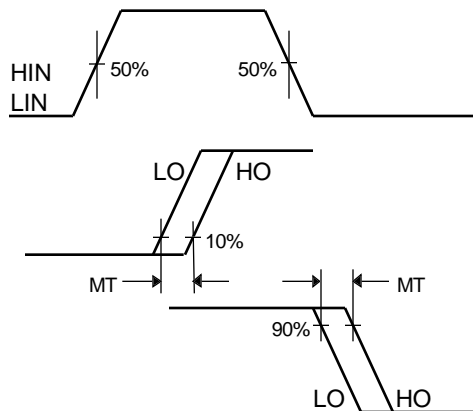


Figure 6. Delay Matching Waveform Definitions

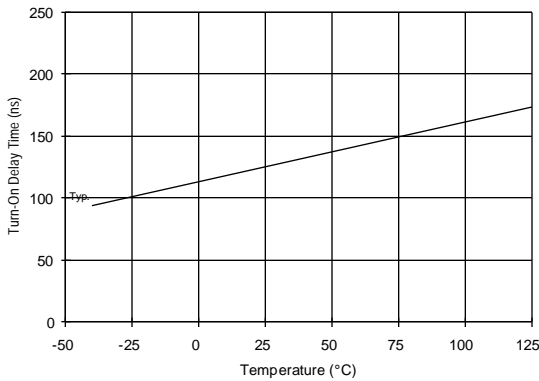


Figure 7A. Turn-On Time vs. Temperature

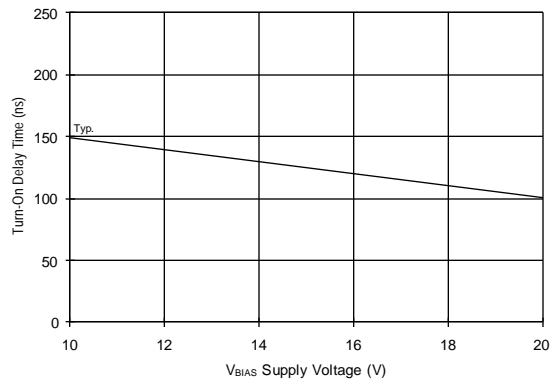


Figure 7B. Turn-On Time vs. Voltage

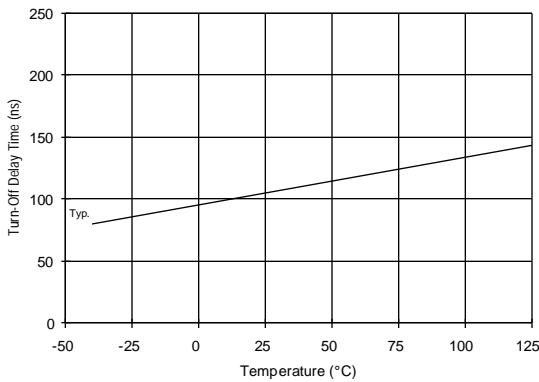


Figure 8A. Turn-Off Time vs. Temperature

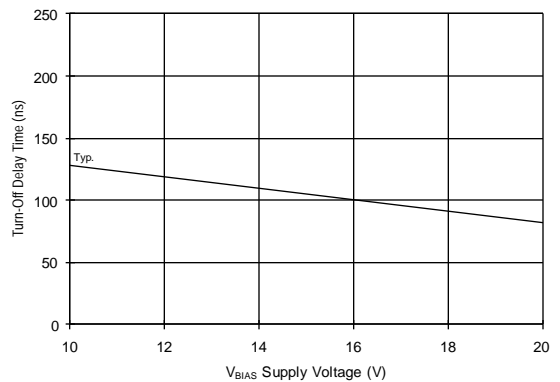


Figure 8B. Turn-Off Time vs. Voltage

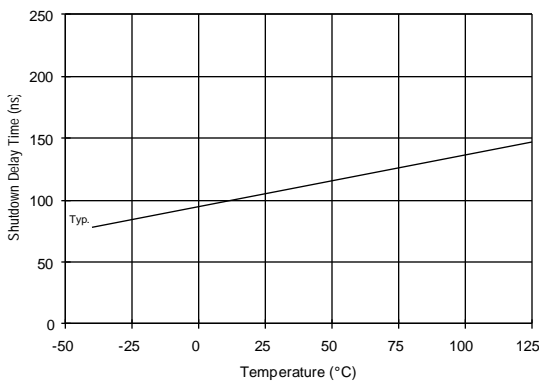


Figure 9A. Shutdown Time vs. Temperature

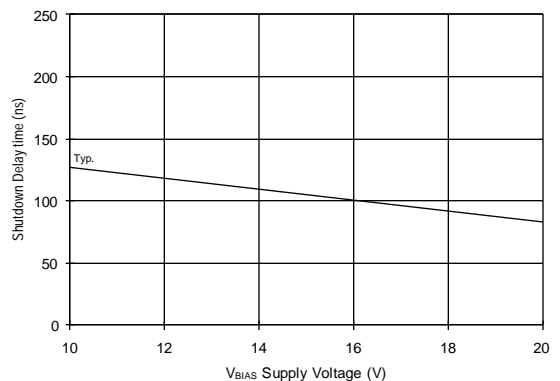


Figure 9B. Shutdown Time vs. Voltage

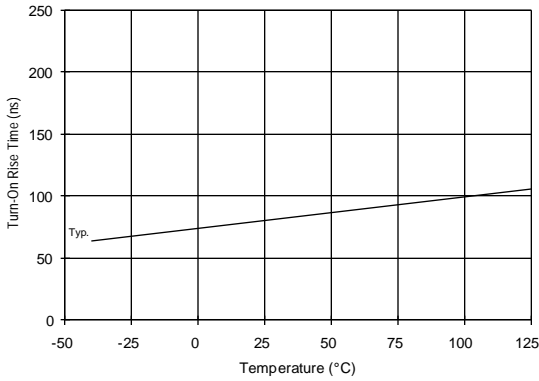


Figure 10A. Turn-On Rise Time vs. Temperature

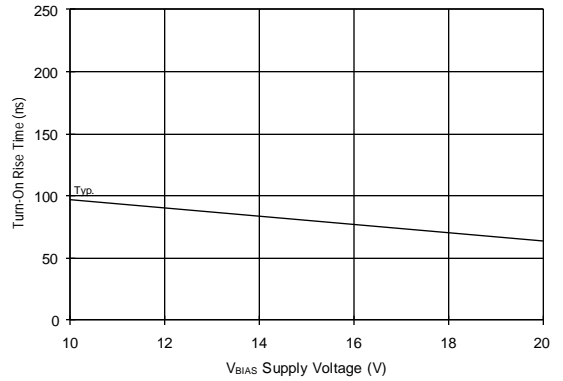


Figure 10B. Turn-On Rise Time vs. Voltage

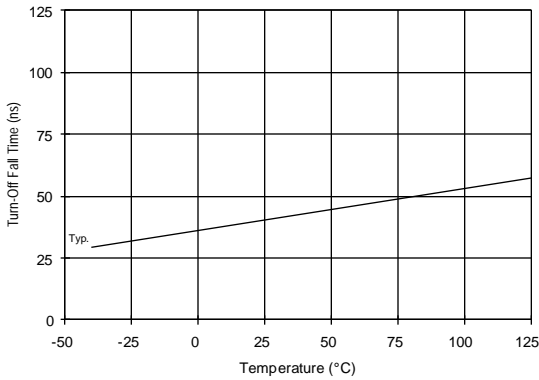


Figure 11A. Turn-Off Fall Time vs. Temperature

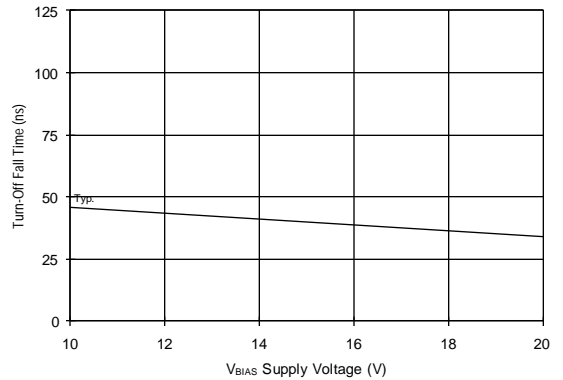


Figure 11B. Turn-Off Fall Time vs. Voltage

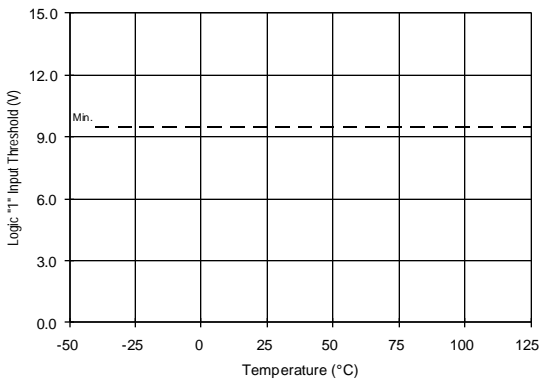


Figure 12A. Logic "1" Input Threshold vs. Temperature

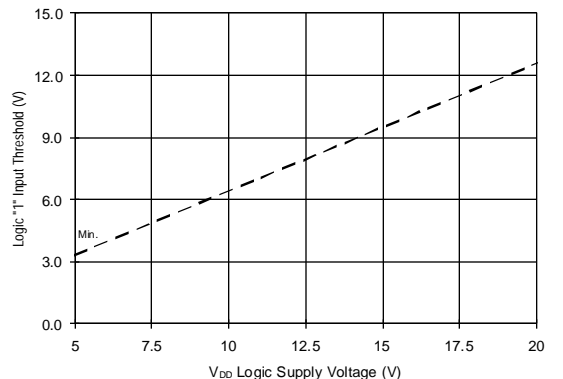


Figure 12B. Logic "1" Input Threshold vs. Voltage

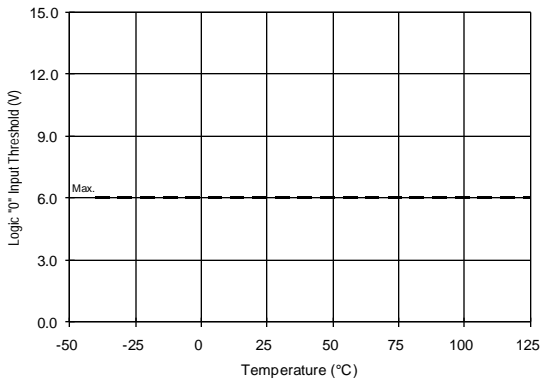


Figure 13A. Logic "0" Input Threshold vs. Temperature

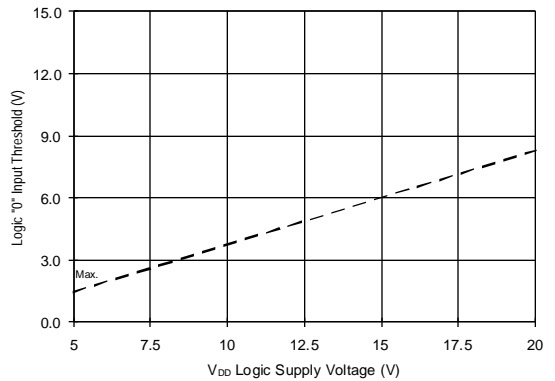


Figure 13B. Logic "0" Input Threshold vs. Voltage

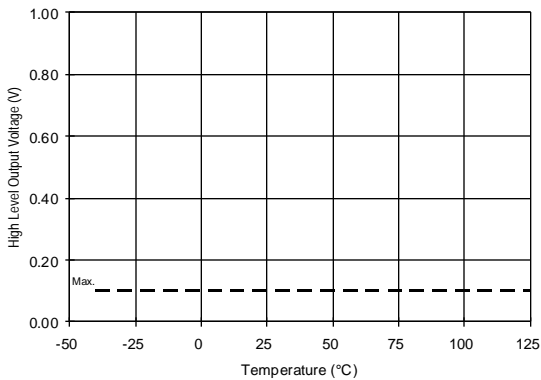


Figure 14A. High Level Output vs. Temperature

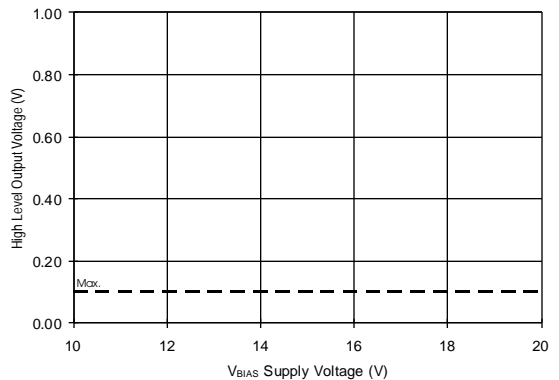


Figure 14B. High Level Output vs. Voltage

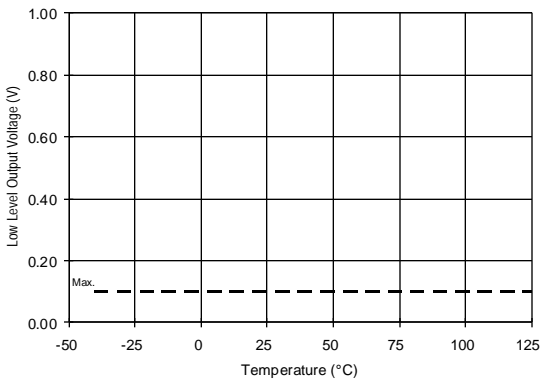


Figure 15A. Low Level Output vs. Temperature

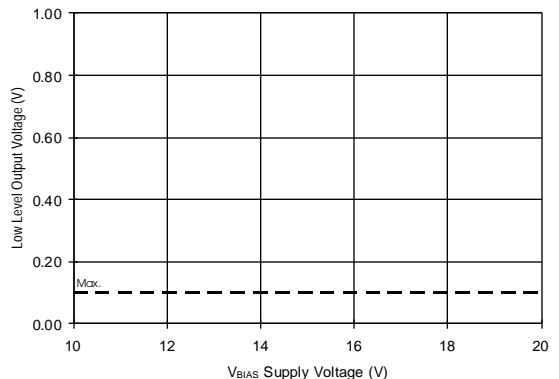


Figure 15B. Low Level Output vs. Voltage

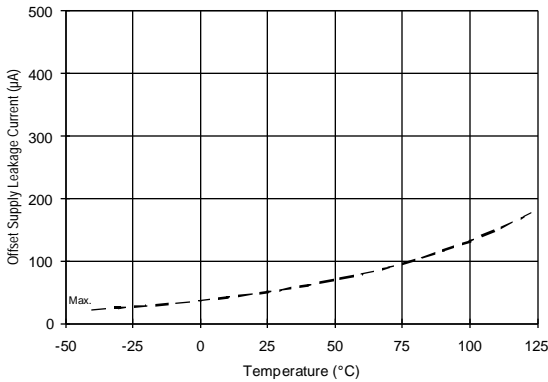


Figure 16A. Offset Supply Current vs. Temperature

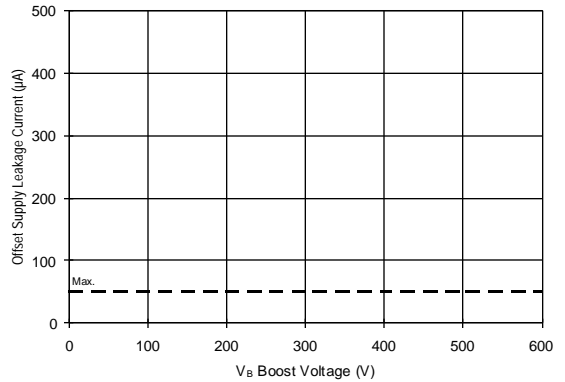


Figure 16B. Offset Supply Current vs. Voltage

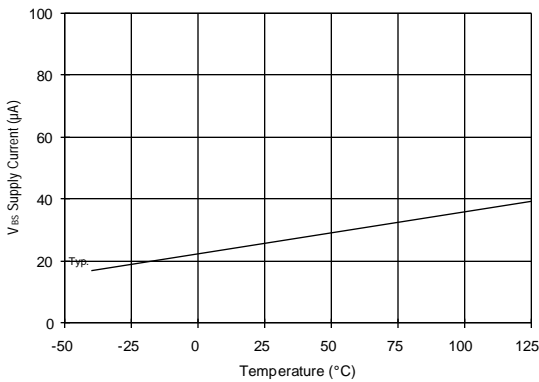


Figure 17A. V_{BS} Supply Current vs. Temperature

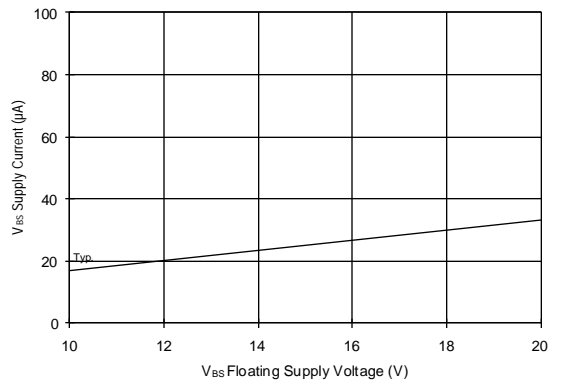


Figure 17B. V_{BS} Supply Current vs. Voltage

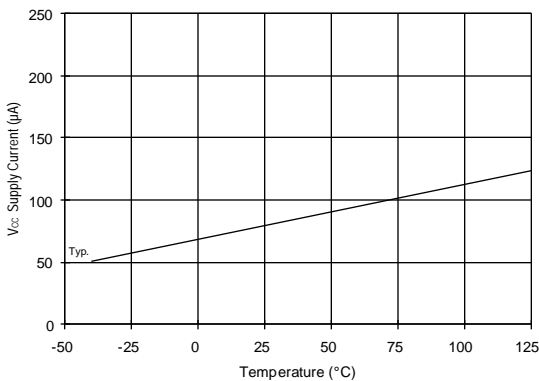


Figure 18A. V_{CC} Supply Current vs. Temperature

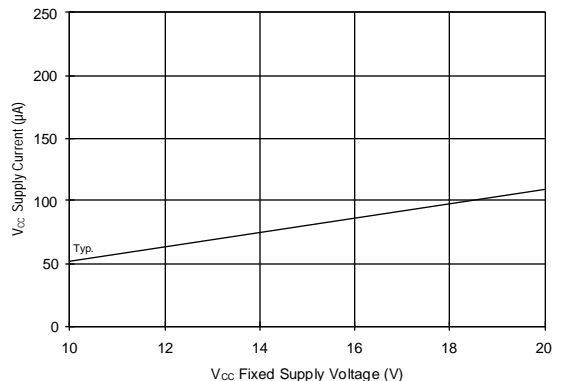


Figure 18B. V_{CC} Supply Current vs. Voltage

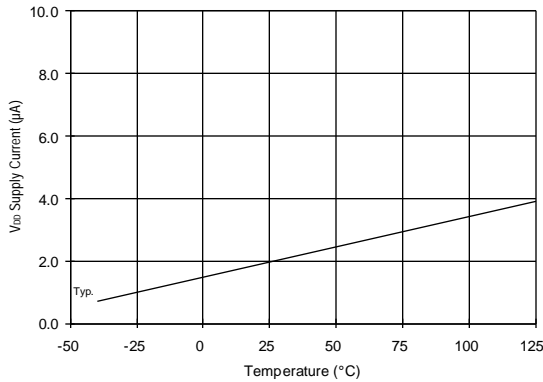


Figure 19A. V_{DD} Supply Current vs. Temperature

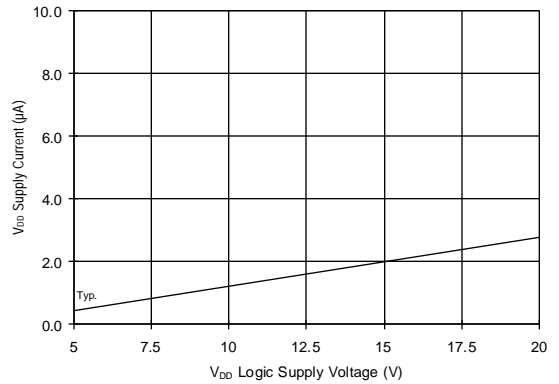


Figure 19B. V_{DD} Supply Current vs. Voltage

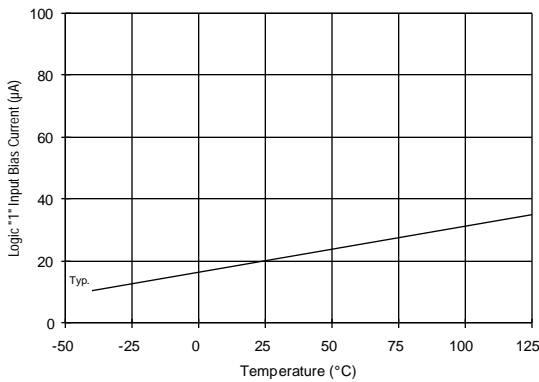


Figure 20A. Logic "1" Input Current vs. Temperature

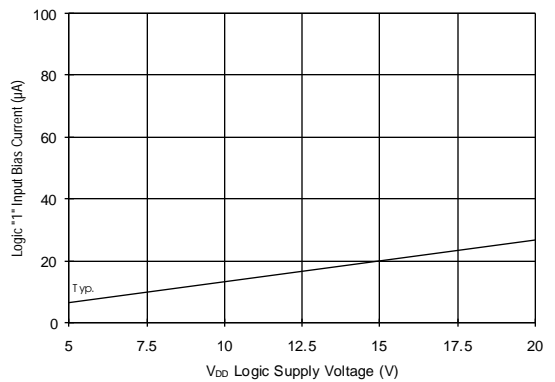


Figure 20B. Logic "1" Input Current vs. Voltage

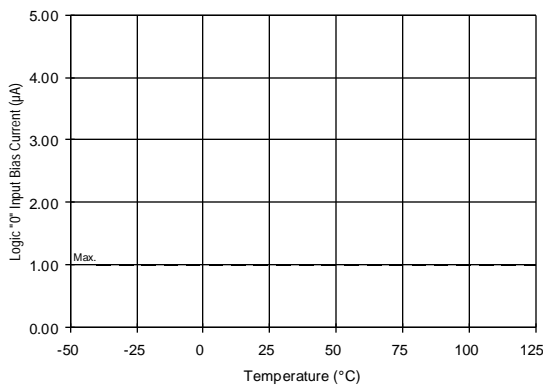


Figure 21A. Logic "0" Input Current vs. Temperature

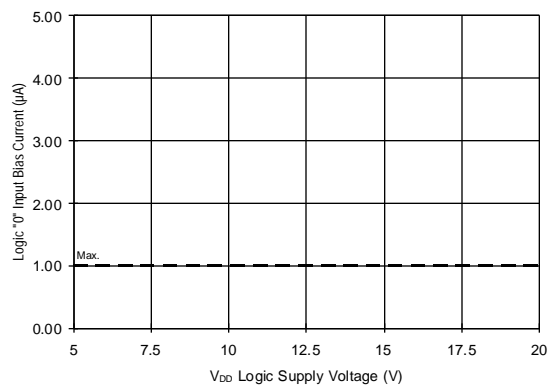


Figure 21B. Logic "0" Input Current vs. Voltage

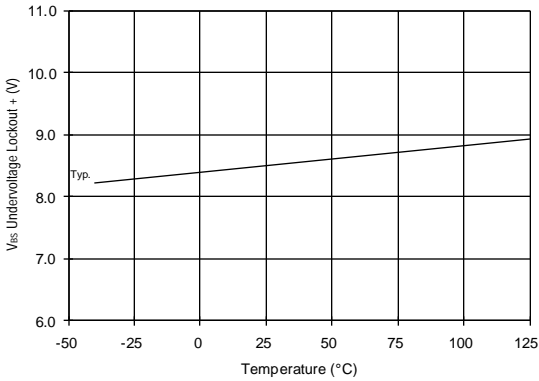


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

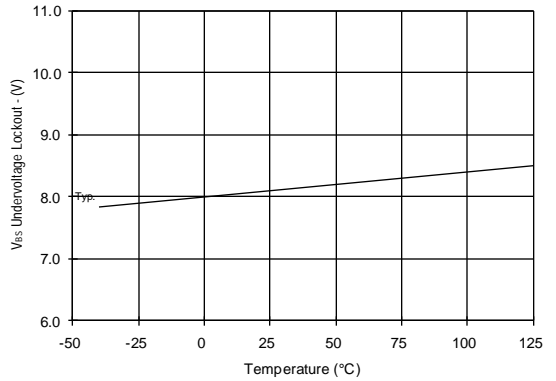


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

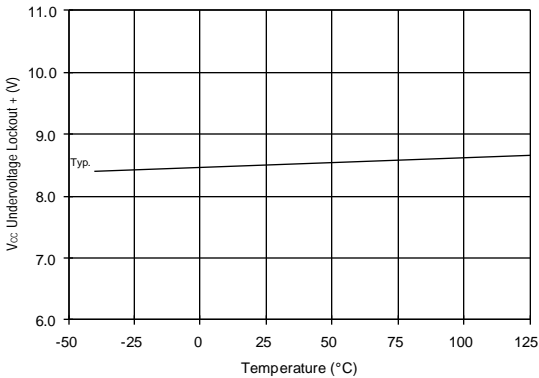


Figure 24. V_{CC} Undervoltage (+) vs. Temperature

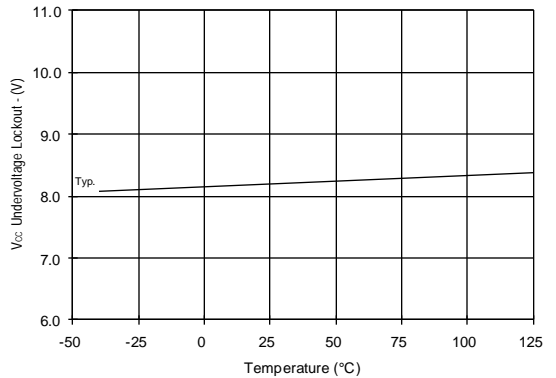


Figure 25. V_{CC} Undervoltage (-) vs. Temperature

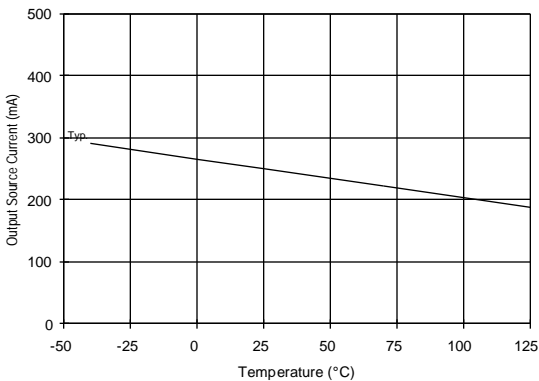


Figure 26A. Output Source Current vs. Temperature

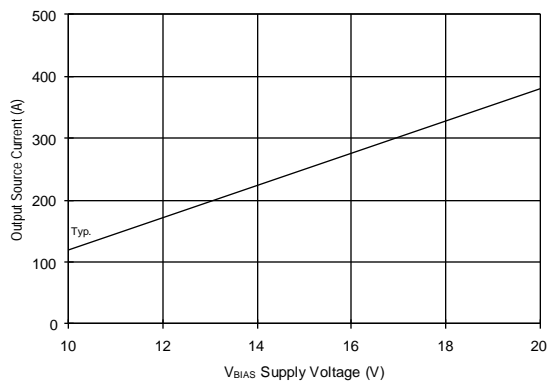


Figure 26B. Output Source Current vs. Voltage

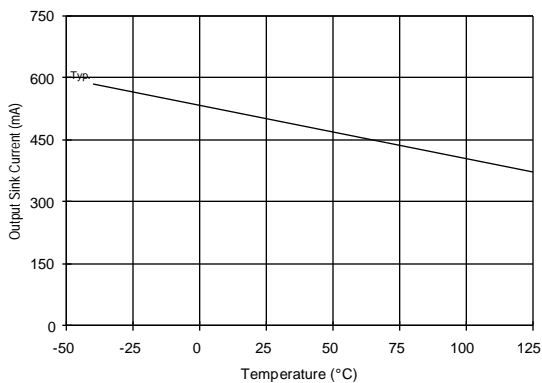


Figure 27A. Output Sink Current vs. Temperature

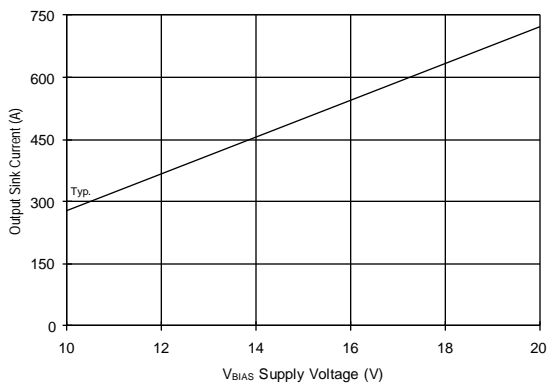


Figure 27B. Output Sink Current vs. Voltage

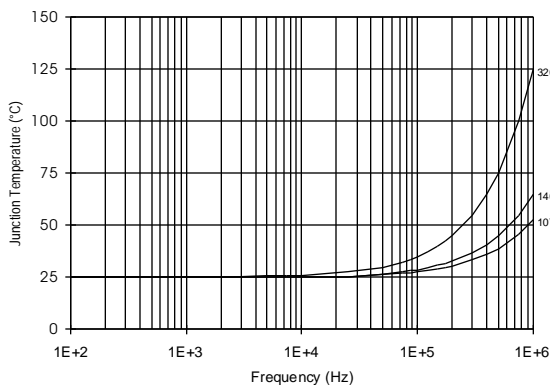


Figure 28. IR2112 T_J vs. Frequency (IRFBC20)
 $R_{GATE} = 33\Omega, V_{CC} = 15V$

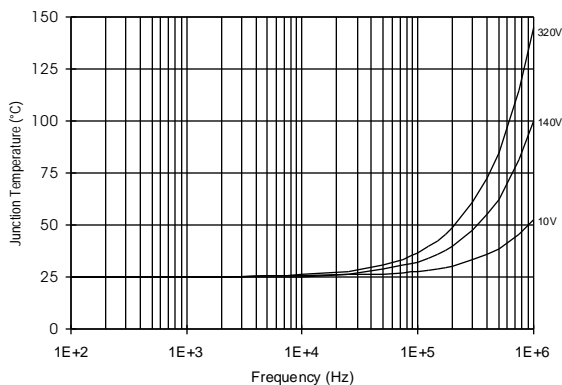


Figure 29. IR2112 T_J vs. Frequency (IRFBC30)
 $R_{GATE} = 22\Omega, V_{CC} = 15V$

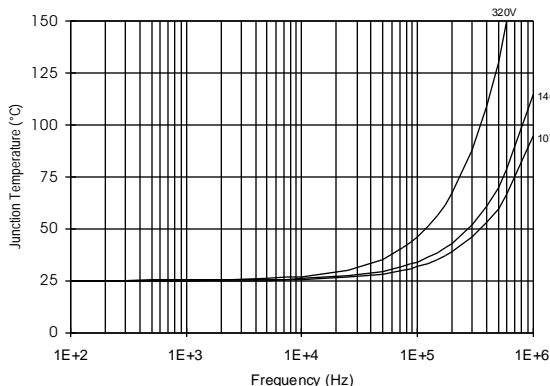


Figure 30. IR2112 T_J vs. Frequency (IRFBC40)
 $R_{GATE} = 15\Omega, V_{CC} = 15V$

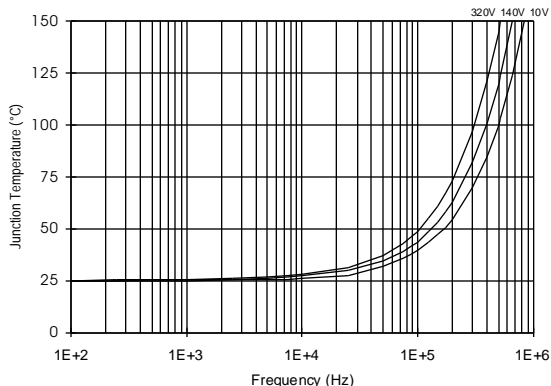


Figure 31. IR2112 T_J vs. Frequency (IRFPE50)
 $R_{GATE} = 10\Omega, V_{CC} = 15V$

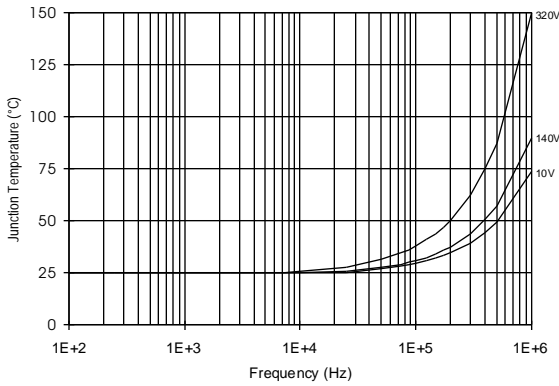


Figure 32. IR2112S T_J vs. Frequency (IRFBC20)
 $R_{GATE} = 33\Omega, V_{CC} = 15V$

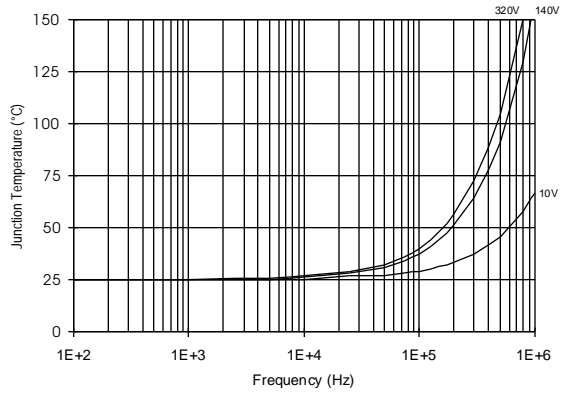


Figure 33. IR2112ST T_J vs. Frequency (IRFBC30)
 $R_{GATE} = 22\Omega, V_{CC} = 15V$

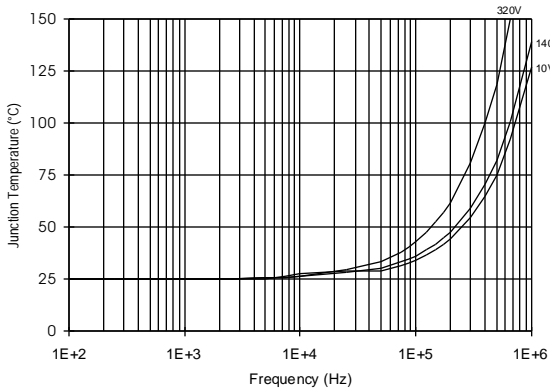


Figure 34. IR2112S T_J vs. Frequency (IRFBC40)
 $R_{GATE} = 15\Omega, V_{CC} = 15V$

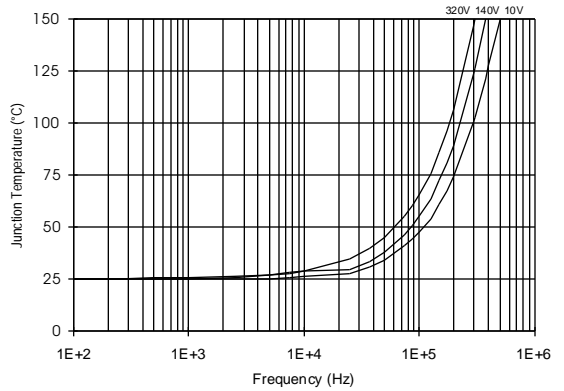


Figure 35. IR2112S T_J vs. Frequency (IRFPE50)
 $R_{GATE} = 10\Omega, V_{CC} = 15V$

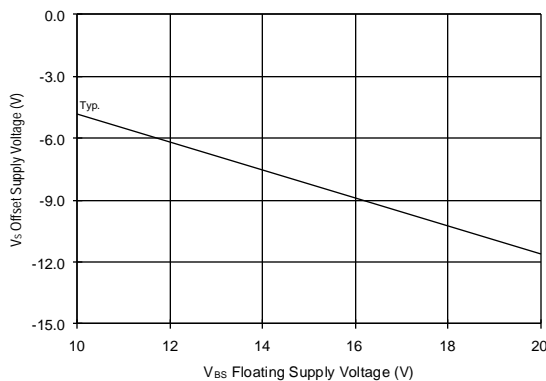


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

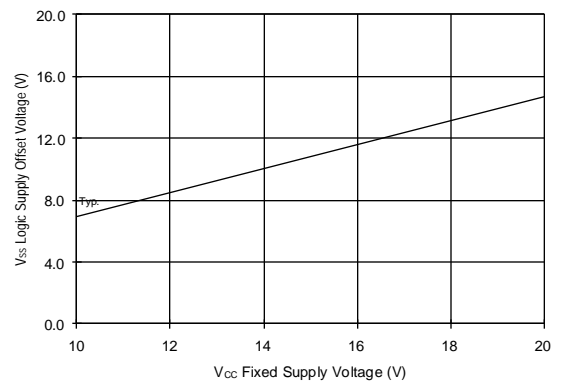


Figure 37. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage