



LC75391, 75391M

Single-Chip Electronic Volume Control System



Overview

The LC75391 and LC75391M are single-chip electronic volume and tone control systems that support volume control, tone control, and input and output signal switching functions controlled by serial input data.

Functions

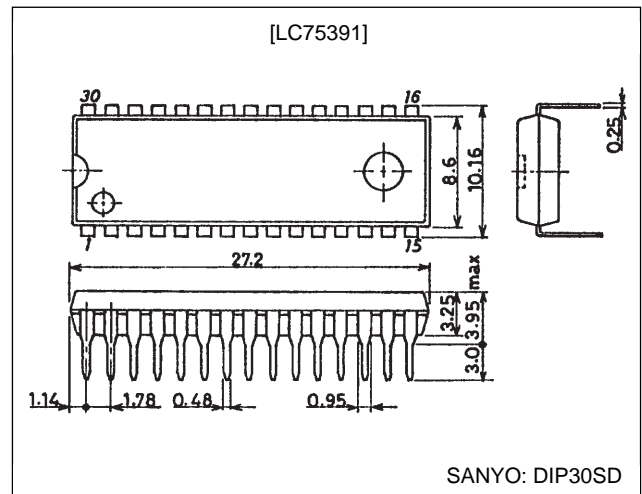
- Input and output signal switching: The four I/O switches can be set to on or off independently.
- Volume control: Independent control of the left and right channels can be used to implement a balance function.
0 to -20 dB in 2 dB steps, -20 to -32 dB in 3 dB steps, -32 to -53 dB in 4 dB steps, -52 to -70 dB in 4.5 dB steps, and -∞.
- Tone controls: Four frequency characteristic types selectable by setting internal switches.
Also supports a buffer function that requires no external components.
- Two general-purpose output ports: These ports allow this LSI to control motorized volume controls and general-purpose logic.

- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

Package Dimensions

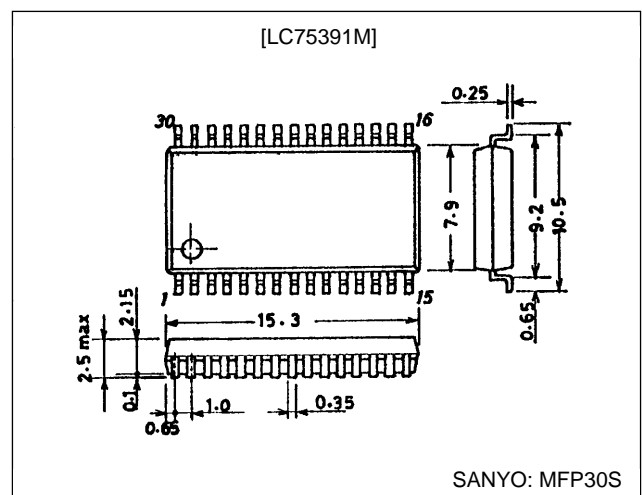
unit: mm

3196-DIP30SD



unit: mm

3216-MFP30S



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{DD} max	V _{DD}	12	V
Maximum input voltage	V _{IN} max	CL, DI, CE, L1 to L4, R1 to R4	V _{SS} - 0.3 to V _{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 85°C	160	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-50 to +125	°C

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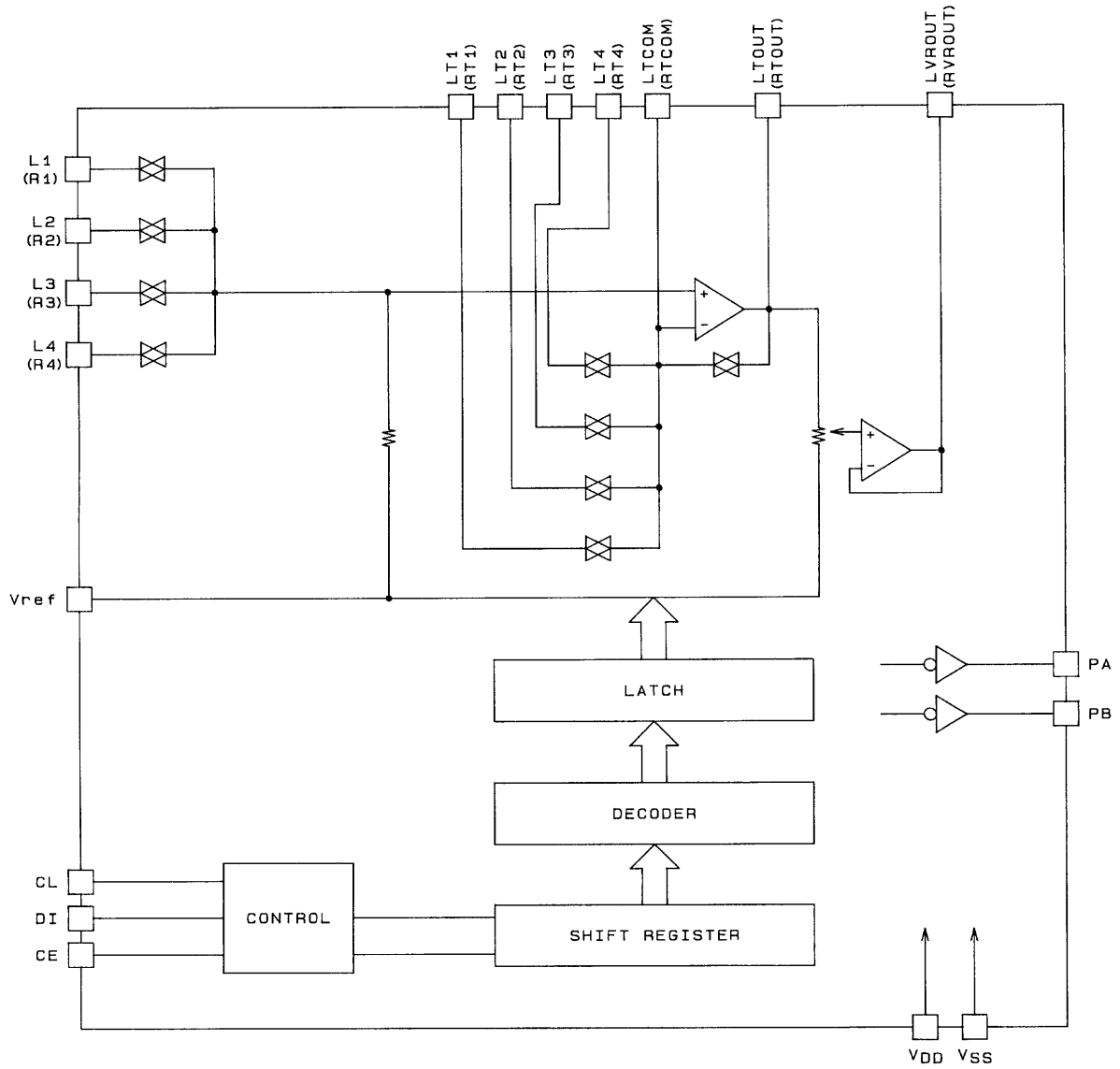
Allowable Operating Ranges at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	5.5		11.0	V
Input high-level voltage	V_{IH}	CL, DI, CE	4.0		V_{DD}	V
Input low-level voltage	V_{IL}	CL, DI, CE	V_{SS}		1.0	V
Output high-level voltage	V_{OH}	PA, PB: $I_O = 5\text{ mA}$	$V_{DD} - 2$		V_{DD}	V
Output low-level voltage	V_{OL}	PA, PB: $I_O = 5\text{ mA}$	V_{SS}		2.0	V
Input voltage amplitude	V_{IN}	L1 to L4, R1 to R4	V_{SS}		V_{DD}	Vp-p
Input pulse width	$t_{\phi W}$	CL	1.0			μs
Setup time	$t_{\text{set up}}$	CL, DI, CE	1.0			μs
Hold time	t_{hold}	CL, DI, CE	1.0			μs
Operating frequency	fopg	CL			500	kHz

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{DD} = 10\text{ V}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
[Input Block]						
Input resistance	R_{in}	L1 to L4, R1 to R4		500		k Ω
[Overall Characteristics]						
Total harmonic distortion	THD (1)	$V_{IN} = 100\text{ mVrms}$, $f = 1\text{ kHz}$, overall, buffer mode off, flat state		0.013		%
	THD (2)	$V_{IN} = 100\text{ mVrms}$, $f = 20\text{ kHz}$, overall, buffer mode off, flat state		0.013		%
Crosstalk	CT	$V_{IN} = 1\text{ Vrms}$, $f = 1\text{ kHz}$, overall, $R_g = 1\text{ k}\Omega$, buffer mode off, flat state		81		dB
Maximum attenuation	$V_{O\text{ min}}$	$V_{IN} = 1\text{ Vrms}$, $f = 1\text{ kHz}$, main volume at $-\infty$, buffer mode on		-80		dB
Output noise voltage	V_N (1)	Flat overall (IHF-A), $R_g = 1\text{ k}\Omega$, buffer mode off, flat state		15		μV
	V_N (2)	Flat overall (DIN-AUDIO), $R_g = 1\text{ k}\Omega$, buffer mode off, flat state		22		μV
Current drain	I_{DD}	$V_{DD} - V_{SS} = 11\text{ V}$		7	10	mA
Input high-level current	I_{IH}	CL, DI, CE, $V_{IN} = 10\text{ V}$			10	μA
Input low-level current	I_{IL}	CL, DI, CE, $V_{IN} = 0\text{ V}$	-10			μA

Equivalent Circuit Block Diagram

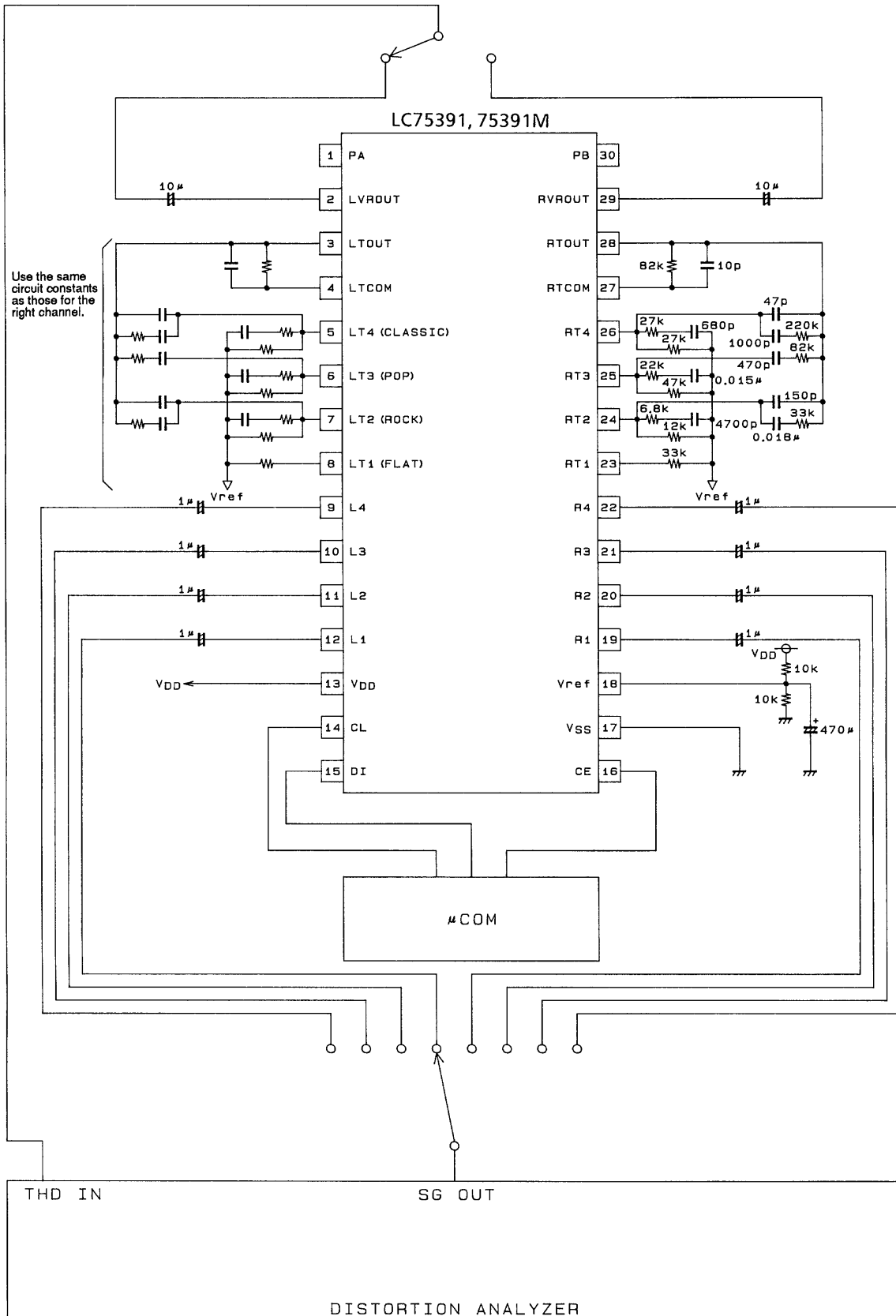


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Test Circuits

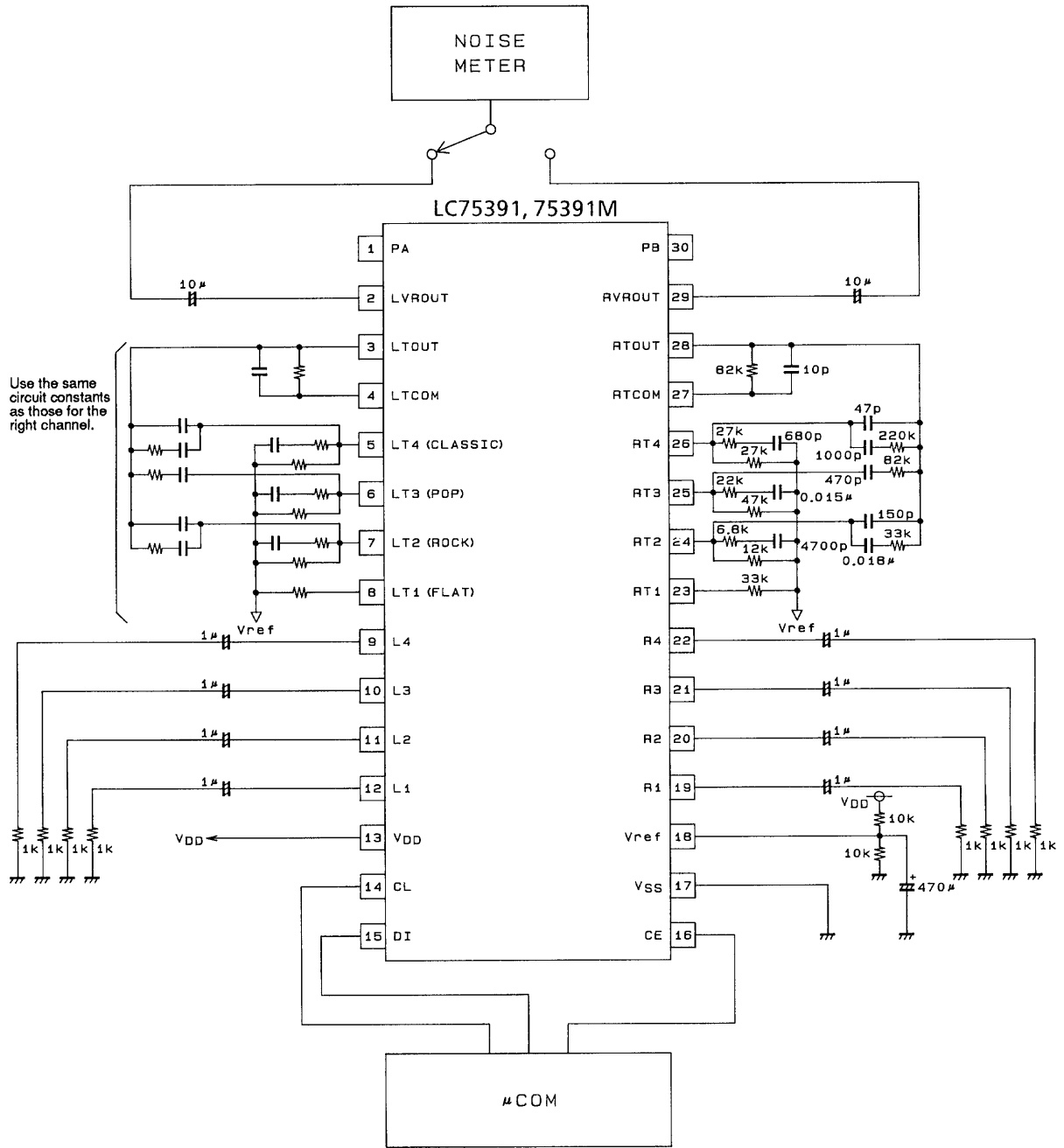
1. Total harmonic distortion



A04358
 Unit (resistance: Ω , capacitance: F)

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2. Output noise voltage

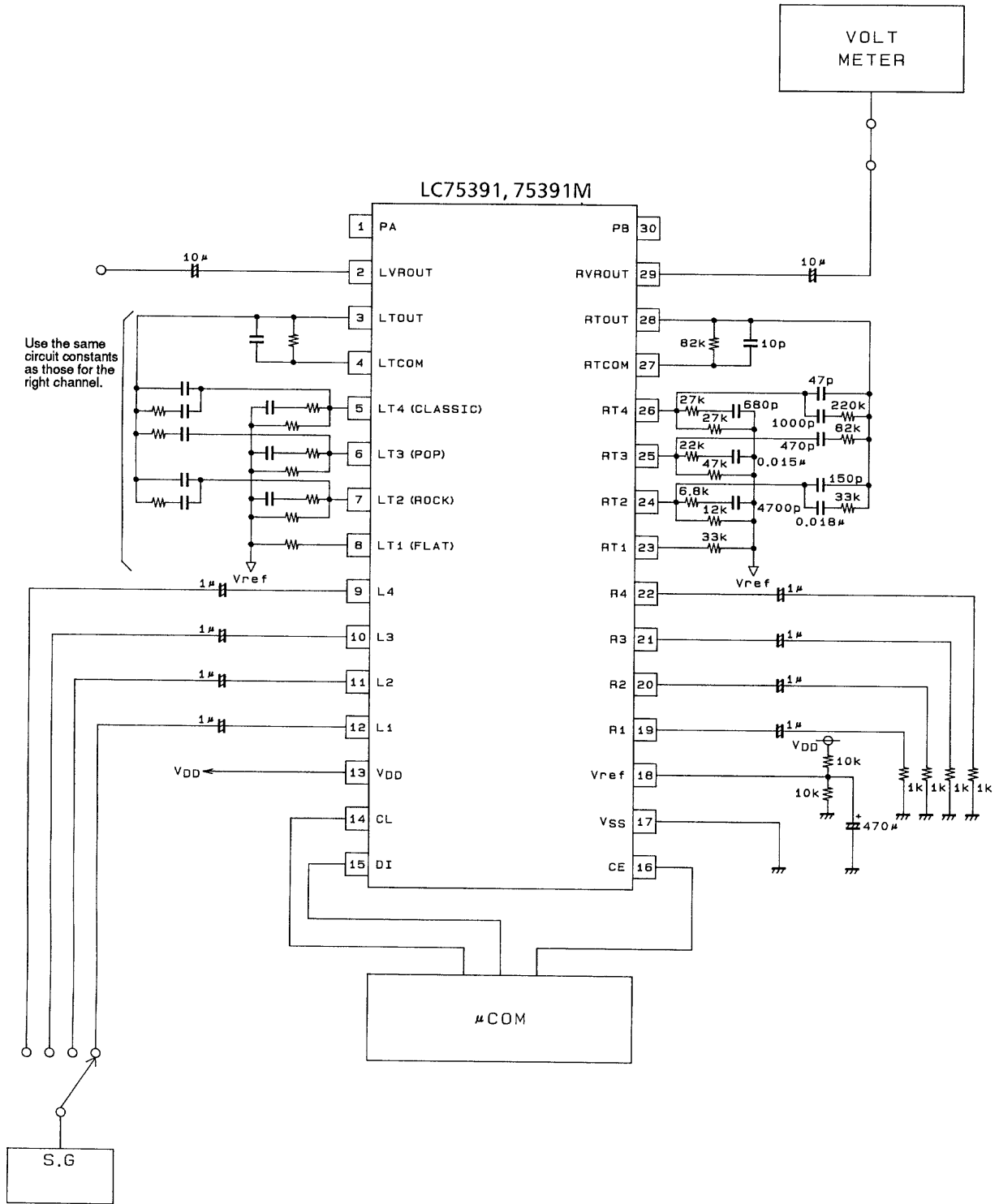


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Unit (resistance: Ω, capacitance: F)

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3. Crosstalk

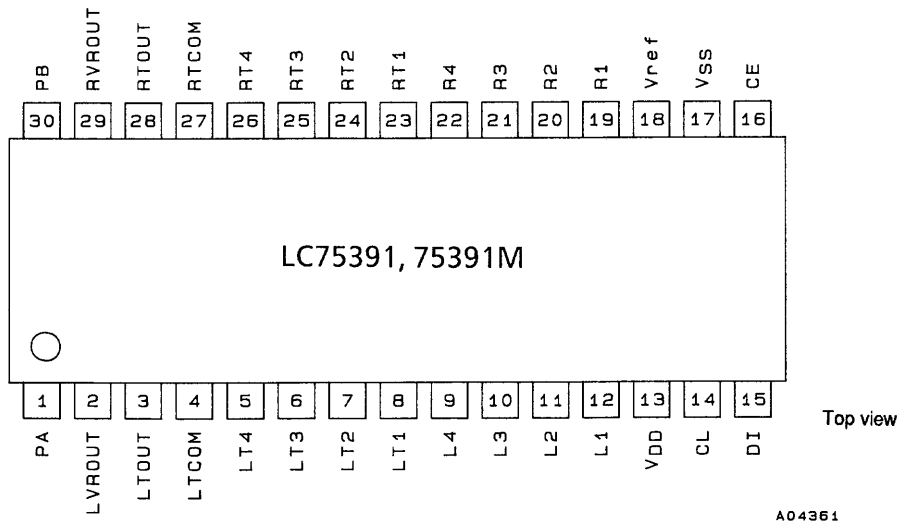


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Unit (resistance: Ω, capacitance: F)

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Pin Assignment



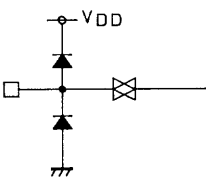
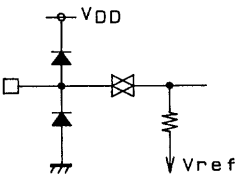
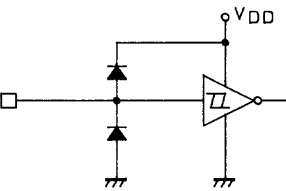
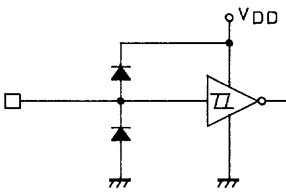
Pin Functions

Pin No.	Symbol	Function	Circuit configuration
1 30	PA PB	Digital CMOS output port	<p style="text-align: right;">A04362</p>
2 29	LVRROUT RVRROUT	Volume control circuit outputs	<p style="text-align: right;">A04363</p>
3 28	LTOUT RTOUT	Tone control circuit outputs	<p style="text-align: right;">A04364</p>
4 27	LTCOM RTCOM	Tone control circuit operational amplifier inverting inputs	

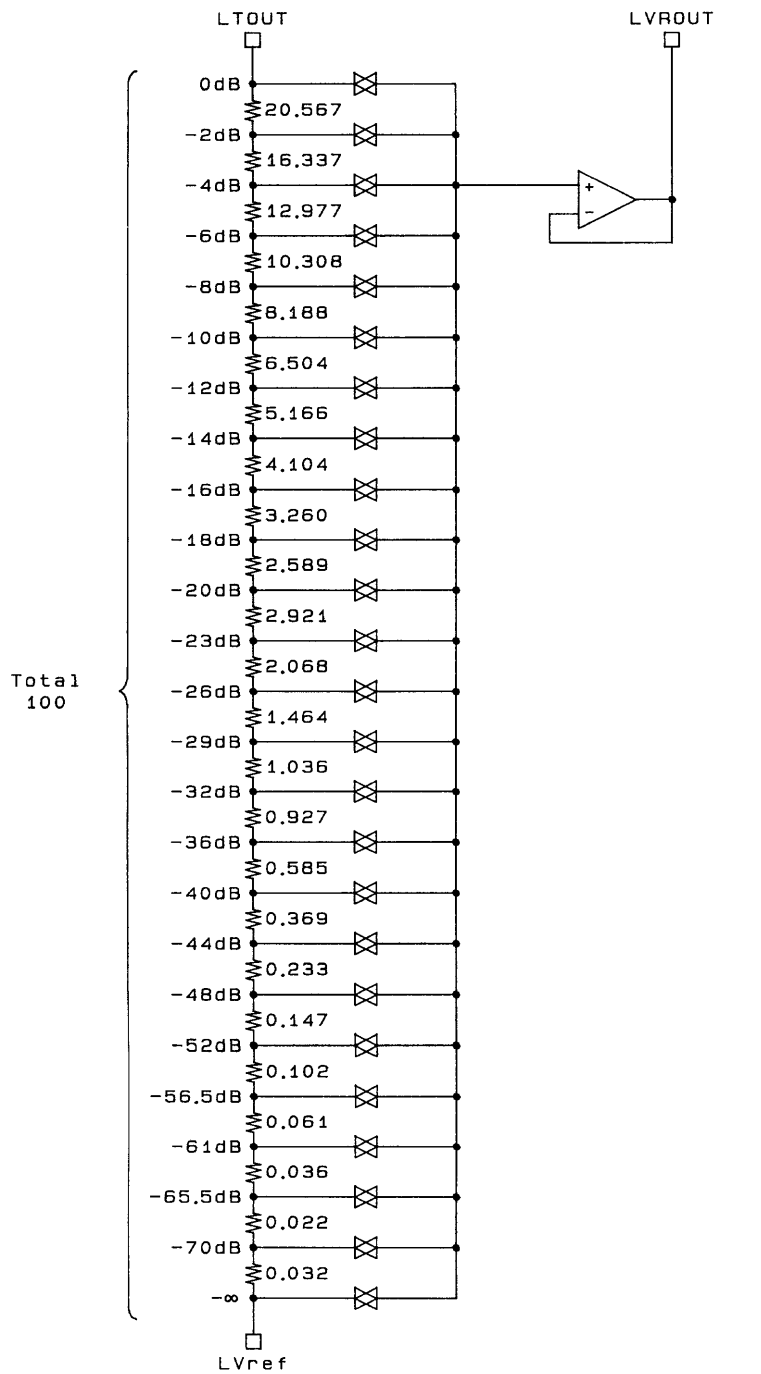
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Pin No.	Symbol	Function	Circuit configuration
8 7 6 5 23 24 25 26	LT1 LT2 LT3 LT4 RT1 RT2 RT3 RT4	Connections for the external components that determine the tone control pattern	 <p style="text-align: right;">A04365</p>
12 11 10 9 19 20 21 22	L1 L2 L3 L4 R1 R2 R3 R4	Audio signal inputs and outputs	 <p style="text-align: right;">A04366</p>
13	V _{DD}	Power supply	
18	V _{ref}	Analog system ground	
17	V _{SS}	Ground	
14 15	CL DI	Serial data and clock inputs for device control	 <p style="text-align: right;">A04367</p>
16	CE	Chip enable Data is read into internal latches and all analog switches change state when this input changes from high to low. Data transfer is enabled when this input is high.	 <p style="text-align: right;">A04367</p>

Volume Control Equivalent Circuit

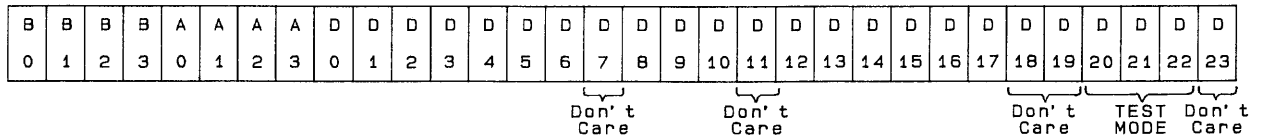
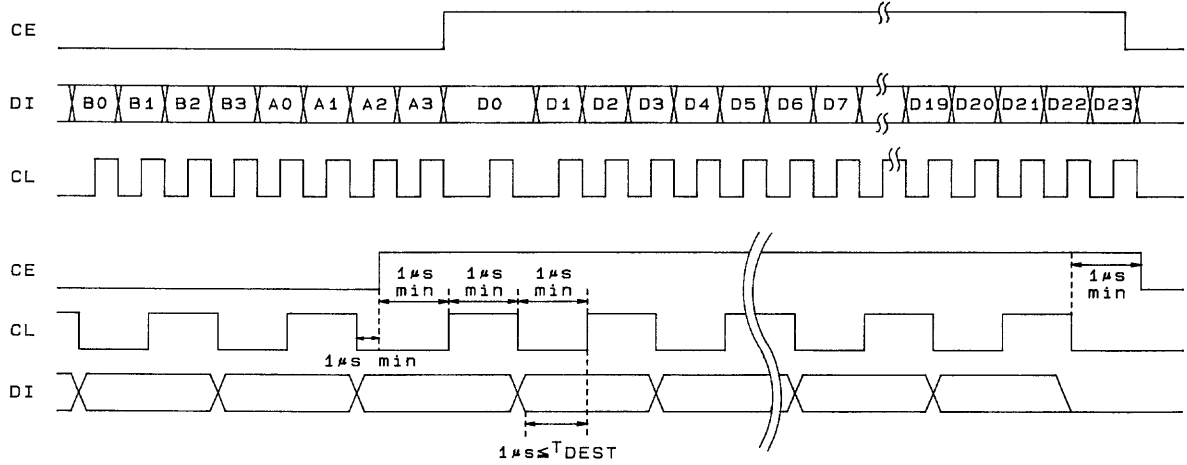


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The right channel is identical.
Unit (resistance: kΩ)

Control System Timing and Data Formats

The LC75391 is controlled by applying the stipulated data to the CE, CL, and DI pins. The data structure consists of a total of 32 bits, of which 8 bits are address and 24 bits are data.



Address code

Address code							
B	B	B	B	A	A	A	A
0	1	2	3	0	1	2	3
0	1	0	0	0	0	0	1

(B2HEX)

General-purpose port (PA) control data

D
0
0
1

Output low
Output high

General-purpose port (PB) control data

D
1
0
1

Output low
Output high

Volume control data

D	D	
2	5	
00000	-∞	
10000	-70dB	
01000	-65.5dB	
11000	-61dB	
00100	-56.5dB	
10100	-52dB	
01100	-48dB	
11100	-44dB	
00010	-40dB	
10010	-36dB	
01010	-32dB	
11010	-29dB	
00110	-26dB	
10110	-23dB	
01110	-20dB	
11110	-18dB	
00001	-16dB	
10001	-14dB	
01001	-12dB	
11001	-10dB	
00101	-8dB	
10101	-6dB	
01101	-4dB	
11101	-2dB	
00011	0dB	

Tone pattern control data

D	D	
8	9	
0	0	T1 ON
1	0	T2 ON
0	1	T3 ON
1	1	T4 ON

Buffer mode

D	
10	
0	T5 OFF
1	T5 ON

Channel selection

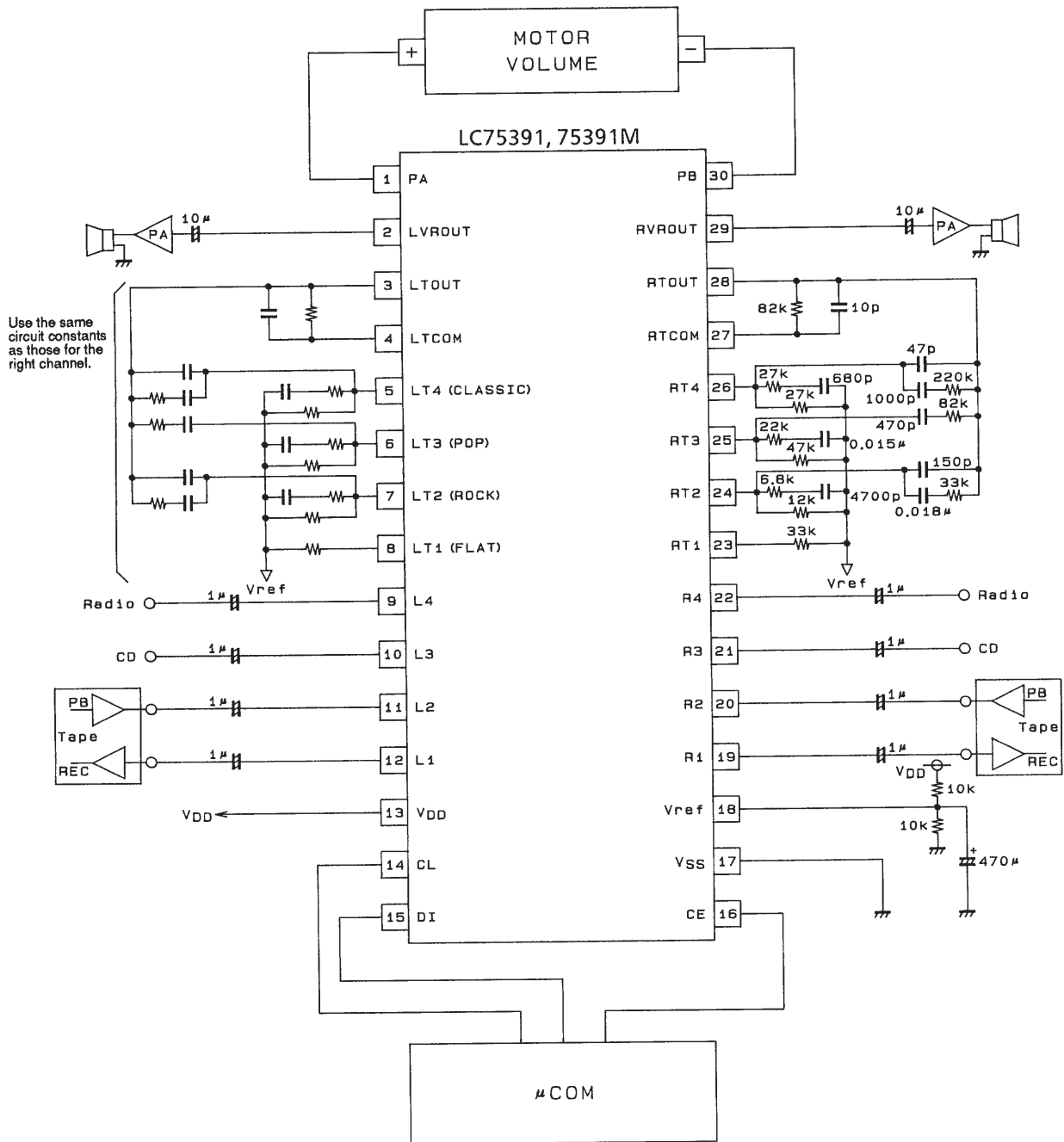
D	D	
16	17	
0	0	Lch
0	1	Rch
1	1	Left and right together

Function switch control data

D	
12	
0	L1 (R1) OFF
1	L1 (R1) ON
D	
13	
0	L2 (R2) OFF
1	L2 (R2) ON
D	
14	
0	L3 (R3) OFF
1	L3 (R3) ON
D	
15	
0	L4 (R4) OFF
1	L4 (R4) ON

Note: The bits D20, D21, and D22 are test mode selection bits. These bits must be set to 0 by user applications.

Application Circuit Example 1 (3-input type)



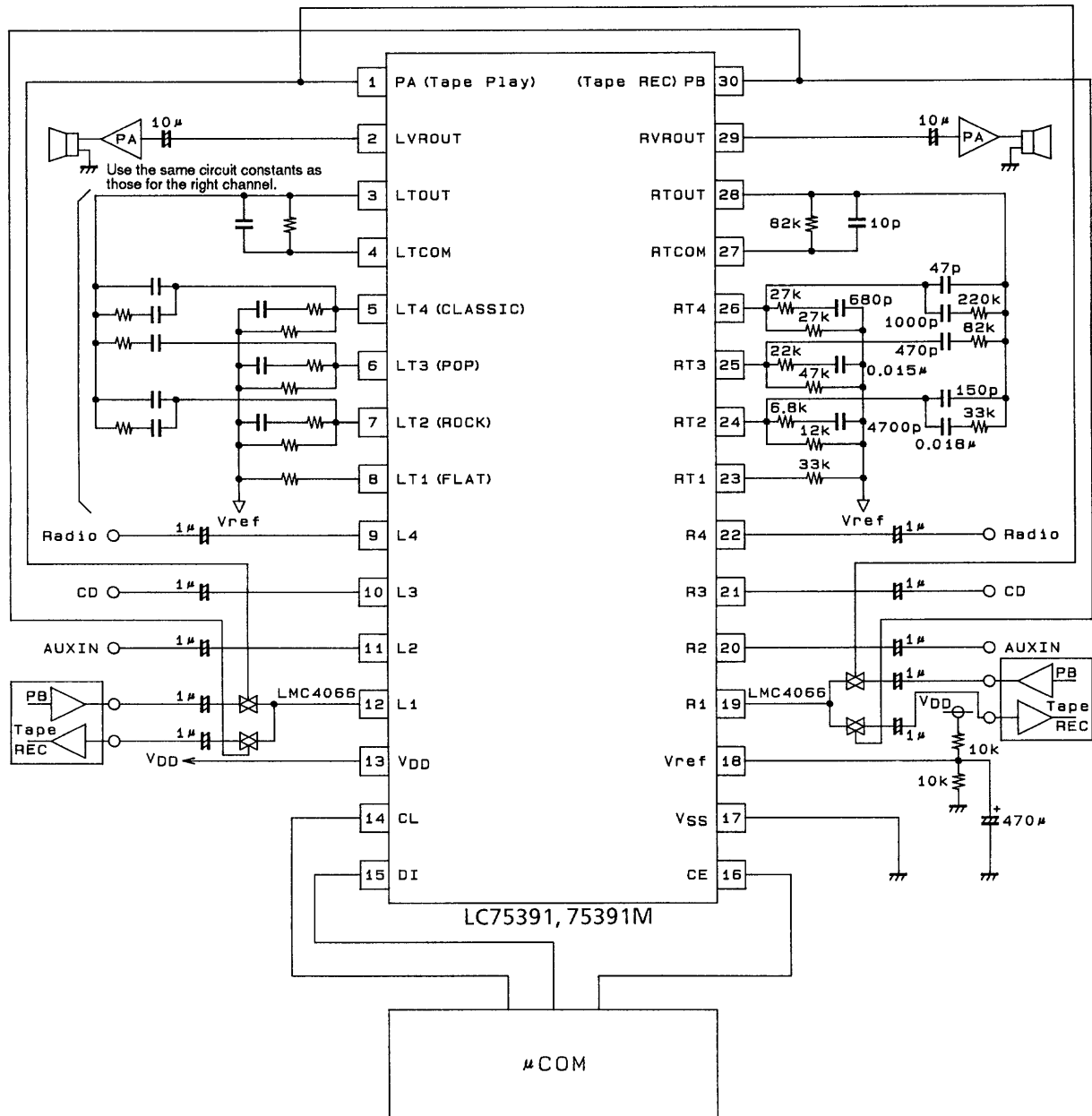
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Unit (resistance: Ω, capacitance: F)

Usage Notes

1. The internal analog switch states are undefined when power is first applied. Signals should be muted externally until the control data has been set up.
2. Cover the CL, DI, and CE pin signal lines with the ground pattern or use shielded cable for those lines to prevent the high-frequency digital signals transmitted to the CL, DI, and CE pins from entering the analog system as noise.
3. Use bipolar capacitors if at all possible for capacitors for which no polarity is indicated.
4. We recommend making large changes in the electronic volume control setting, such as from 0 dB to $-\infty$ dB, by using several intermediate steps as shown in the example below. This can reduce the switching noise associated with large changes.
Example: 0 dB \rightarrow -10 dB \rightarrow -20 dB \rightarrow -40 dB \rightarrow -70 dB \rightarrow $-\infty$

Application Circuit Example 2 (4-input type)

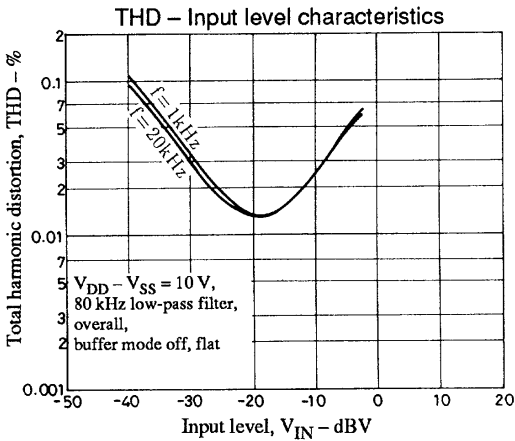
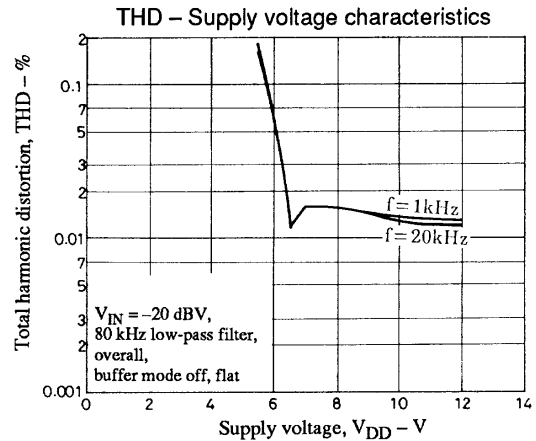
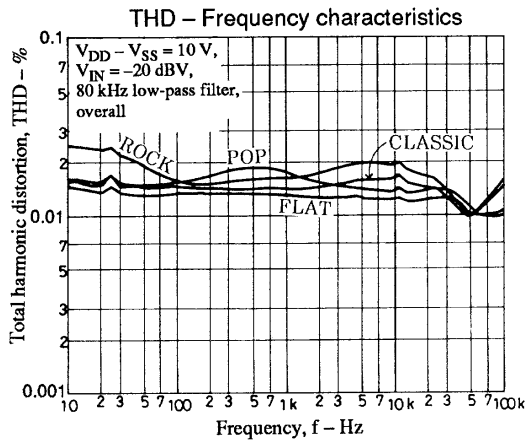
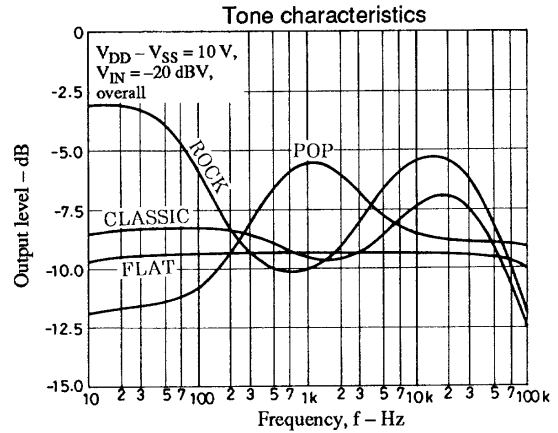
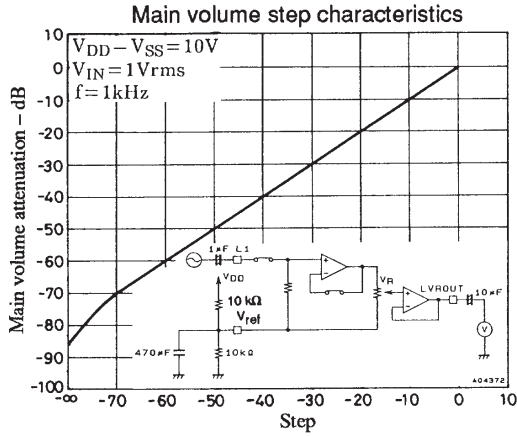


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Unit (resistance: Ω, capacitance: F)

Usage Notes

1. The internal analog switch states are undefined when power is first applied. Signals should be muted externally until the control data has been set up.
2. Cover the CL, DI, and CE pin signal lines with the ground pattern or use shielded cable for those lines to prevent the high-frequency digital signals transmitted to the CL, DI, and CE pins from entering the analog system as noise.
3. If at all possible, use bipolar capacitors for capacitors which have no polarity indicated.
4. We recommend using several intermediate steps as shown in the example below to make large changes in the electronic volume control setting, such as from 0 dB to $-\infty$ dB. This can reduce the switching noise associated with these large changes.
Example: 0 dB \rightarrow -10 dB \rightarrow -20 dB \rightarrow -40 dB \rightarrow -70 dB \rightarrow $-\infty$



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