

MC14584B

Hex Schmitt Trigger

The MC14584B Hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14584B may be used in place of the MC14069UB hex inverter for enhanced noise immunity to “square up” slowly changing waveforms.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Can Be Used to Replace MC14069UB
- For Greater Hysteresis, Use MC14106B which is Pin-for-Pin Replacement for CD40106B and MM74C14

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

| Symbol | Parameter | Value | Unit |
|-------------------|---|------------------------|--------------------|
| V_{DD} | DC Supply Voltage Range | -0.5 to +18.0 | V |
| V_{in}, V_{out} | Input or Output Voltage Range (DC or Transient) | -0.5 to $V_{DD} + 0.5$ | V |
| I_{in}, I_{out} | Input or Output Current (DC or Transient) per Pin | ± 10 | mA |
| P_D | Power Dissipation, per Package (Note 3.) | 500 | mW |
| T_A | Ambient Temperature Range | -55 to +125 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature Range | -65 to +150 | $^{\circ}\text{C}$ |
| T_L | Lead Temperature (8-Second Soldering) | 260 | $^{\circ}\text{C}$ |

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
Plastic “P and D/DW” Packages: - 7.0 mW/ $^{\circ}\text{C}$ From 65 $^{\circ}\text{C}$ To 125 $^{\circ}\text{C}$

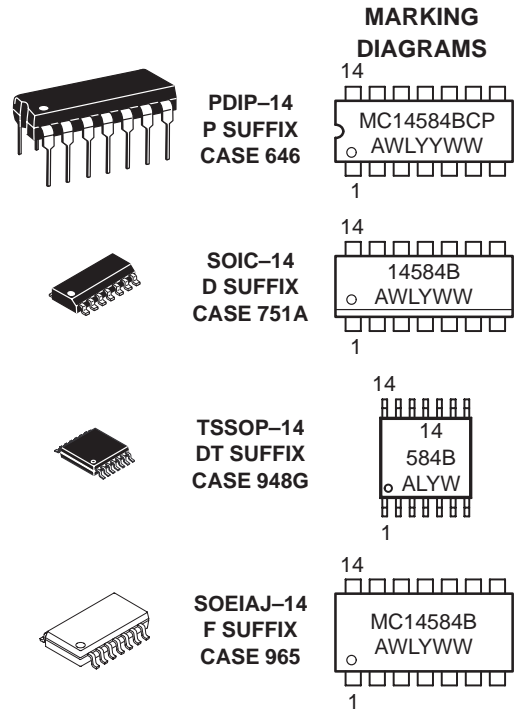
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



ON Semiconductor

<http://onsemi.com>



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

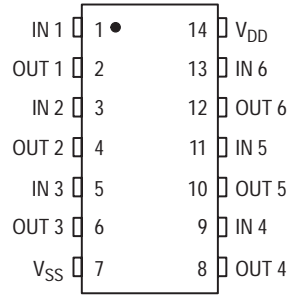
ORDERING INFORMATION

| Device | Package | Shipping |
|--------------|-----------|------------------|
| MC14584BCP | PDIP-14 | 2000/Box |
| MC14584BD | SOIC-14 | 55/Rail |
| MC14584BDR2 | SOIC-14 | 2500/Tape & Reel |
| MC14584BDT | TSSOP-14 | 96/Rail |
| MC14584BDTEL | TSSOP-14 | 2000/Tape & Reel |
| MC14584BF | SOEIAJ-14 | See Note 1. |
| MC14584BFEL | SOEIAJ-14 | See Note 1. |

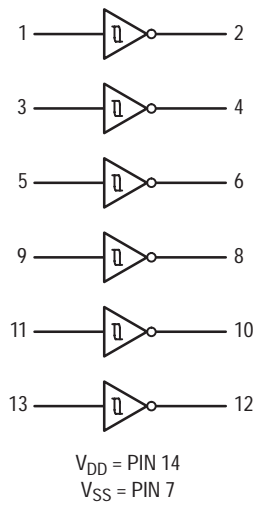
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

MC14584B

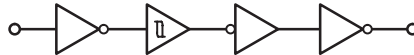
PIN ASSIGNMENT



LOGIC DIAGRAM



EQUIVALENT CIRCUIT SCHEMATIC (1/6 OF CIRCUIT SHOWN)



MC14584B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V_{DD} Vdc | - 55°C | | 25°C | | | 125°C | | Unit |
|--|-----------------------|-----------------|------------------------------------|------|-------|----------|------|-------|------|------|
| | | | Min | Max | Min | Typ (4.) | Max | Min | Max | |
| Output Voltage $V_{in} = V_{DD}$ $V_{in} = 0$ | "0" Level V_{OL} | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc |
| | | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| | | 15 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| | "1" Level V_{OH} | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | |
| | | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | |
| | | 15 | 14.95 | — | 14.95 | 15 | — | 14.95 | — | |
| Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc) ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc) | Source I_{OH} | 5.0 | -3.0 | — | -2.4 | -4.2 | — | -1.7 | — | mAdc |
| | | 5.0 | -0.64 | — | -0.51 | -0.88 | — | -0.36 | — | |
| | | 10 | -1.6 | — | -1.3 | -2.25 | — | -0.9 | — | |
| | | 15 | -4.2 | — | -3.4 | -8.8 | — | -2.4 | — | |
| | Sink I_{OL} | 5.0 | 0.64 | — | 0.51 | 0.88 | — | 0.36 | — | |
| | | 10 | 1.6 | — | 1.3 | 2.25 | — | 0.9 | — | |
| 15 | | 4.2 | — | 3.4 | 8.8 | — | 2.4 | — | | |
| Input Current | I_{in} | 15 | — | ±0.1 | — | ±0.00001 | ±0.1 | — | ±1.0 | μAdc |
| Input Capacitance ($V_{in} = 0$) | C_{in} | — | — | — | — | 5.0 | 7.5 | — | — | pF |
| Quiescent Current (Per Package) | I_{DD} | 5.0 | — | 0.25 | — | 0.0005 | 0.25 | — | 7.5 | μAdc |
| | | 10 | — | 0.5 | — | 0.0010 | 0.5 | — | 15 | |
| | | 15 | — | 1.0 | — | 0.0015 | 1.0 | — | 30 | |
| Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching) | I_T | 5.0 | $I_T = (1.8 \mu A/kHz) f + I_{DD}$ | | | | | | | μAdc |
| | | 10 | $I_T = (3.6 \mu A/kHz) f + I_{DD}$ | | | | | | | |
| | | 15 | $I_T = (5.4 \mu A/kHz) f + I_{DD}$ | | | | | | | |
| Hysteresis Voltage | V_H (7.) | 5.0 | 0.27 | 1.0 | 0.25 | 0.6 | 1.0 | 0.21 | 1.0 | Vdc |
| | | 10 | 0.36 | 1.3 | 0.3 | 0.7 | 1.2 | 0.25 | 1.2 | |
| | | 15 | 0.77 | 1.7 | 0.6 | 1.1 | 1.5 | 0.50 | 1.4 | |
| Threshold Voltage Positive-Going Negative-Going | V_{T+} | 5.0 | 1.9 | 3.5 | 1.8 | 2.7 | 3.4 | 1.7 | 3.4 | Vdc |
| | | 10 | 3.4 | 7.0 | 3.3 | 5.3 | 6.9 | 3.2 | 6.9 | |
| | | 15 | 5.2 | 10.6 | 5.2 | 8.0 | 10.5 | 5.2 | 10.5 | |
| | V_{T-} | 5.0 | 1.6 | 3.3 | 1.6 | 2.1 | 3.2 | 1.5 | 3.2 | Vdc |
| | | 10 | 3.0 | 6.7 | 3.0 | 4.6 | 6.7 | 3.0 | 6.7 | |
| | | 15 | 4.5 | 9.7 | 4.6 | 6.9 | 9.8 | 4.7 | 9.9 | |

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.001$.

7. $V_H = V_{T+} - V_{T-}$ (But maximum variation of V_H is specified as less than $V_{T+ \text{ max}} - V_{T- \text{ min}}$).

MC14584B

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | V_{DD} Vdc | Min | Typ (8.) | Max | Unit |
|------------------------|-----------------------|-----------------|-----|----------|-----|------|
| Output Rise Time | t_{TLH} | 5.0 | — | 100 | 200 | ns |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 40 | 80 | |
| Output Fall Time | t_{THL} | 5.0 | — | 100 | 200 | ns |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 40 | 80 | |
| Propagation Delay Time | t_{PLH} , t_{PHL} | 5.0 | — | 125 | 250 | ns |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 40 | 80 | |

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14584B

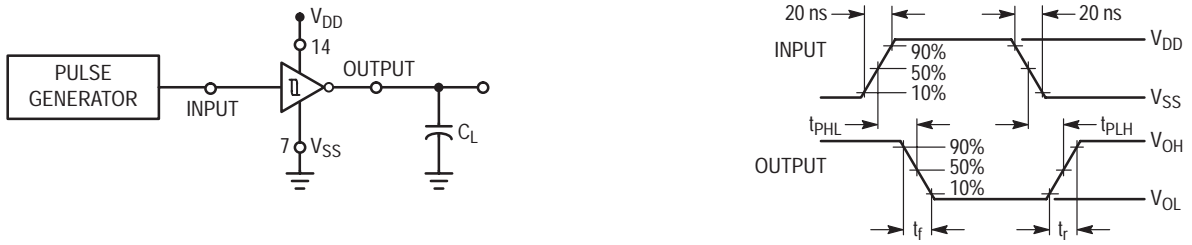


Figure 1. Switching Time Test Circuit and Waveforms

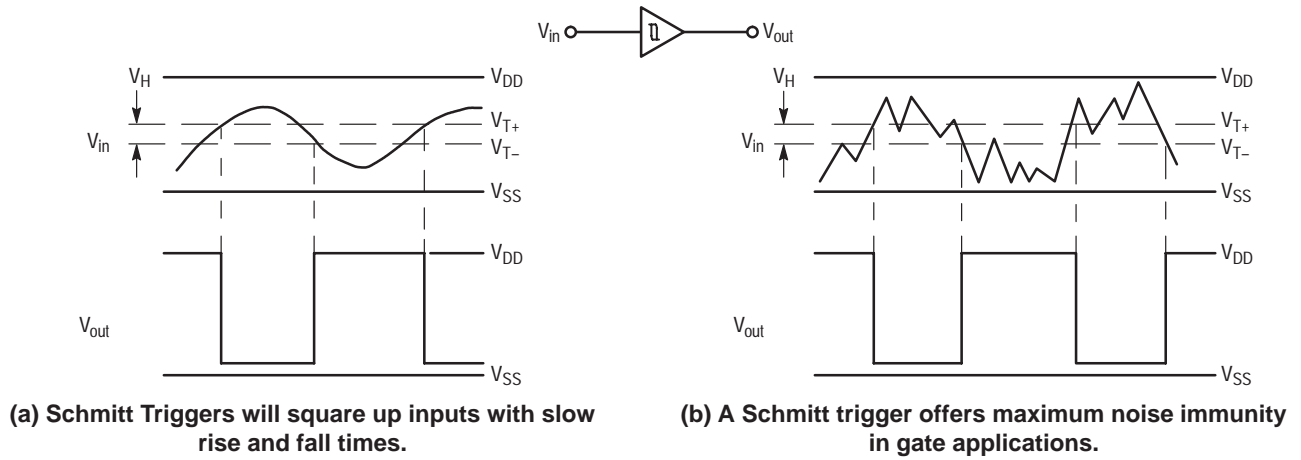


Figure 2. Typical Schmitt Trigger Applications

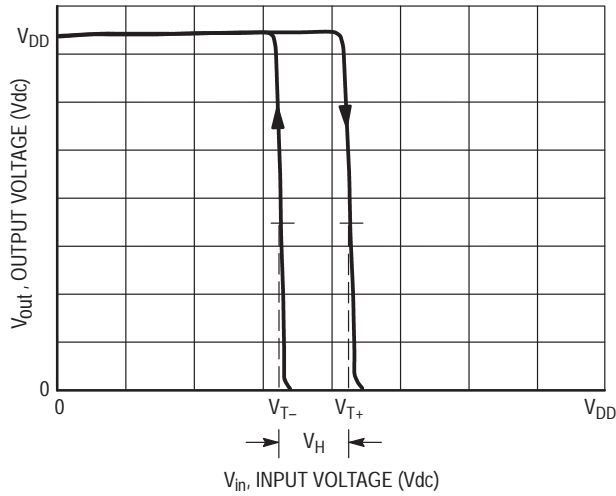
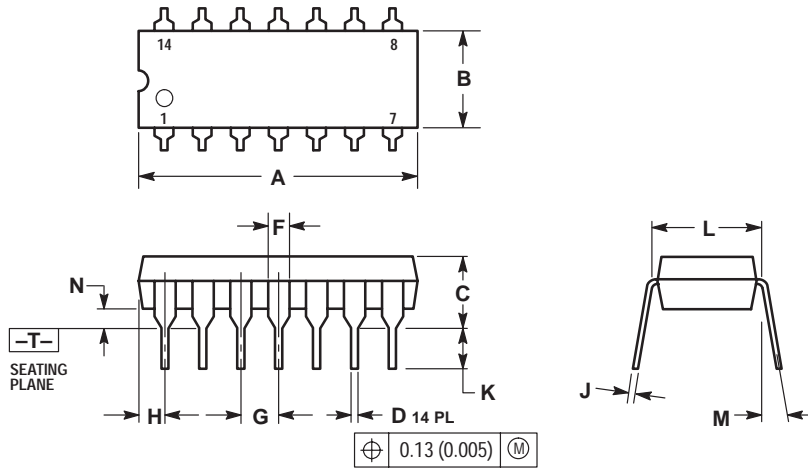


Figure 3. Typical Transfer Characteristics

MC14584B

PACKAGE DIMENSIONS

P SUFFIX PLASTIC DIP PACKAGE CASE 646-06 ISSUE M

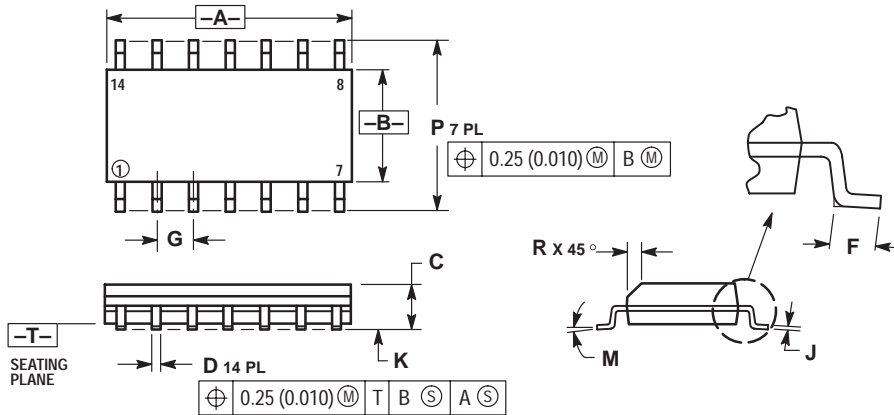


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 18.80 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.290 | 0.310 | 7.37 | 7.87 |
| M | --- | 10° | --- | 10° |
| N | 0.015 | 0.039 | 0.38 | 1.01 |

D SUFFIX PLASTIC SOIC PACKAGE CASE 751A-03 ISSUE F



NOTES:

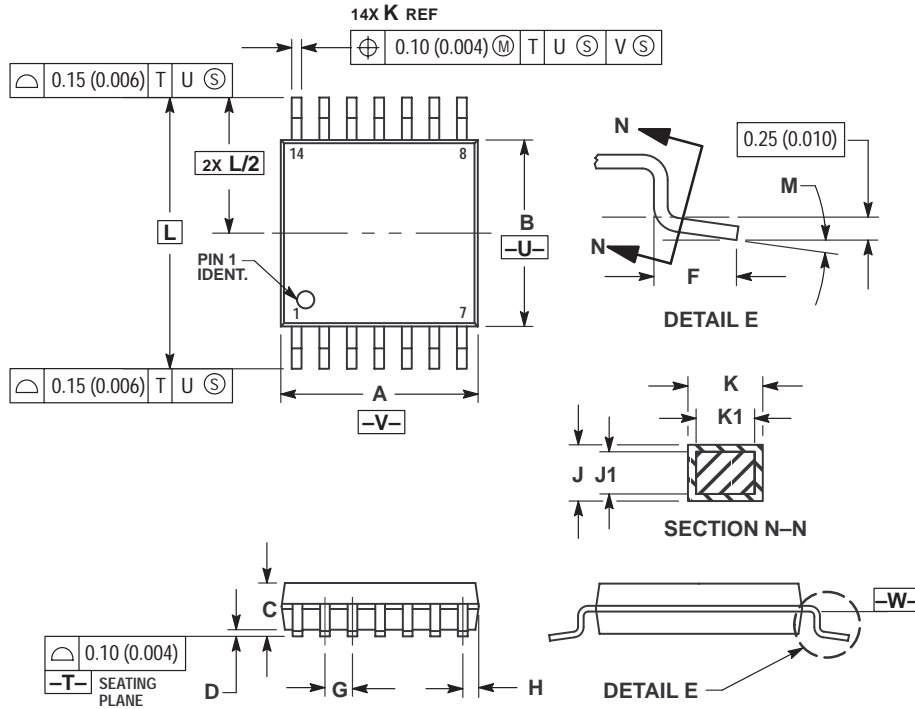
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.60 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

MC14584B

PACKAGE DIMENSIONS

DT SUFFIX
 PLASTIC TSSOP PACKAGE
 CASE 948G-01
 ISSUE O



NOTES:

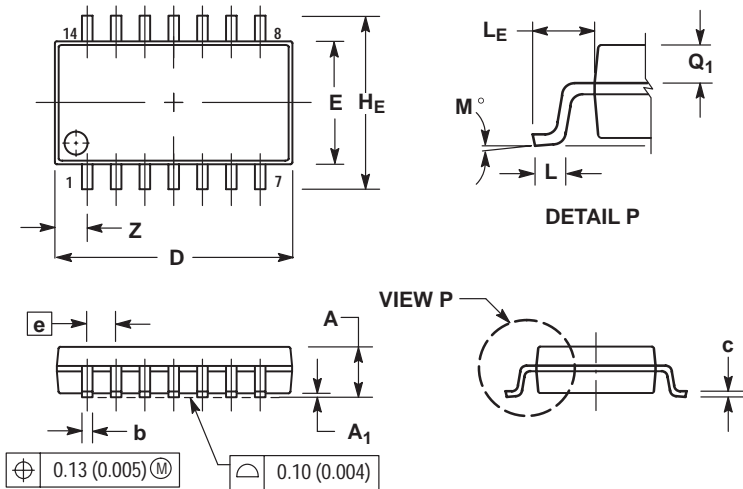
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE - W.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

MC14584B

PACKAGE DIMENSIONS


F SUFFIX PLASTIC EIAJ SOIC PACKAGE CASE 965-01 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | — | 2.05 | — | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| HE | 7.40 | 8.20 | 0.291 | 0.323 |
| 0.50 | 0.50 | 0.85 | 0.020 | 0.033 |
| LE | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | — | 1.42 | — | 0.056 |

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (M-F 1:00pm to 5:00pm Munich Time)
Email: ONlit-german@hibbertco.com
French Phone: (+1) 303-308-7141 (M-F 1:00pm to 5:00pm Toulouse Time)
Email: ONlit-french@hibbertco.com
English Phone: (+1) 303-308-7142 (M-F 12:00pm to 5:00pm UK Time)
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, England, Ireland

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)
Email: ONlit-spanish@hibbertco.com

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001-800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549
Phone: 81-3-5740-2745
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.