

Z86233/243

CMOS Z8® 8K ROM

CONSUMER CONTROLLER PROCESSOR

FEATURES

| Part | ROM Kbytes | RAM bytes | I/O | Package Information |
|--------|---------------|--------------|-----|---|
| Z86233 | 8 | 237 | 24 | 28-pinDIP,SOIC,PLCC |
| Z86243 | 8 | 236 | 32 | 40-pin DIP, 44-pin PLCC, 44-pin QFP |

- 3.0-to 5.5-Volt Operating Range
- Low-Power Consumption: 40 mW (Typical @5.0V)
- 0°C to +70°C Temperature Range
(-40°C to +105°C Temperature Range Available)
- Three Expanded Register File Control Registers
- Z86C33/C43 Pin and Package Compatible Version
(With Addition of 4K ROM)
- 32 Input/Output Lines (Three with Comparator Inputs)
(Z86243 Only)
- Vectored, Prioritized Interrupts with Programmable
Polarity
- Two Comparators
- Two Programmable 8-Bit Counter/Timers, Each
with a 6-Bit Programmable Prescaler
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- On-Chip Oscillator that Accepts a Crystal, Ceramic
Resonator, LC, RC, or External Clock Drive
- RAM and ROM Protect
- Clock Free Watch-Dog Timer (WDT) Reset

GENERAL DESCRIPTION

The Z86233/243 Consumer Controller Processor is a member of Zilog's Z8® single-chip microcontroller family featuring enhanced wake-up circuitry, programmable Watch-Dog timers and low-EMI options. The parts provide flexible and efficient growth paths for designers currently using the 4K ROM versions of the consumer controller devices (Z86C30/C40/C33/C43).

Four address spaces, the Program Memory, Register File, Data Memory and Expanded Register File (ERF), support a wide range of memory configurations. Through the ERF, the designer has access to two additional control registers which provide extra peripheral devices, I/O ports, and register addresses.

For applications demanding powerful I/O capabilities, the Z86243 provides 32 pins dedicated to input and output. The Z86233 provides 24 pins dedicated to input and output. These lines are grouped into four ports with eight lines each, and are configurable under software control to provide timing, status signals, or parallel I/O.

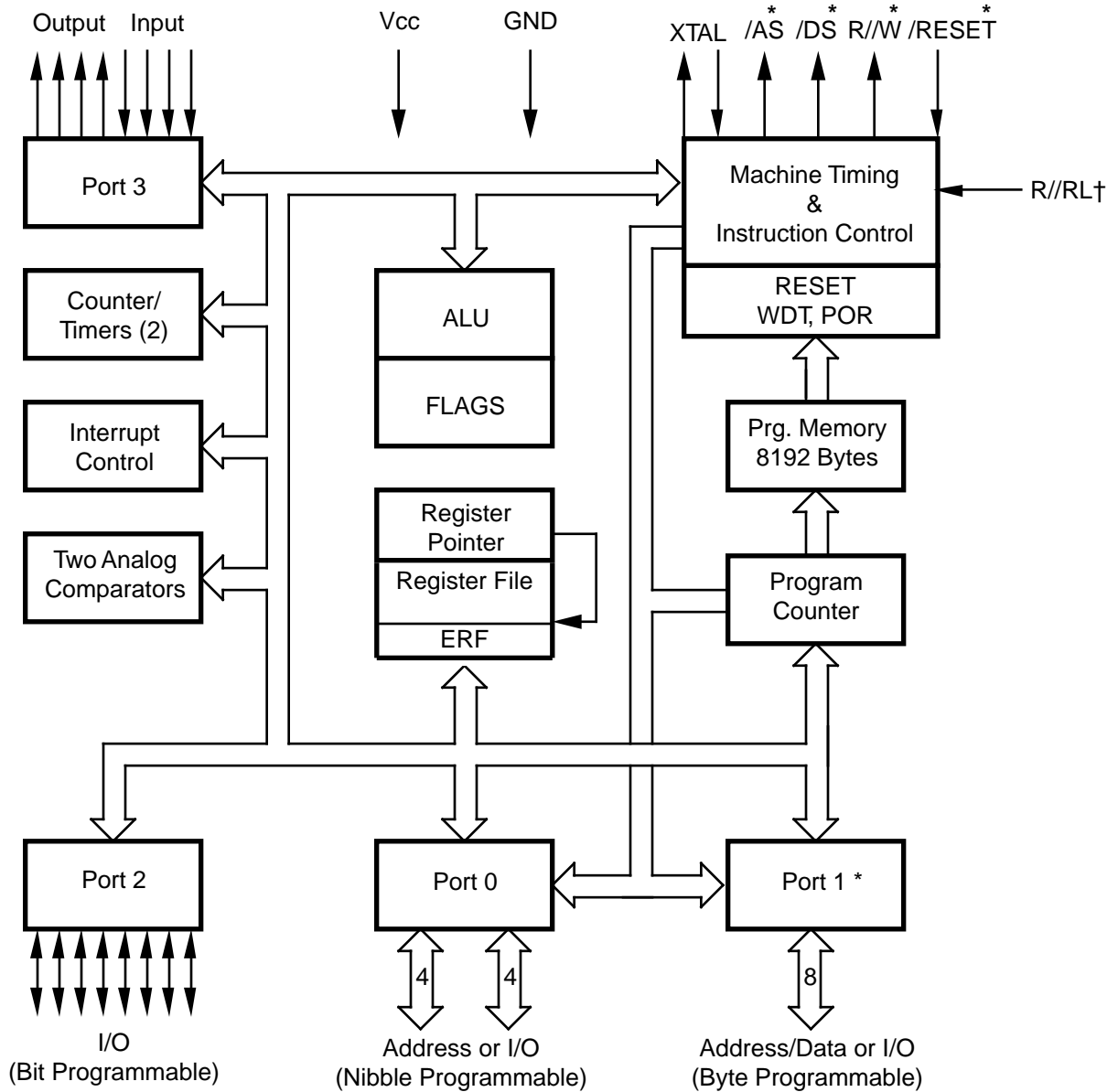
With ROM/ROMless selectivity, the Z86243 provides both external memory and pre-programmed ROM, which enables this Z8 microcontroller to be used in high-volume applications, or where code flexibility is required.

Note: All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

| Connection | Circuit | Device |
|-----------------|-----------------|----------------------|
| Power Ground | V_{CC} GND | V_{DD} V_{SS} |

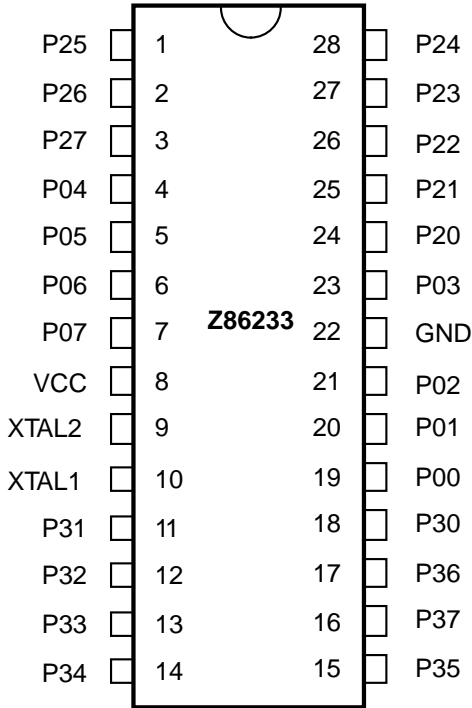
GENERAL DESCRIPTION (Continued)



* Not available on Z86233.
† Available on Z86243 44-Pin QFP and PLCC versions only.

Functional Block Diagram

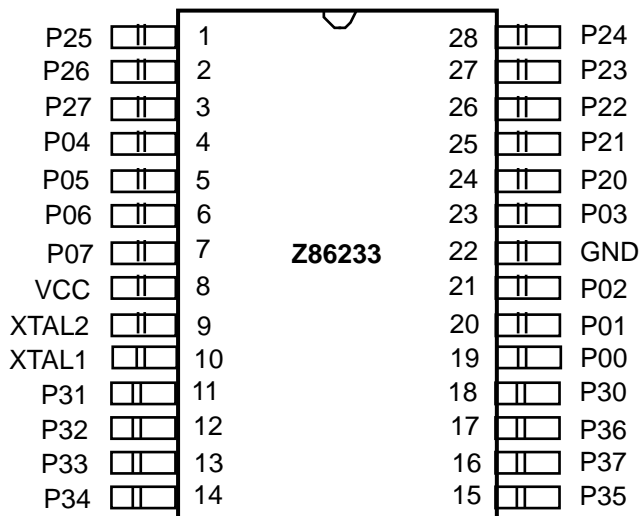
PIN DESCRIPTION



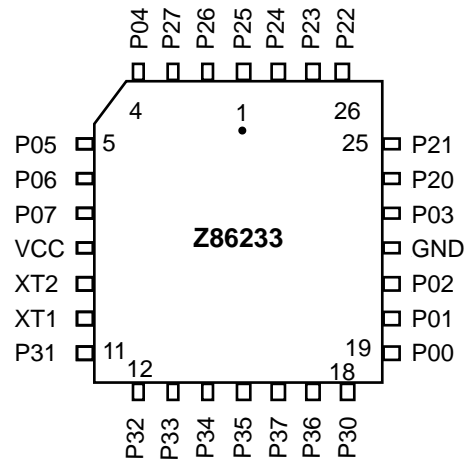
28-Pin DIP Pin Configuration

28-Pin DIP/SOIC/PLCC Pin Identification

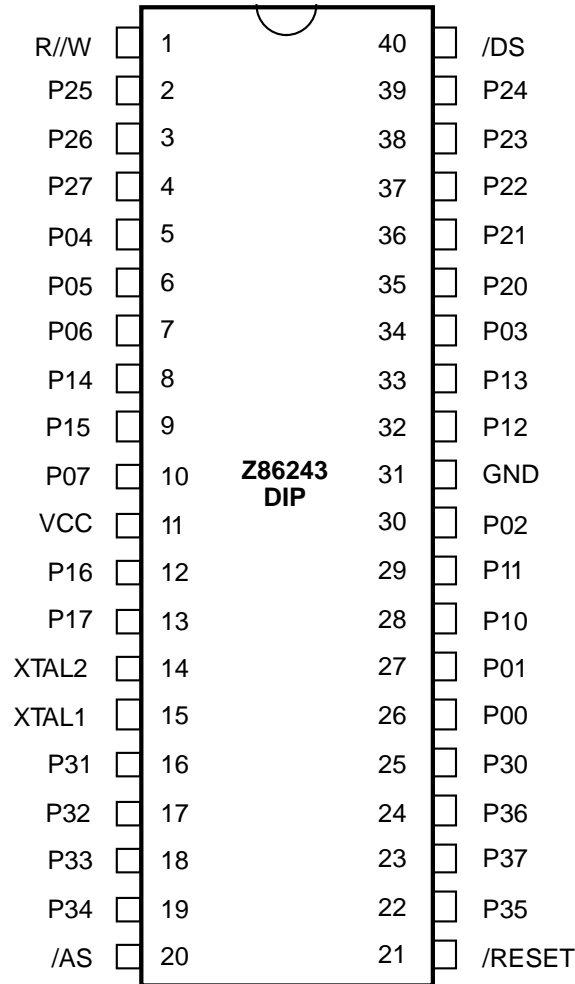
| Pin # | Symbol | Function | Direction |
|-------|-----------------|------------------------|--------------|
| 1-3 | P25-P27 | Port 2, Pins 5,6,7 | In/Output |
| 4-7 | P07-P04 | Port 0, Pins 4,5,6,7 | In/Output |
| 8 | V _{CC} | Power Supply | |
| 9 | XTAL2 | Crystal Oscillator | Output |
| 10 | XTAL1 | Crystal Oscillator | Input |
| 11-13 | P33-P31 | Port 3, Pins 1,2,3 | Fixed Input |
| 14-15 | P35-P34 | Port 3, Pins 4,5 | Fixed Output |
| 16 | P37 | Port 3, Pin 7 | Fixed Output |
| 17 | P36 | Port 3, Pin 6 | Fixed Output |
| 18 | P30 | Port 3, Pin 0 | Fixed Input |
| 19-21 | P02-P00 | Port 0, Pins 0,1,2 | In/Output |
| 22 | GND | Ground | |
| 23 | P03 | Port 0, Pins 3 | In/Output |
| 24-28 | P24-P20 | Port 2, Pins 0,1,2,3,4 | In/Output |



28-Pin SOIC Pin Configuration

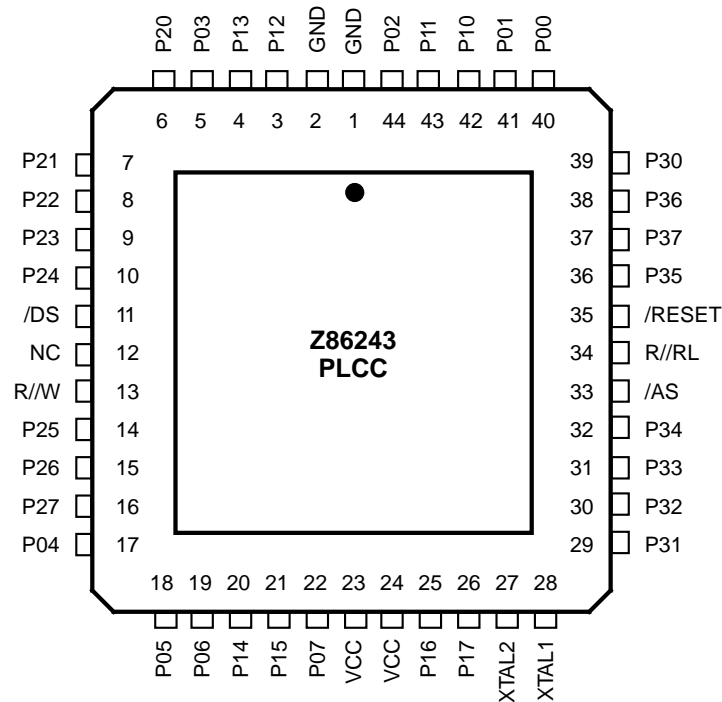


28-Pin PLCC Pin Configuration

PIN DESCRIPTION (Continued)

40-Pin DIP Pin Configuration
40-Pin DIP Pin Configuration

| Pin # | Symbol | Function | Direction |
|-------|-----------------|----------------------|-----------|
| 1 | R/W | Read/Write | Output |
| 2-4 | P25-P27 | Port 2, Pins 5, 6, 7 | In/Output |
| 5-7 | P04-P06 | Port 0, Pins 4, 5, 6 | In/Output |
| 8-9 | P14-P15 | Port 1, Pins 4, 5 | In/Output |
| 10 | P07 | Port 0, Pin 7 | In/Output |
| 11 | V _{cc} | Power Supply | |
| 12-13 | P16-P17 | Port 1, Pins 6, 7 | In/Output |
| 14 | XTAL2 | Crystal Oscillator | Output |
| 15 | XTAL1 | Crystal Oscillator | Input |
| 16-18 | P31-P33 | Port 3, Pins 1, 2, 3 | Input |
| 19 | P34 | Port 3, Pin 4 | Output |
| 20 | /AS | Address Strobe | Output |
| 21 | /RESET | Reset | Input |

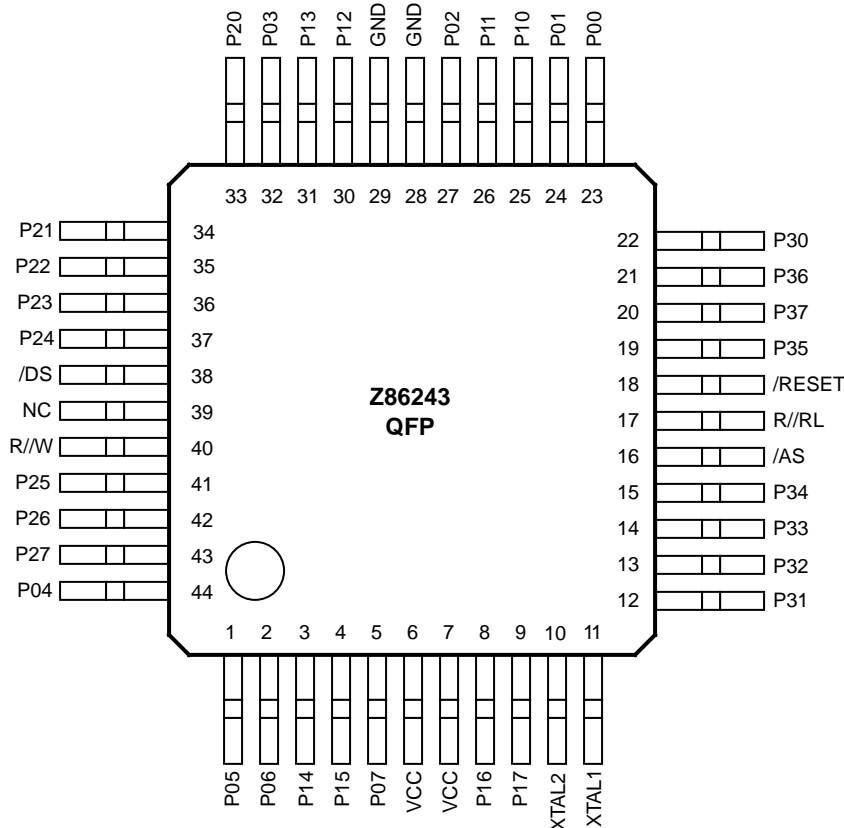
| Pin # | Symbol | Function | Direction |
|-------|---------|------------------------|-----------|
| 22 | P35 | Port 3, Pin 5 | Output |
| 23 | P37 | Port 3, Pin 7 | Output |
| 24 | P36 | Port 3, Pin 6 | Output |
| 25 | P30 | Port 3, Pin 0 | Input |
| 26-27 | P00-P01 | Port 0, Pins 0,1 | In/Output |
| 28-29 | P10-P11 | Port 1, Pins 0,1 | In/Output |
| 30 | P02 | Port 0, Pin 2 | In/Output |
| 31 | GND | Ground | |
| 32-33 | P12-P13 | Port 1, Pins 2, 3 | In/Output |
| 34 | P03 | Port 0, Pin 3 | In/Output |
| 35-39 | P20-P24 | Port 2, Pins 0,1,2,3,4 | In/Output |
| 40 | /DS | Data Strobe | Output |



44-Pin PLCC Pin Configuration

44-Pin PLCC Pin Identification

| Pin # | Symbol | Function | Direction | Pin # | Symbol | Function | Direction |
|-------|-----------------|------------------------|-----------|-------|---------|--------------------|-----------|
| 1 | GND | Ground | | 27 | XTAL2 | Crystal Oscillator | Output |
| 2 | GND | Ground | | 28 | XTAL1 | Crystal Oscillator | Input |
| 3-4 | P12-P13 | Port 1, Pins 2,3 | In/Output | 29-31 | P31-P33 | Port 3, Pins 1,2,3 | Input |
| 5 | P03 | Port 0, Pin 3 | In/Output | 32 | P34 | Port 3, Pin 4 | Output |
| 6-10 | P20-P24 | Port 2, Pins 0,1,2,3,4 | In/Output | 33 | /AS | Address Strobe | Output |
| 11 | /DS | Data Strobe | Output | 34 | R//RL | ROM/ROMless select | Input |
| 12 | N/C | Not Connected | | 35 | /RESET | Reset | Input |
| 13 | R/W | Read/Write | Output | 36 | P35 | Port 3, Pin 5 | Output |
| 14-16 | P25-P27 | Port 2, Pins 5,6,7 | In/Output | 37 | P37 | Port 3, Pin 7 | Output |
| 17-19 | P04-P06 | Port 0, Pins 4,5,6 | In/Output | 38 | P36 | Port 3, Pin 6 | Output |
| 20-21 | P14-P15 | Port 1, Pins 4,5 | In/Output | 39 | P30 | Port 3, Pin 0 | Input |
| 22 | P07 | Port 0, Pin 7 | In/Output | 40-41 | P00-P01 | Port 0, Pins 0,1 | In/Output |
| 23 | V _{CC} | Power Supply | | 42-43 | P10-P11 | Port 1, Pins 0,1 | In/Output |
| 24 | V _{CC} | Power Supply | | 44 | P02 | Port 0, Pin 2 | In/Output |
| 25-26 | P16-P17 | Port 1, Pins 6,7 | In/Output | | | | |

PIN DESCRIPTION (Continued)

44-Pin QFP Pin Configuration
44-Pin QFP Pin Identification

| Pin # | Symbol | Function | Direction | Pin # | Symbol | Function | Direction |
|-------|-----------------|--------------------|-----------|-------|---------|------------------------|-----------|
| 1-2 | P05-P06 | Port 0, Pins 5,6 | In/Output | 21 | P36 | Port 3, Pin 6 | Output |
| 3-4 | P14-P05 | Port 1, Pins 4,5 | In/Output | 22 | P30 | Port 3, Pin 0 | Input |
| 5 | P07 | Port 0, Pin 7 | In/Output | 23-24 | P00-P01 | Port 0, Pin 0,1 | In/Output |
| 6-7 | V _{CC} | Power Supply | | 25-26 | P10-P11 | Port 1, Pins 0,1 | In/Output |
| 8-9 | P16-P17 | Port 1, Pins 6,7 | In/Output | 27 | P02 | Port 0, Pin 2 | In/Output |
| 10 | XTAL2 | Crystal Oscillator | Output | 28 | GND | Ground | |
| 11 | XTAL1 | Crystal Oscillator | Input | 29 | GND | Ground | |
| 12-14 | P31-P33 | Port 3, Pins 1,2,3 | Input | 30-31 | P12-P13 | Port 1, Pins 2,3 | In/Output |
| 15 | P34 | Port 3, Pin 4 | Output | 32 | P03 | Port 0, Pin 3 | In/Output |
| 16 | /AS | Address Strobe | Output | 33-37 | P20-24 | Port 2, Pins 0,1,2,3,4 | In/Output |
| 17 | R//RL | ROM/ROMless select | Input | 38 | /DS | Data Strobe | Output |
| 18 | /RESET | Reset | Input | 39 | N/C | Not Connected | |
| 19 | P35 | Port 3, Pin 5 | Output | 40 | R//W | Read/Write | Output |
| 20 | P37 | Port 3, Pin 7 | Output | 41-43 | P25-P27 | Port 2, Pins 5,6,7 | In/Output |
| | | | | 44 | P04 | Port 0, Pin 4 | In/Output |

ABSOLUTE MAXIMUM RATINGS

| Parameter | Min | Max | Units |
|--|------|------------|---------|
| Ambient Temperature under Bias | -40 | +105 | C |
| Storage Temperature | -65 | +150 | C |
| Voltage on any Pin with Respect to V_{SS} [Note 1] | -0.6 | +7 | V |
| Voltage on V_{DD} Pin with Respect to V_{SS} | -0.3 | +7 | V |
| Voltage on XTAL1 and /RESET Pins with Respect to V_{SS} [Note 2] | -0.6 | $V_{DD}+1$ | V |
| Total Power Dissipation | | 1.21 | W |
| Maximum Allowable Current out of V_{SS} | | 220 | mA |
| Maximum Allowable Current into V_{DD} | | 180 | mA |
| Maximum Allowable Current into an Input Pin [Note 3] | -600 | +600 | μ A |
| Maximum Allowable Current into an Open-Drain Pin [Note 4] | -600 | +600 | μ A |
| Maximum Allowable Output Current Sunked by Any I/O Pin | | 25 | mA |
| Maximum Allowable Output Current Sourced by Any I/O Pin | | 25 | mA |

Notes:

- [1] This applies to all pins except XTAL pins and where otherwise noted.
 [2] There is no input protection diode from pin to V_{DD} .
 [3] This excludes XTAL pins.
 [4] Device pin is not at an output Low state.

Notice:

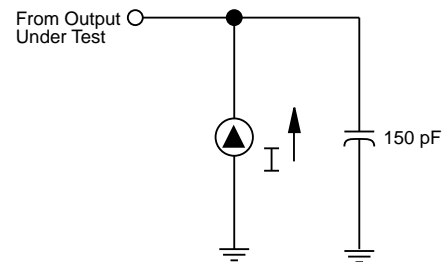
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 1.21 W for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] \\ + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] \\ + \text{sum of } (V_{OL} \times I_{OL})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Test Load).



Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{ MHz}$; unmeasured pins returned to GND.

| Parameter | Min | Max |
|--------------------|-----|-------|
| Input capacitance | 0 | 12 pF |
| Output capacitance | 0 | 12 pF |
| I/O capacitance | 0 | 12 pF |

DC ELECTRICAL CHARACTERISTICS

| Sym | Parameter | V _{CC} Note [3] | T _A = 0° C to +70°C | | T _A = -40°C to +105°C | | Typical [1] @ 25°C | Units | Conditions | Notes |
|---------------------|---------------------------------|-----------------------------|-----------------------------------|----------------------|-------------------------------------|----------------------|-----------------------|-------|--|-----------|
| | | | Min | Max | Min | Max | | | | |
| V _{CH} | Clock Input High Voltage | 3.0V | 0.7 V _{CC} | V _{CC} +0.3 | 0.7 V _{CC} | V _{CC} +0.3 | 1.8 | V | Driven by External Clock Generator | |
| | | 5.5V | 0.7 V _{CC} | V _{CC} +0.3 | 0.7 V _{CC} | V _{CC} +0.3 | 2.6 | V | Driven by External Clock Generator | |
| V _{CL} | Clock Input Low Voltage | 3.0V | GND-0.3 | 0.2 V _{CC} | GND-0.3 | 0.2 V _{CC} | 1.2 | V | Driven by External Clock Generator | |
| | | 5.5V | GND-0.3 | 0.2 V _{CC} | GND-0.3 | 0.2 V _{CC} | 2.1 | V | Driven by External Clock Generator | |
| V _{IH} | Input High Voltage | 3.0V | 0.7 V _{CC} | V _{CC} +0.3 | 0.7 V _{CC} | V _{CC} +0.3 | 1.8 | V | | |
| | | 5.5V | 0.7 V _{CC} | V _{CC} +0.3 | 0.7 V _{CC} | V _{CC} +0.3 | 2.6 | V | | |
| V _{IL} | Input Low Voltage | 3.0V | GND-0.3 | 0.2 V _{CC} | GND-0.3 | 0.2 V _{CC} | 1.1 | V | | |
| | | 5.5V | GND-0.3 | 0.2 V _{CC} | GND-0.3 | 0.2 V _{CC} | 1.6 | V | | |
| V _{OH1} | Output High Voltage | 3.0V | V _{CC} -0.4 | | V _{CC} -0.4 | | 3.1 | V | I _{OH} = -2.0 mA | [8] |
| | | 5.5V | V _{CC} -0.4 | | V _{CC} -0.4 | | 4.8 | V | I _{OH} = -2.0 mA | [8] |
| V _{OL1} | Output Low Voltage | 3.0V | | 0.6 | | 0.6 | 0.2 | V | I _{OL} = +4.0 mA | [8] |
| | | 5.5V | | 0.4 | | 0.4 | 0.1 | V | I _{OL} = +4.0 mA | [8] |
| V _{OL2} | Output Low Voltage | 3.0V | | 1.2 | | 1.2 | 0.3 | V | I _{OL} = +6 mA | [8] |
| | | 5.5V | | 1.2 | | 1.2 | 0.4 | V | I _{OL} = +12 mA | [8] |
| V _{RH} | Reset Input High Voltage | 3.0V | .8 V _{CC} | V _{CC} | .8 V _{CC} | V _{CC} | 1.8 | V | | [13] |
| | | 5.5V | .8 V _{CC} | V _{CC} | .8 V _{CC} | V _{CC} | 2.6 | V | | [13] |
| V _{RI} | Reset Input Low Voltage | 3.0V | GND-0.3 | 0.2 V _{CC} | GND-0.3 | 0.2 V _{CC} | 1.1 | V | | [13] |
| | | 5.5V | GND-0.3 | 0.2 V _{CC} | GND-0.3 | 0.2 V _{CC} | 1.6 | V | | [13] |
| V _{OLR} | Reset Output Low Voltage | 3.0V | | 0.6 | | 0.6 | 0.3 | V | I _{OL} = +1.0 mA | [13] |
| | | 5.5V | | 0.6 | | 0.6 | 0.2 | V | I _{OL} = +1.0 mA | [13] |
| V _{OFFSET} | Comparator Input Offset Voltage | 3.0V | | 25 | | 25 | 10 | mV | | [10] |
| | | 5.5V | | 25 | | 25 | 10 | mV | | [10] |
| I _{IL} | Input Leakage | 3.0V | -1 | 1 | -1 | 2 | 0.004 | μA | V _{IN} = 0V, V _{CC} | |
| | | 5.5V | -1 | 1 | -1 | 2 | 0.004 | μA | V _{IN} = 0V, V _{CC} | |
| I _{OL} | Output Leakage | 3.0V | -1 | 1 | -1 | 2 | 0.004 | μA | V _{IN} = 0V, V _{CC} | |
| | | 5.5V | -1 | 1 | -1 | 2 | 0.004 | μA | V _{IN} = 0V, V _{CC} | |
| I _{IR} | Reset Input Current | 3.0V | -20 | -130 | -18 | -130 | -60 | μA | | |
| | | 5.5V | -20 | -180 | -18 | -180 | -85 | μA | | |
| I _{CC} | Supply Current | 3.0V | | 20 | | 20 | 7 | mA | @ 16 MHz | [4] |
| | | 5.5V | | 25 | | 25 | 20 | mA | @ 16 MHz | [4] |
| | | 3.0V | | 15 | | 15 | 5 | mA | @ 12 MHz | [4] |
| | | 5.5V | | 20 | | 20 | 15 | mA | @ 12 MHz | [4] |
| I _{CC1} | Standby Current (Halt Mode) | 3.0V | | 4.5 | | 4.5 | 2.0 | mA | V _{IN} = 0V, V _{CC} @ 16 MHz | [4] |
| | | 5.5V | | 8 | | 8 | 3.7 | mA | V _{IN} = 0V, V _{CC} @ 16 MHz | [4] |
| | | 3.0V | | 3.4 | | 3.4 | 1.5 | mA | Clock Divide-by-16 @ 16 MHz | [4] |
| | | 5.5V | | 7.0 | | 7.0 | 2.9 | mA | Clock Divide-by-16 @ 16 MHz | [4] |
| I _{CC2} | Standby Current (Stop Mode) | 3.0V | | 8 | | 8 | 2 | μA | V _{IN} = 0V, V _{CC} WDT is not Running | [6,11] |
| | | 5.5V | | 10 | | 10 | 4 | μA | V _{IN} = 0V, V _{CC} WDT is not Running | [6,11] |
| | | 3.0V | | 500 | | 600 | 310 | μA | V _{IN} = 0V, V _{CC} WDT is Running | [6,11,14] |
| | | 5.5V | | 800 | | 1000 | 600 | μA | V _{IN} = 0V, V _{CC} WDT is Running | [6,11,14] |

DC ELECTRICAL CHARACTERISTICS (Continued)

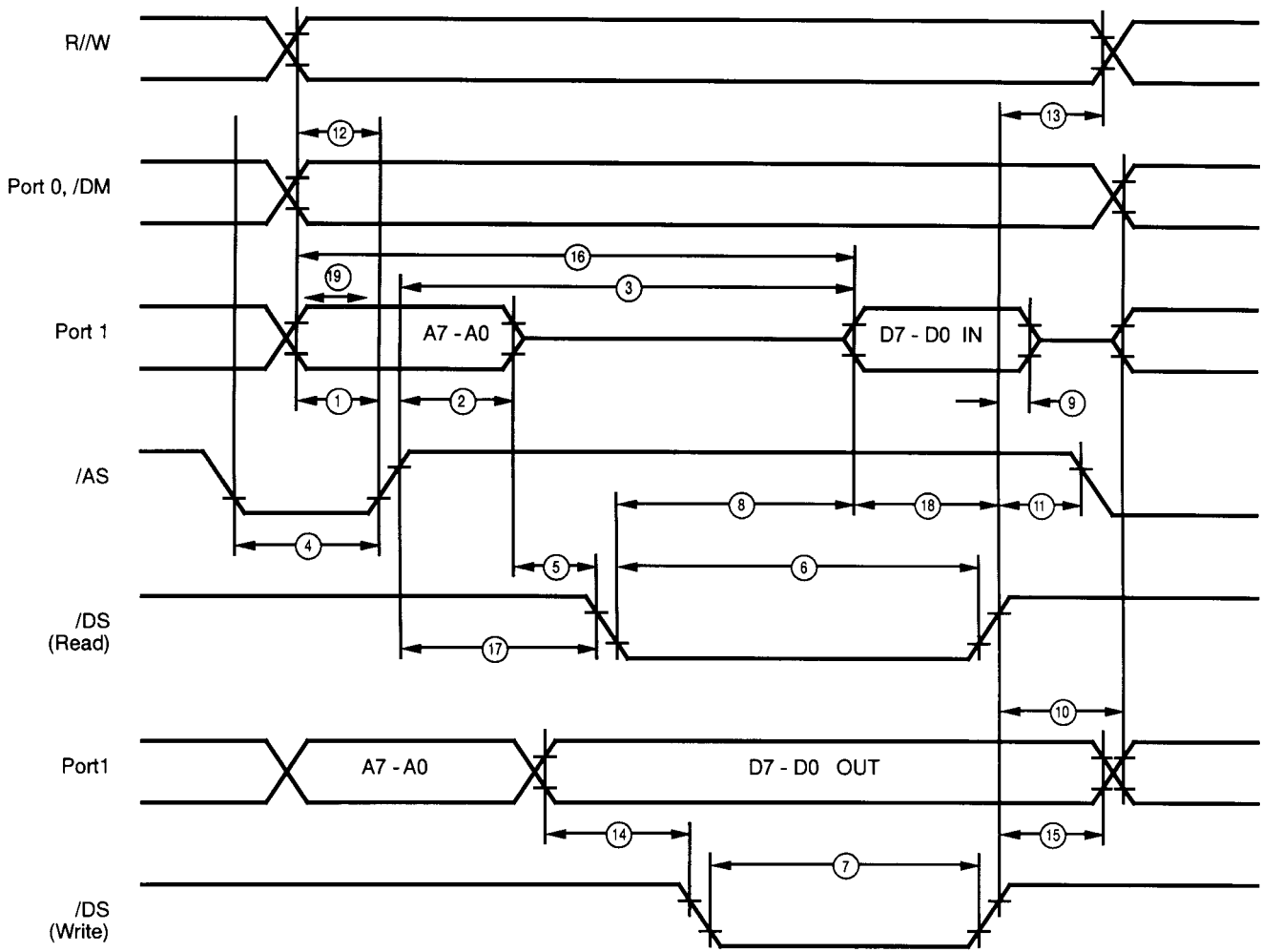
| Sym | Parameter | V _{CC} Note [3] | T _A = 0°C to +70°C | | T _A = -40°C to +105°C | | Typical [1] @ 25°C | Units | Conditions | Notes | |
|------------------|---|-----------------------------|----------------------------------|-----------------------|-------------------------------------|-----------------------|-----------------------|-------|--|---------------------------|--------|
| | | | Min | Max | Min | Max | | | | | |
| V ^{ICR} | Input Common Mode Voltage Range | 3.0 | GND-0.3 | V _{CC} -1.0V | GND-0.3 | V _{CC} -1.5V | | V | | [10] | |
| | | 5.5 | GND-0.3 | V _{CC} -1.0V | GND-0.3 | V _{CC} -1.5V | | V | | [10] | |
| I _{ALL} | Auto Latch Low Current | 3.0V | | 8 | | 10 | 3 | μA | 0V < V _{IN} < V _{CC} | [9] | |
| | | 5.5V | | 15 | | 20 | 5 | μA | 0V < V _{IN} < V _{CC} | [9] | |
| I _{ALH} | Auto Latch High Current | 3.0V | | -5 | | -7 | -3 | μA | 0V < V _{IN} < V _{CC} | [9] | |
| | | 5.5V | | -8 | | -10 | -6 | μA | 0V < V _{IN} < V _{CC} | [9] | |
| V _{LV} | V _{CC} Low Voltage Protection Voltage | | | | | 2.1 | 3.3 | 2.8 | V | 4 MHz max Int. CLK Freq. | [7,15] |
| | | | 2.4 | 3.1 | | | | 2.8 | V | 6 MHz max Int. CLK Freq. | [7,14] |
| V _{OH} | Output High Voltage (Low EMI Mode) | 3.3V | V _{CC} -0.4 | | V _{CC} -0.4 | | | 3.1 | V | I _{OH} = -0.5 mA | |
| | | 5.0V | V _{CC} -0.4 | | V _{CC} -0.4 | | | 4.8 | V | I _{OH} = -0.5 mA | |
| V _{OL} | Output Low Voltage (Low EMI Mode) | 3.3V | | 0.6 | | 0.6 | | 0.2 | V | I _{OL} = 1.0 mA | |
| | | 5.0V | | 0.4 | | 0.4 | | 0.1 | V | I _{OL} = 1.0 mA | |

Notes:

- [1] Typical values are at V_{CC} = 5.0V and 3.3V.
- [2] GND = 0V.
- [3] The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.
- [4] All outputs unloaded, I/O pins floating, inputs at rail.
- [5] CL1 = CL2 = 100 pF.
- [6] Same as note [4] except inputs at V_{CC}.
- [7] The V_{LV} increases as the temperature decreases.
- [8] Standard Mode (not Low EMI).
- [9] Auto Latch (Mask Option) selected.
- [10] For analog comparator, inputs when analog comparators are enabled.
- [11] Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
- [12] Excludes clock pins.
- [13] Z86243 Only.
- [14] 0°C to 70°C (standard temperature).
- [14] -40°C to 105°C (extended temperature).

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram



External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table
 (SCLK/TCLK = XTAL/2)

| No | Symbol | Parameter | Note [3] V _{cc} | T _A = 0°C to +70°C | | | | T _A = -40°C to +105°C | | | | Units | Notes |
|----|-----------|--|-----------------------------|-------------------------------|-----|--------|-----|----------------------------------|-----|--------|-----|-------|-------|
| | | | | 12 MHz | | 16 MHz | | 12 MHz | | 16 MHz | | | |
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| 1 | TdA(AS) | Address Valid to /AS Rise Delay | 3.0 | 35 | | 25 | | 35 | | 25 | | ns | [2] |
| | | | 5.5 | 35 | | 25 | | 35 | | 25 | | | |
| 2 | TdAS(A) | /AS Rise to Address Float Delay | 3.0 | 45 | | 35 | | 45 | | 35 | | ns | [2] |
| | | | 5.5 | 45 | | 35 | | 45 | | 35 | | ns | |
| 3 | TdAS(DR) | /AS Rise to Read Data Req'd Valid | 3.0 | | 250 | | 180 | | 250 | | 180 | ns | [1,2] |
| | | | 5.5 | | 250 | | 180 | | 250 | | 180 | ns | |
| 4 | TwAS | /AS Low Width | 3.0 | 55 | | 40 | | 55 | | 40 | | ns | [2] |
| | | | 5.5 | 55 | | 40 | | 55 | | 40 | | ns | |
| 5 | Td | Address Float to /DS Fall | 3.0 | 0 | | 0 | | 0 | | 0 | | ns | |
| | | | 5.5 | 0 | | 0 | | 0 | | 0 | | ns | |
| 6 | TwDSR | /DS (Read) Low Width | 3.0 | 200 | | 135 | | 200 | | 135 | | ns | [1,2] |
| | | | 5.5 | 200 | | 135 | | 200 | | 135 | | ns | |
| 7 | TwDSW | /DS (Write) Low Width | 3.0 | 110 | | 80 | | 110 | | 80 | | ns | [1,2] |
| | | | 5.5 | 110 | | 80 | | 110 | | 80 | | ns | |
| 8 | TdDSR(DR) | /DS Fall to Read Data Req'd Valid | 3.0 | | 150 | | 75 | | 150 | | 75 | ns | [1,2] |
| | | | 5.5 | | 150 | | 75 | | 150 | | 75 | ns | |
| 9 | ThDR(DS) | Read Data to /DS Rise Hold Time | 3.0 | 0 | | 0 | | 0 | | 0 | | ns | [2] |
| | | | 5.5 | 0 | | 0 | | 0 | | 0 | | ns | |
| 10 | TdDS(A) | /DS Rise to Address Active Delay | 3.0 | 45 | | 50 | | 45 | | 50 | | ns | [2] |
| | | | 5.5 | 55 | | 50 | | 55 | | 50 | | ns | |
| 11 | TdDS(AS) | /DS Rise to /AS Fall Delay | 3.0 | 30 | | 35 | | 30 | | 35 | | ns | [2] |
| | | | 5.5 | 45 | | 35 | | 45 | | 55 | | ns | |
| 12 | TdR/W(AS) | R/W Valid to /AS Rise Delay | 3.0 | 45 | | 25 | | 45 | | 25 | | ns | [2] |
| | | | 5.5 | 45 | | 25 | | 45 | | 25 | | ns | |
| 13 | TdDS(R/W) | /DS Rise to R/W Not Valid | 3.0 | 45 | | 35 | | 45 | | 35 | | ns | [2] |
| | | | 5.5 | 45 | | 35 | | 45 | | 35 | | ns | |
| 14 | TdDW(DSW) | Write Data Valid to /DS Fall (Write) Delay | 3.0 | 55 | | 25 | | 55 | | 25 | | ns | [2] |
| | | | 5.5 | 55 | | 25 | | 55 | | 25 | | ns | |
| 15 | TdDS(DW) | /DS Rise to Write Data Not Valid Delay | 3.0 | 45 | | 35 | | 45 | | 35 | | ns | [2] |
| | | | 5.5 | 55 | | 35 | | 55 | | 35 | | ns | |
| 16 | TdA(DR) | Address Valid to Read Data Req'd Valid | 3.0 | | 310 | | 230 | | 310 | | 230 | ns | [1,2] |
| | | | 5.5 | | 310 | | 230 | | 310 | | 230 | ns | |
| 17 | TdAS(DS) | /AS Rise to /DS Fall Delay | 3.0 | 65 | | 45 | | 65 | | 45 | | ns | [2] |
| | | | 5.5 | 65 | | 45 | | 65 | | 45 | | ns | |
| 18 | TdDI(DS) | Data Input Setup to /DS Rise | 3.0 | 115 | | 60 | | 115 | | 60 | | ns | [1,2] |
| | | | 5.5 | 75 | | 60 | | 75 | | 60 | | ns | |
| 19 | TdDM(AS) | /DM Valid to /AS Rise Delay | 3.0 | 35 | | 30 | | 35 | | 30 | | ns | [2] |
| | | | 5.5 | 35 | | 30 | | 35 | | 30 | | ns | |

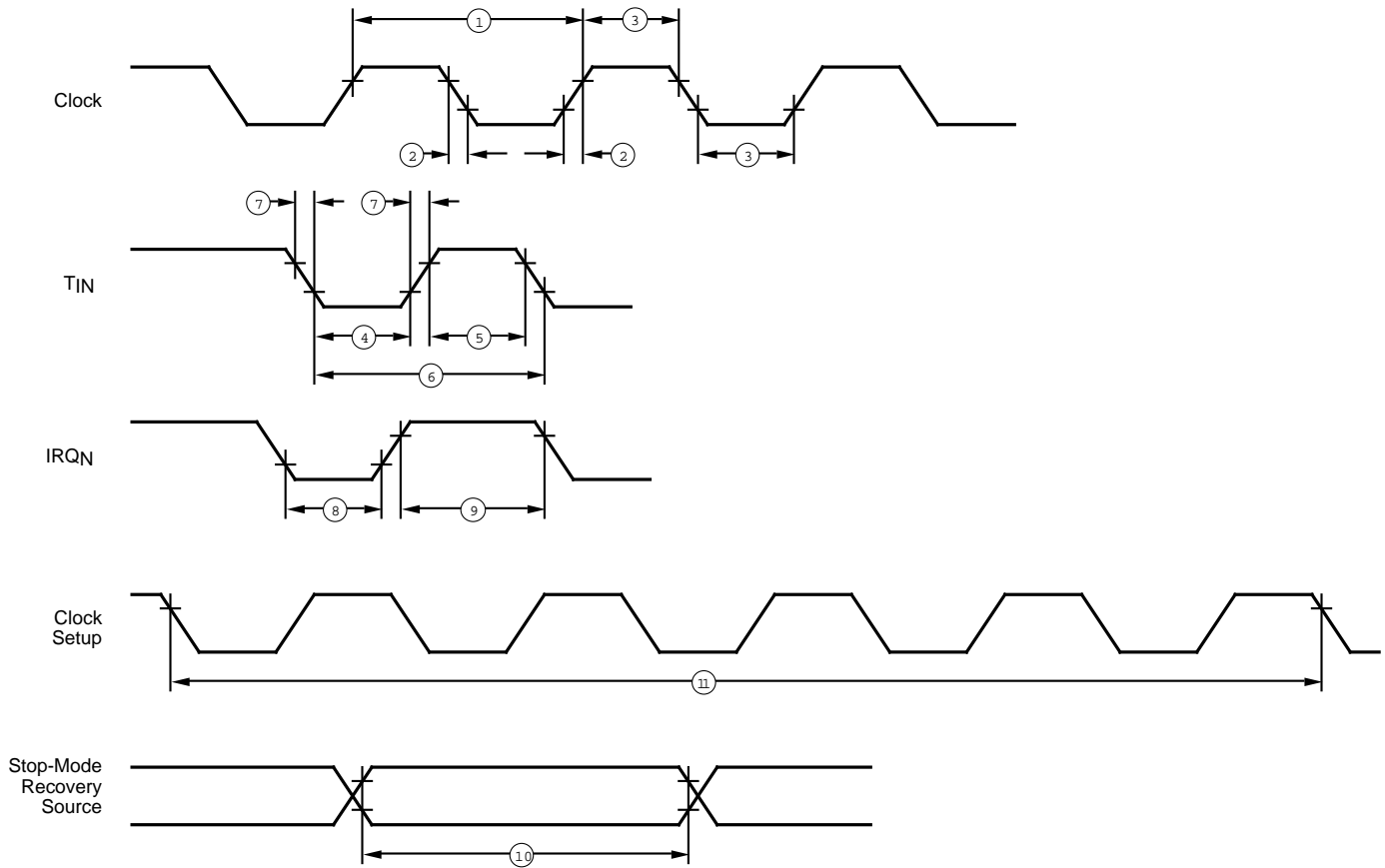
Notes:

- [1] When using extended memory timing add 2 TpC.
 [2] Timing numbers given are for minimum TpC.
 [3] The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.

Standard Test Load

All timing references use 0.7 V_{cc} for a logic 1 and 0.2 V_{cc} for a logic 0.

AC ELECTRICAL CHARACTERISTICS
Additional Timing Diagram



Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (SCLK/TCLK = XTAL/2)

| No | Symbol | Parameter | V _{CC} Note[6] | T _A = 0°C to +70°C | | | | T _A = -40°C to +105°C | | | | Units | Notes |
|----|------------------|---|----------------------------|-------------------------------|------|--------|------|----------------------------------|------|--------|------|-------|------------|
| | | | | 12 MHz | | 16 MHz | | 12 MHz | | 16 MHz | | | |
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| 1 | TpC | Input Clock Period | 3.0V | 83 | DC | 62.5 | DC | 83 | DC | 62.5 | DC | ns | [1] |
| | | | 5.5V | 83 | DC | 62.5 | DC | 83 | DC | 62.5 | DC | ns | [1] |
| 2 | TrC,TfC | Clock Input Rise & Fall Times | 3.0V | | 15 | | 15 | | 15 | | 15 | ns | [1] |
| | | | 5.5V | | 15 | | 15 | | 15 | | 15 | ns | [1] |
| 3 | TwC | Input Clock Width | 3.0V | 41 | | 31 | | 41 | | 31 | | ns | [1] |
| | | | 5.5V | 41 | | 31 | | 41 | | 31 | | ns | [1] |
| 4 | TwTinL | Timer Input Low Width | 3.0V | 100 | | 100 | | 100 | | 100 | | ns | [1] |
| | | | 5.5V | 70 | | 70 | | 70 | | 70 | | ns | [1] |
| 5 | TwTinH | Timer Input High Width | 3.0V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | [1] |
| | | | 5.5V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | [1] |
| 6 | TpTin | Timer Input Period | 3.0V | 8TpC | | 8TpC | | 8TpC | | 8TpC | | | [1] |
| | | | 5.5V | 8TpC | | 8TpC | | 8TpC | | 8TpC | | | [1] |
| 7 | TrTin, TfTin | Timer Input Rise & Fall Timer | 3.0V | | 100 | | 100 | | 100 | | 100 | ns | [1] |
| | | | 5.5V | | 100 | | 100 | | 100 | | 100 | ns | [1] |
| 8A | TwIL | Int. Request Low Time | 3.0V | 100 | | 100 | | 100 | | 100 | | ns | [1,2] |
| | | | 5.5V | 70 | | 70 | | 70 | | 70 | | ns | [1,2] |
| 8B | TwIL | Int. Request Low Time | 3.0V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | [1,3] |
| | | | 5.5V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | [1,3] |
| 9 | TwIH | Int. Request Input High Time | 3.0V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | [1,2] |
| | | | 5.5V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | [1,2] |
| 10 | TwsM | STOP-Mode Recovery Width Spec | 3.0V | 12 | | 12 | | 12 | | 12 | | ns | |
| | | | 5.5V | 12 | | 12 | | 12 | | 12 | | ns | |
| 11 | Tost | Oscillator Startup Time | 3.0V | | 5TpC | | 5TpC | | 5TpC | | 5TpC | | [4] |
| | | | 5.5V | | 5TpC | | 5TpC | | 5TpC | | 5TpC | | [4] |
| 12 | Twdt | Watch-Dog Timer Delay Time Before Time-Out | 3.0V | 10 | | 10 | | 10 | | 10 | | ms | D1 0 0 [5] |
| | | | 5.5V | 5 | | 5 | | 5 | | 5 | | ms | 0 0 [5] |
| | | | 3.0V | 20 | | 20 | | 20 | | 20 | | ms | 0 1 [5] |
| | | | 5.5V | 10 | | 10 | | 10 | | 10 | | ms | 0 1 [5] |
| | | | 3.0V | 40 | | 40 | | 40 | | 40 | | ms | 1 0 [5] |
| | | | 5.5V | 20 | | 20 | | 20 | | 20 | | ms | 1 0 [5] |
| | | | 3.0V | 160 | | 160 | | 160 | | 160 | | ms | 1 1 [5] |
| | | | 5.5V | 80 | | 80 | | 80 | | 80 | | ms | 1 1 [5] |
| 13 | T _{POR} | Power On Reset Delay | 3.0V | 7 | 24 | 7 | 24 | 7 | 25 | 7 | 25 | ms | |
| | | | 5.5V | 3 | 13 | 3 | 13 | 3 | 14 | 3 | 14 | ms | |

Notes:

- [1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
- [2] Interrupt request via Port 3 (P31-P33).
- [3] Interrupt request via Port 3 (P30).
- [4] SMR-D5 = 0.
- [5] Reg. WDTMR, internal RC used.
- [6] The V_{DD} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

AC ELECTRICAL CHARACTERISTICS

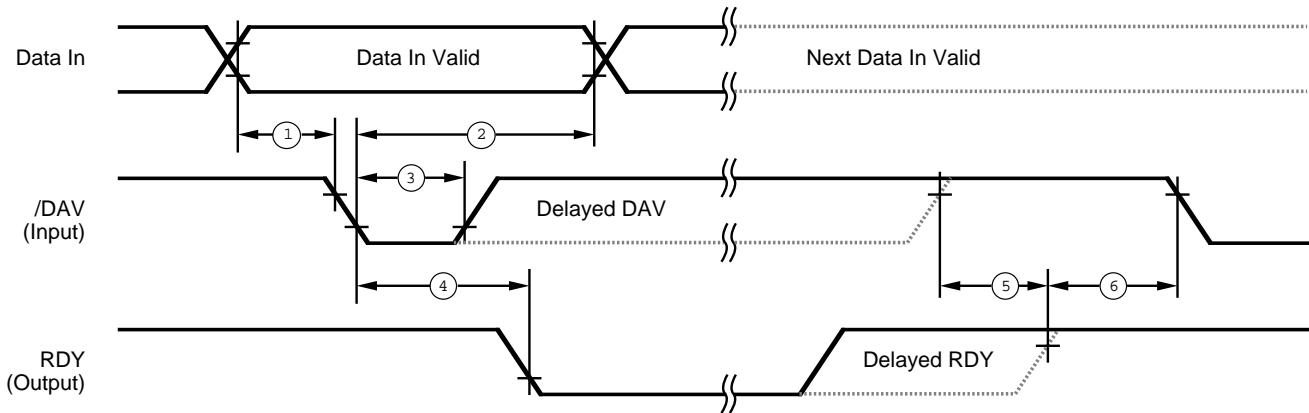
Additional Timing Table (Divide-By-One Mode, SCLK/TCLK = XTAL)

| No | Symbol | Parameter | V _{cc} Note [6] | T _A = 0°C to +70°C | | T _A = -40°C to +105°C | | Units | Notes |
|----|-----------------|-------------------------------|-----------------------------|-------------------------------|------|----------------------------------|------|-------|-----------|
| | | | | 4 MHz | | 4 MHz | | | |
| | | | | Min | Max | Min | Max | | |
| 1 | TpC | Input Clock Period | 3.0V | 250 | DC | 250 | DC | ns | [1,7,8] |
| | | | 5.5V | 250 | DC | 250 | DC | ns | [1,7,8] |
| 2 | TrC,TfC | Clock Input Rise & Fall Times | 3.0V | | 25 | | 25 | ns | [1,7,8] |
| | | | 5.5V | | 25 | | 25 | ns | [1,7,8] |
| 3 | TwC | Input Clock Width | 3.0V | 125 | | 125 | | ns | [1,7,8] |
| | | | 5.5V | 125 | | 125 | | ns | [1,7,8] |
| 4 | TwTinL | Timer Input Low Width | 3.0V | 100 | | 100 | | ns | [1,7,8] |
| | | | 5.5V | 70 | | 70 | | ns | [1,7,8] |
| 5 | TwTinH | Timer Input High Width | 3.0V | 3TpC | | 3TpC | | | [1,7,8] |
| | | | 5.5V | 3TpC | | 3TpC | | | [1,7,8] |
| 6 | TpTin | Timer Input Period | 3.0V | 4TpC | | 4TpC | | | [1,7,8] |
| | | | 5.5V | 4TpC | | 4TpC | | | [1,7,8] |
| 7 | TrTin, TfTin | Timer Input Rise & Fall Timer | 3.0V | | 100 | | 100 | ns | [1,7,8] |
| | | | 5.5V | | 100 | | 100 | ns | [1,7,8] |
| 8A | TwlL | Int. Request Low Time | 3.0V | 100 | | 100 | | ns | [1,2,7,8] |
| | | | 5.5V | 70 | | 70 | | ns | [1,2,7,8] |
| 8B | TwlL | Int. Request Low Time | 3.0V | 3TpC | | 3TpC | | | [1,3,7,8] |
| | | | 5.5V | 3TpC | | 3TpC | | | [1,3,7,8] |
| 9 | TwhH | Int. Request Input High Time | 3.0V | 3TpC | | 3TpC | | | [1,2,7,8] |
| | | | 5.5V | 3TpC | | 2TpC | | | [1,2,7,8] |
| 10 | TwsM | STOP-Mode Recovery Width Spec | 3.0V | 12 | | 12 | | ns | [4,8] |
| | | | 5.5V | 12 | | 12 | | ns | [4,8] |
| 11 | Tost | Oscillator Startup Time | 3.0V | | 5TpC | | 5TpC | | [4,8,9] |
| | | | 5.5V | | 5TpC | | 5TpC | | [4,8,9] |

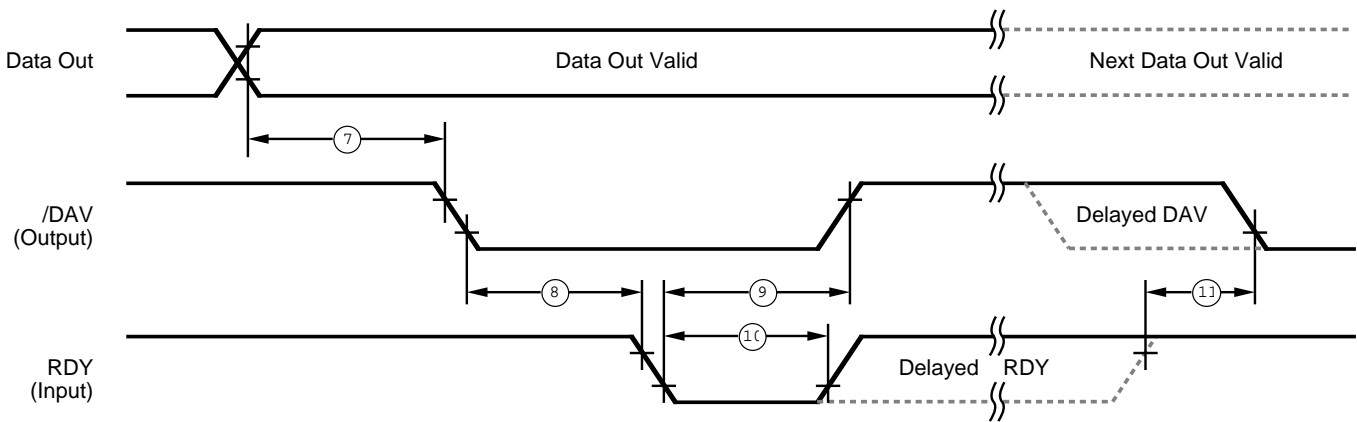
Notes:

- [1] Timing Reference uses 0.7 V_{cc} for a logic 1 and 0.2 V_{cc} for a logic 0.
- [2] Interrupt request via Port 3 (P33-P31).
- [3] Interrupt request via Port 3 (P30).
- [4] SMR-D5 = 1, POR STOP mode delay is on.
- [5] Reg. WDTMR.
- [6] The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.5V ±0.5V.
- [7] SMR D1 = 0.
- [8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
- [9] For RC and LC oscillator, and for oscillator driven by clock driver.

AC ELECTRICAL CHARACTERISTICS
Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table

| No | Symbol | Parameter | V _{CC} Note[1,2] | T _A = 0°C to +70°C | | | | T _A = -40°C to +105°C | | | | Data Direction |
|----|--------------|----------------------------|------------------------------|-------------------------------|-----|--------|-----|----------------------------------|-----|--------|-----|-------------------|
| | | | | 12 MHz | | 16 MHz | | 12 MHz | | 16 MHz | | |
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| 1 | TsDI(DAV) | Data In Setup Time | 3.0V | 0 | | 0 | | 0 | | 0 | | IN |
| | | | 5.5V | 0 | | 0 | | 0 | | 0 | | IN |
| 2 | ThDI(DAV) | Data In Hold Time | 3.0V | 160 | | 160 | | 160 | | 160 | | IN |
| | | | 5.5V | 115 | | 115 | | 115 | | 115 | | IN |
| 3 | TwDAV | Data Available Width | 3.0V | 155 | | 155 | | 155 | | 155 | | IN |
| | | | 5.5V | 110 | | 110 | | 110 | | 110 | | IN |
| 4 | TdDAVI(RDY) | DAV Fall to RDY Fall Delay | 3.0V | | 160 | | 160 | | 160 | | 160 | IN |
| | | | 5.5V | | 115 | | 115 | | 115 | | 115 | IN |
| 5 | TdDAVI(dRDY) | DAV Rise to RDY Rise Delay | 3.0V | | 120 | | 120 | | 120 | | 120 | IN |
| | | | 5.5V | | 80 | | 80 | | 80 | | 80 | IN |
| 6 | TdRDY0(DAV) | RDY Rise to DAV Fall Delay | 3.0V | 0 | | 0 | | 0 | | 0 | | IN |
| | | | 5.5V | 0 | | 0 | | 0 | | 0 | | IN |
| 7 | TdD0(DAV) | Data Out to DAV Fall Delay | 3.0V | 42 | | 31 | | 42 | | 31 | | OUT |
| | | | 5.5V | 42 | | 31 | | 42 | | 31 | | OUT |
| 8 | TdDAV0(RDY) | DAV Fall to RDY Fall Delay | 3.0V | 0 | | 0 | | 0 | | 0 | | OUT |
| | | | 5.5V | 0 | | 0 | | 0 | | 0 | | OUT |
| 9 | TdRDY0(DAV) | RDY Fall to DAV Rise Delay | 3.0V | | 160 | | 160 | | 160 | | 160 | OUT |
| | | | 5.5V | | 115 | | 115 | | 115 | | 115 | OUT |
| 10 | TwRDY | RDY Width | 3.0V | 110 | | 110 | | 110 | | 110 | | OUT |
| | | | 5.5V | 80 | | 80 | | 80 | | 80 | | OUT |
| 11 | TdRDY0d(DAV) | RDY Rise to DAV Fall Delay | 3.0V | | 110 | | 110 | | 110 | | 110 | OUT |
| | | | 5.5V | | 80 | | 80 | | 80 | | 80 | OUT |

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

[2] The V_{DD} voltage specification of 3.0V guarantees 3.3V ± 0.3V and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

PRECAUTIONS

- (1) When in ROM Protect Mode, and executing out of *External Program Memory*, instructions LDC, LDCI, LDE, and LDEI *cannot* read Internal Program Memory.

When in ROM Protect Mode, and executing out of *Internal Program Memory*, instructions LDC, LDCI, LDE, and LDEI *can* read Internal Program Memory.
- (2) The device has an oscillator-free reset for the device pins. When the device is reset from a WDT timeout, POR, or V_{BO} , the reset will force the device pins to their reset default state even if the oscillator is not running.
- (3) The Port 3 outputs are reset to High State after Reset, except after Stop-Mode Recovery, at which the outputs remain in the last state.
- (4) Extended timing is operable.
- (5) P0/P1/P2/P3 is Low-EMI software programmable.
- (6) P0/P1/P2 is software programmable for open-drain.
- (7) Expanded register PCON is Write Only.
- (8) WDTMR is writeable only within the first 60 internal system clocks after Reset. Afterward, the WDTMR is write protected.
- (9) Device functions down to the V_{LV} threshold. At temperatures less than 25°C, the V_{LV} threshold will rise to a maximum V_{DD} of 3.6V.
- (10) Low EMI is 25 percent of standard pull-down output driver and 25 percent of standard pull-up output driver.
- (11) There is no clock filter on Reset pin.
- (12) Registers FE Hex (SPH) and FF Hex (SPL) are set to 00Hex after any reset.
- (13) When Low EMI OSC is selected (PCONReg Bit D7=0), the output drive of /DS, /AS, and R//W will also be in low emi mode.
- (14) P01M Reg Bit D4,D3 must be set to 00Hex for Z86233.

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Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: <http://www.zilog.com>