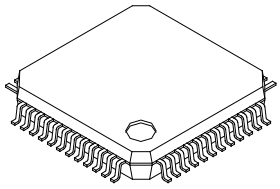
SONY

CXB1567Q

Limiting Amplifier for Optical Fiber Communication Receiver

48 pin QFP (Plastic)



Description

The CXB1567Q achieves the 2R optical-fiber communication receiver functions (Reshaping and Regenerating) on a single chip. This IC is also equipped with the signal interruption alarm output function, which is used to discriminate the existence of data input.

Features

- Auto-offset canceller circuit
- Signal interruption alarm outputs
- Single 5V power supply

Applications

- SONET/SDH: 622.08Mb/s
- Fiber channel: 531.25Mb/s

Absolute Maximum Ratings

• Power supply	$V_{CC} - V_{EE}$	–0.3 to +7.0	V
• Storage temperature	Tstg	–65 to +150	°C
• Input voltage difference: $\lvert V_D - V_{\overline{D}} \rvert$	Vdif	0.0 to +2.5	V
• Input voltage	Vi	–0.3 to V_{CC}	V
• Output current			
(Continuous)	I_O	0 to 50	mA
(Surge current)		0 to 100	mA

Recommended Operating Conditions

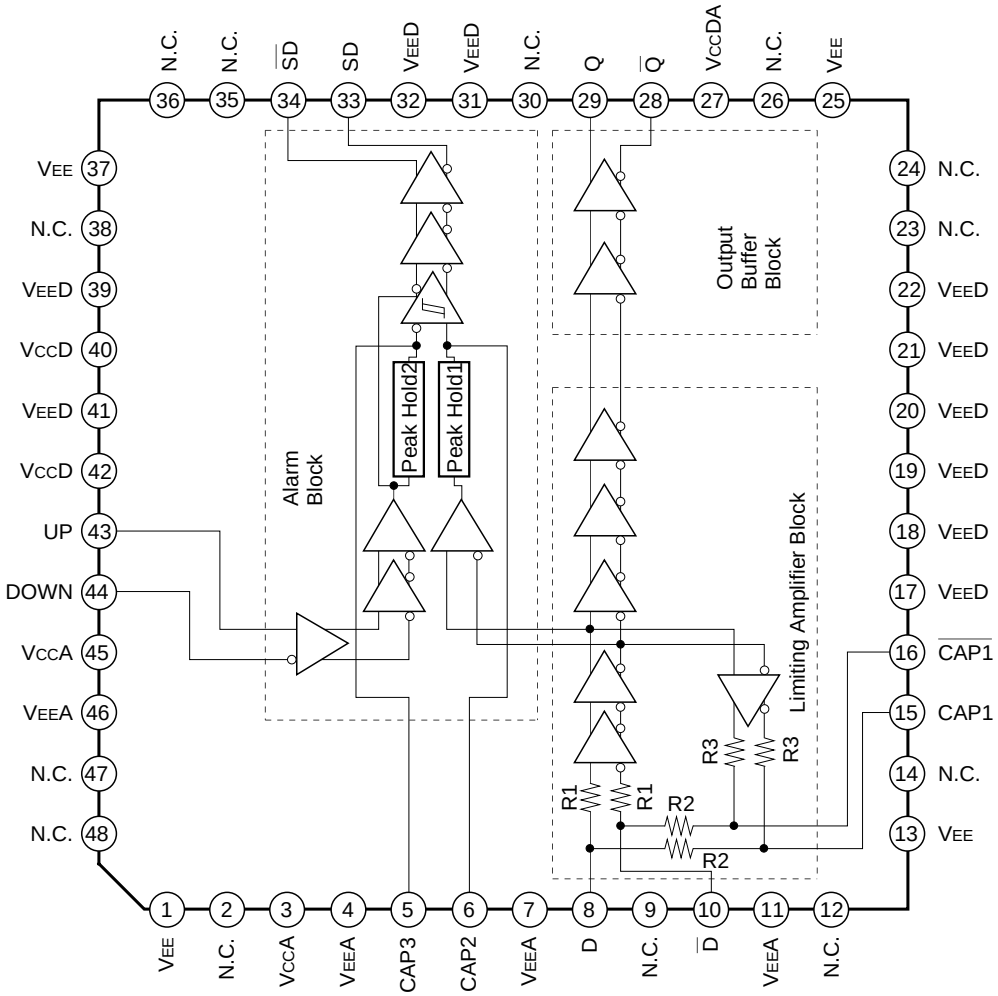
• Supply voltage	$V_{CC} - V_{EE}$	5.0 ± 0.5	V
• Operating temperature	Ta	–40 to +85	°C
• Termination resistor ($Q/\overline{Q}$)			
	R_{T1}	45 to 55	Ω
• Termination resistor ($SD/\overline{SD}$)			
	R_{T2}	45 to 55	Ω
• Termination voltage	$V_{CC} - V_{TT}$	1.8 to 2.2	V

Structure

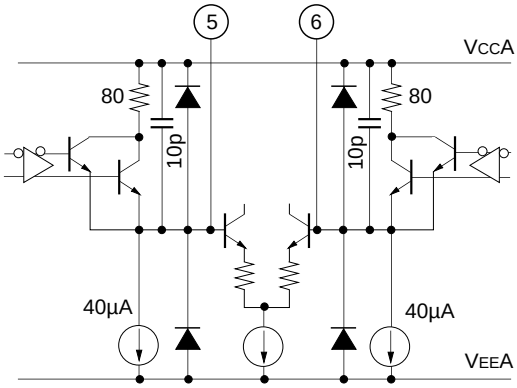
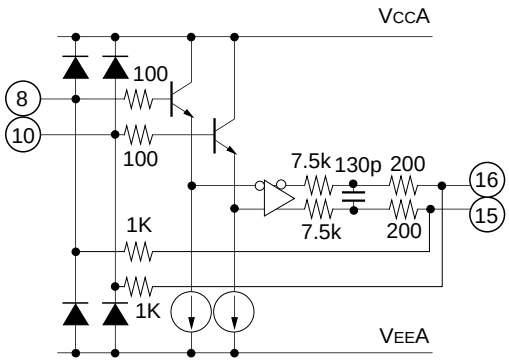
Bipolar silicon monolithic IC

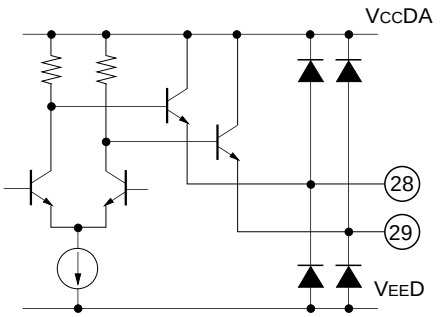
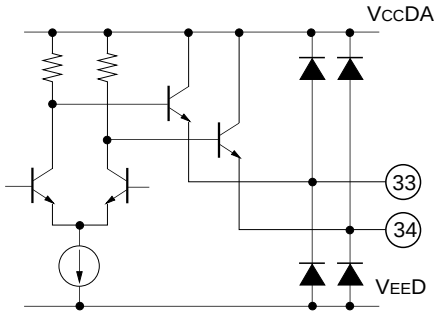
E94709A63-ST

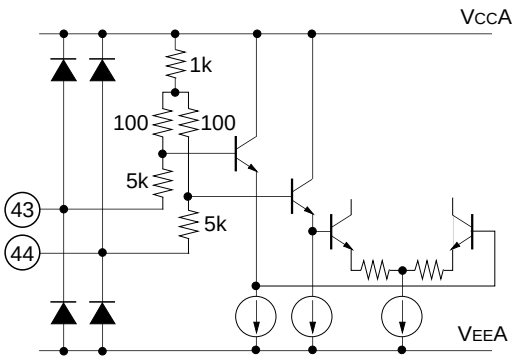
Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Typical pin voltage (V) DC	Typical pin voltage (V) AC	Equivalent circuit	Description
1	V_{EE}	–5V			Negative power supply pin.
2	N.C.				No connection.
3	$V_{CC}A$	0V			Positive power supply pin for analog block.
4	$V_{EE}A$	–5V			Negative power supply pin for analog block.
5	CAP3	–1.8V			Capacitance connection pins for alarm block peak hold circuit. Connect each pin to V_{CC} in 2000pF. CAP2 pin → Peak hold capacitance connection pin for the limiting amplifier signal CAP3 pin → Peak hold capacitance connection pin for the alarm level setting block
6	CAP2	–1.8V			
7	$V_{EE}A$	–5V			Negative power supply pin for analog block.
8	D	–1.3V	–0.9V to –1.7V		Limiting amplifier input pins Ensure that these inputs are AC-coupled.
9	N.C.				
10	$\overline{D}$	–1.3V			
11	$V_{EE}A$	–5V			Negative power supply pin for analog block.
12	N.C.				No connection.
13	V_{EE}	–5V			Negative power supply pin.
14	N.C.				No connection.
15	CAP1	–1.8V			Capacitance connection pins to determine the cut-off frequency for feedback block.
16	$\overline{CAP1}$	–1.8V			
17 to 22	$V_{EE}D$	–5V			Negative power supply pin for digital block.
23, 24	N.C.				No connection.
25	V_{EE}	–5V			Negative power supply pin.

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
26	N.C.				No connection.
27	$V_{CC}DA$	0V			Positive power supply pin for output buffer.
28	$\overline{Q}$		–0.9V to –1.7V		Data signal output pins. Terminate these pins in 50Ω at VTT = –2V.
29	Q		–0.9V to –1.7V		
30	N.C.				No connection.
31, 32	$V_{EE}D$	–5V			Negative power supply pin for digital block.
33	SD		–0.9V to –1.7V		Alarm signal output pins. Terminate these pins in 50Ω at VTT = –2V.
34	$\overline{SD}$		–0.9V to –1.7V		
35, 36	N.C.				No connection.
37	V_{EE}	–5V			Negative power supply pin.
38	N.C.				No connection.
39	$V_{EE}D$	–5V			Negative power supply pin for digital block.
40	$V_{CC}D$	0V			Positive power supply pin for digital block.
41	$V_{EE}D$	–5V			Negative power supply pin for digital block.
42	$V_{CC}D$	0V			Positive power supply pin for digital block.

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
43	UP	–4.7V			Resistor connection pins for alarm level setting. UP pin → When the resistance connected to this pin is increased, the alarm level becomes higher. DOWN pin → Normally connect this pin to VEE.
44	DOWN	–5V			
45	VCCA	0V			Positive power supply pin for analog block.
46	VEEA	–5V			Negative power supply pin for analog block.
47, 48	N.C.				No connection.

Electrical Characteristics

• **DC characteristics** (VCC = VCCA = 0V, VEED= VEEA= VEE = –5V±10%, Ta = –40°C to +85°C, RT = 50Ω, VTT = –2V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current	I_{EE}		–93	–59		mA
Q/$\overline{Q}$ High output voltage	V_{OH}	Ta = 0 to 85°C	–1.03	–0.95	–0.88	V
Q/$\overline{Q}$ Low output voltage	V_{OL}		–1.81	–1.70	–1.62	
SD/$\overline{SD}$ High output voltage	V_{OHS}		–1.25	–0.95	–0.70	
SD/$\overline{SD}$ Low output voltage	V_{OLS}		–1.95	–1.76	–1.57	
Input offset voltage	V_{OFF}			70		µV
D/$\overline{D}$ input resistance	Rin		0.75	1.0	1.25	kΩ

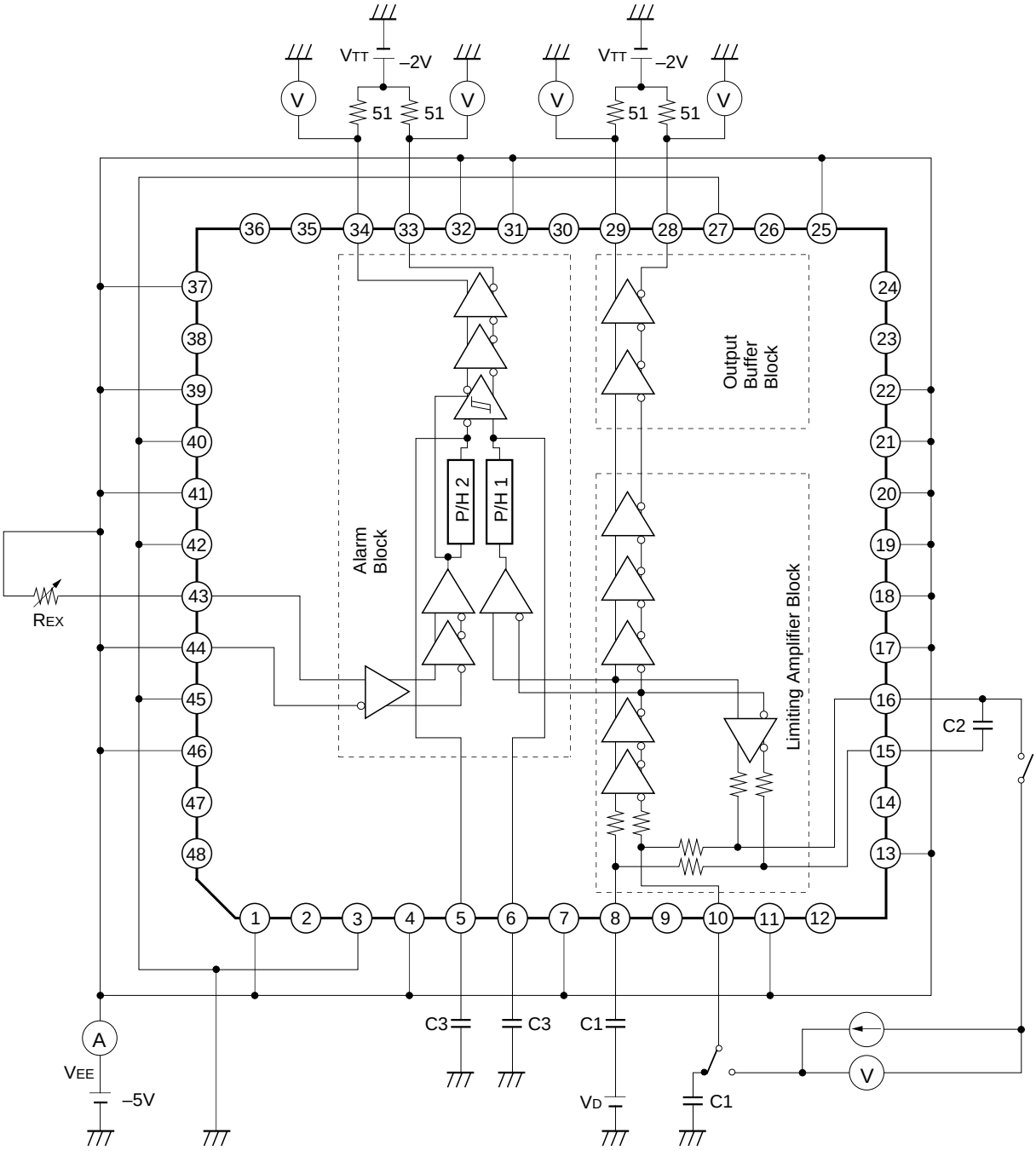
• **AC characteristics** (VCC = VCCA = 0V, VEED= VEEA= VEE = –5V±10%, Ta = –40°C to +85°C, RT = 50Ω, VTT = –2V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximum input data rate	B		622.08			Mbps
Maximum input voltage	V_{MAX}	Single-ended input voltage at D	1000			mVpp
Limiting amplifier gain	GL	IC internal amplitude 400mVpp	66			dB
Q/$\overline{Q}$ rise time	T_{TLH}	20% to 80%		240	450	ps
Q/$\overline{Q}$ fall time	T_{THL}			240	450	
Identification maximum voltage amplitude of alarm level	V_{MIN}		20			mVpp
Hysteresis width	Hys	Electrically tested	4	6	8	dB
Alarm response assert time	T_{AS}	Low → High *1 (SD)	0		100	µs
Alarm response deassert time	T_{DAS}	High → Low *2 (SD)	2.5		100	

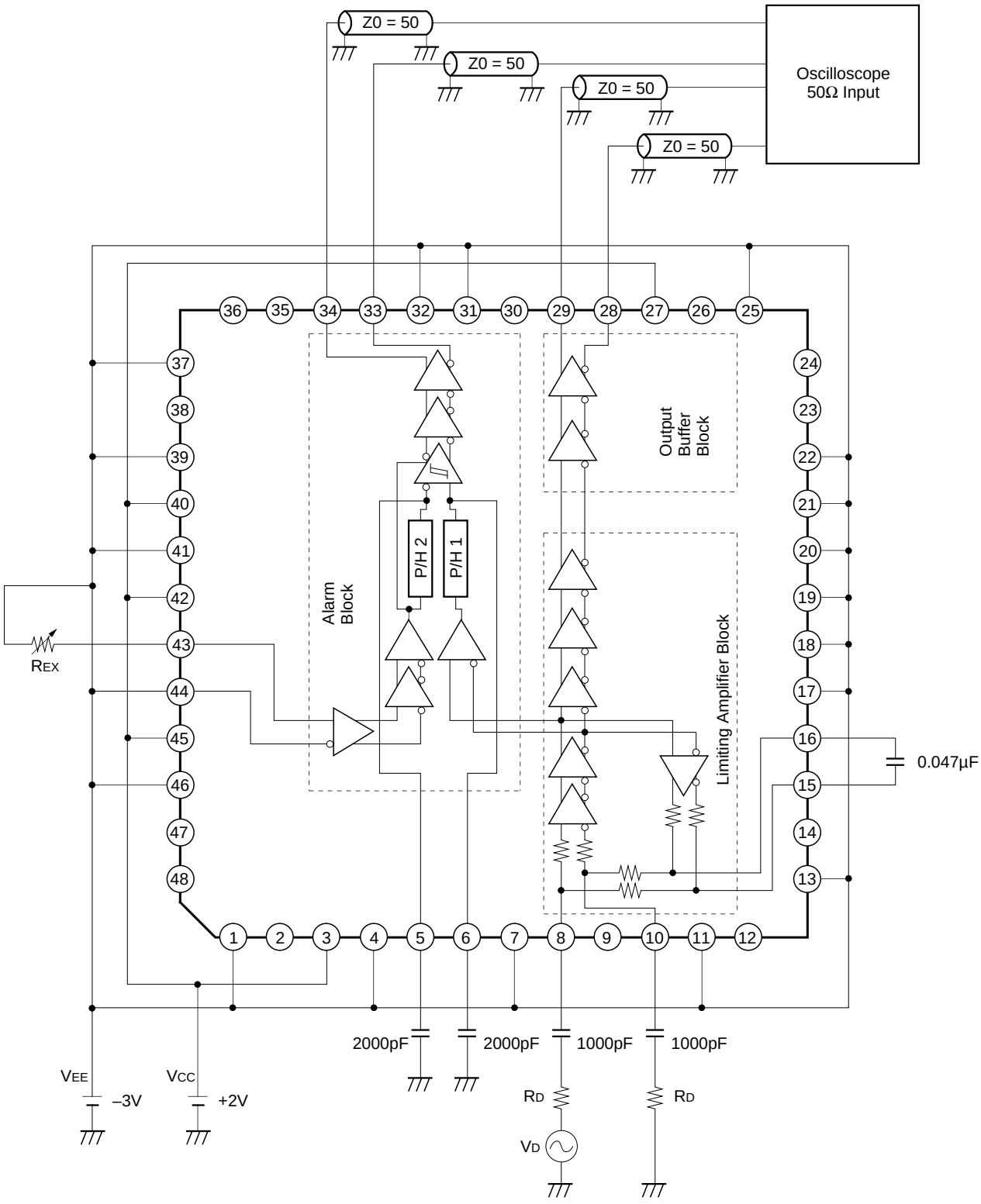
*1 CAP2, CAP3 pin capacitance = 2000pF, REX = 400Ω, Vin = 20mVpp (single ended)

*2 CAP2, CAP3 pin capacitance = 2000pF, REX = 400Ω, Vin = 60mVpp (single ended)

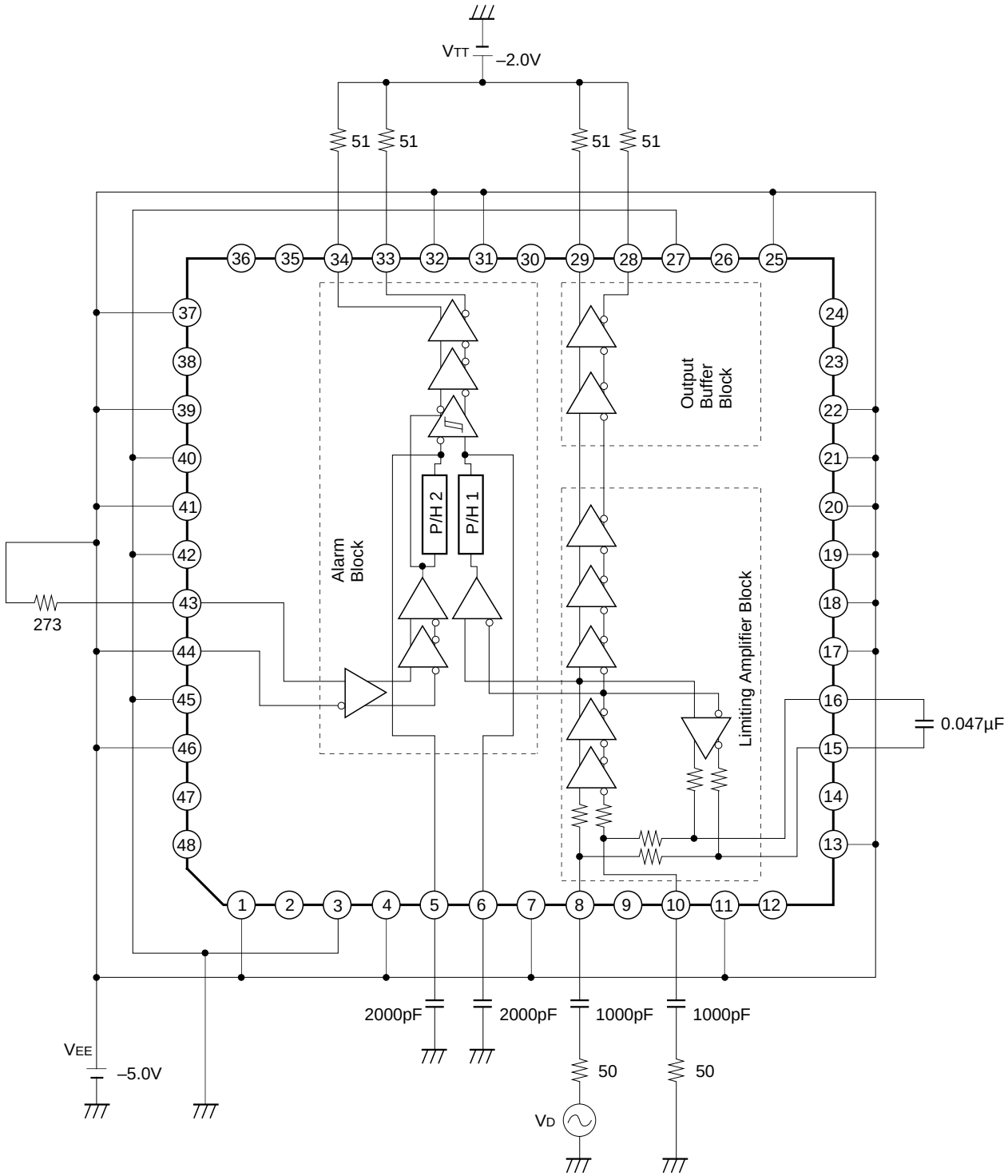
DC Electrical Characteristics Measurement Circuit



AC Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

1. Limiting amplifier block

The limiting amplifier block is equipped with the auto-offset canceller circuit. When external capacitors C1 and C2 are connected as shown in Fig. 1, the DC bias is set automatically in this block. External capacitor C1 and IC internal resistor R1 determine the low input cut-off frequency f2, as shown in Fig. 2. Similarly, external capacitor C2 and internal resistor R2 determine the high cut-off frequency f1 for DC bias feedback. Since peaking characteristics may occur in the low frequency area of the amplifier gain characteristics depending on the f1/f2 combination, set the C1 and C2 values so as to avoid the occurrence of peaking characteristics. The typical values of R1,R2, C1 and C2 are as indicated below. When a single-ended input is used, provide AC grounding by connecting Pin 10 to a capacitor which has the same capacitance as capacitor C1. R_D is the resistor for impedance matching. The same level of output impedance as for the signal source should be applied to Pin 10.

R1 (internal) : 1kΩ
C1 (external) : 1000pF
→ f2: 160kHz

R2 (internal) : 7.5kΩ
C2 (external) : 0.047µF
→ f1: 450Hz

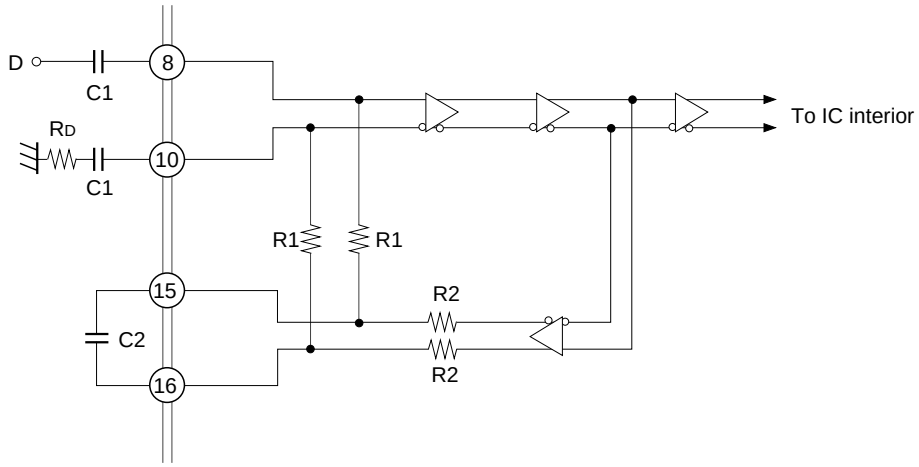


Fig. 1

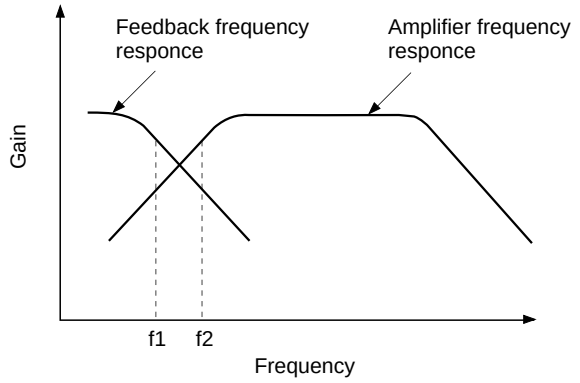


Fig. 2

2. Alarm block

As shown in Fig. 3, the alarm block requires external resistor R_{EX1} for alarm level setting and peak hold capacitor C3. When the resistance value provided for resistor R_{EX1} is increased, the alarm setting level rises. When the resistance value provided for R_{EX2} is increased, the alarm setting level lowers. However, the voltage of Pin 43 should always be higher than that of Pin 44. Normally, short-circuit Pin 44 to V_{EE} (R_{EX2} = 0). See Fig. 5 for the alarm setting level. In the relationship between the alarm setting level and hysteresis width, the hysteresis width is designed to maintain a constant gain (design target value: 6dB) as shown in Fig. 4. External capacitors C3 are used for input signal and alarm level peak hold capacitance. The C3 capacitance value should be set so as to obtain desired assert time and deassert time settings for the alarm signal. The deassert time becomes smaller by connecting resistor R10 between V_{EE} and Pin 5 and resistor R11 between V_{EE} and Pin 6. The R_{EX1} and C3 typical values are indicated below. (A capacitance of approximately 10pF is built in Pins 5 and 6 respectively.)

R_{EX1}: 273Ω (V_{DAS} = 3mVpp)
C3: 2000pF

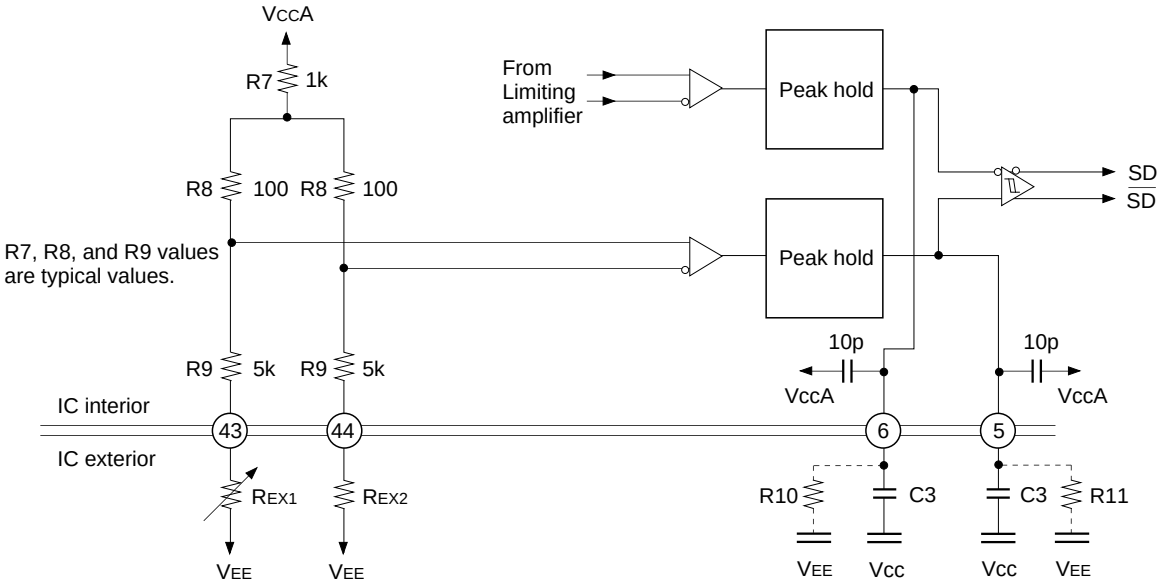


Fig. 3

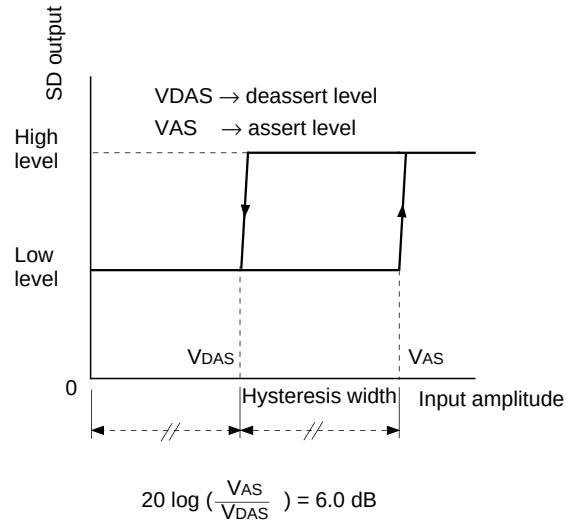


Fig. 4

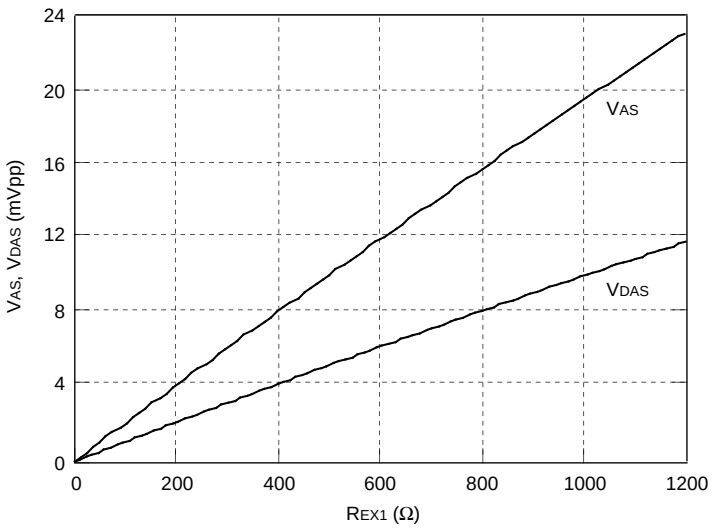
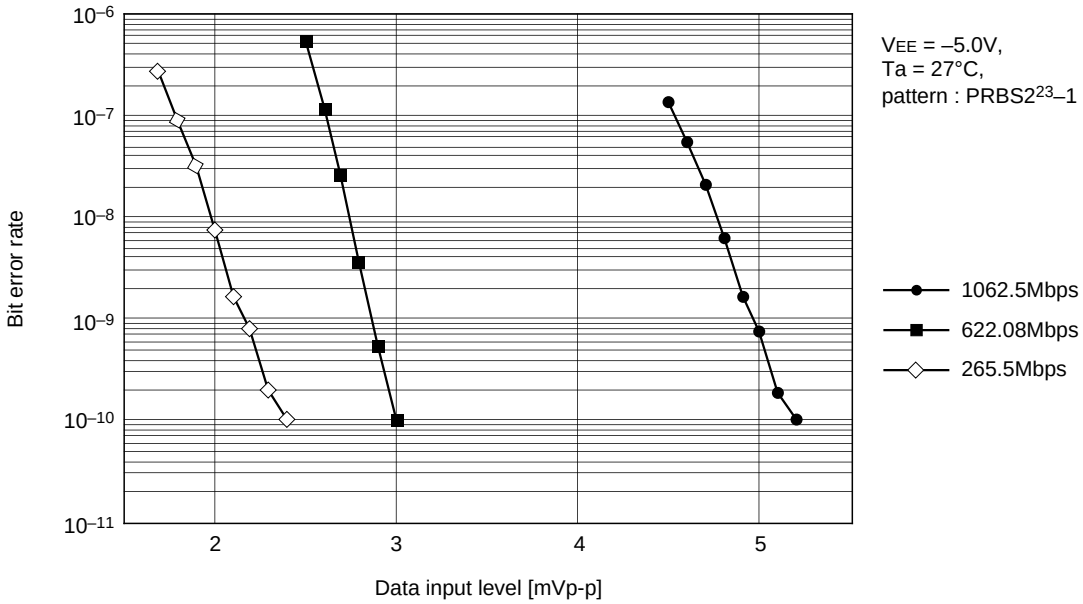


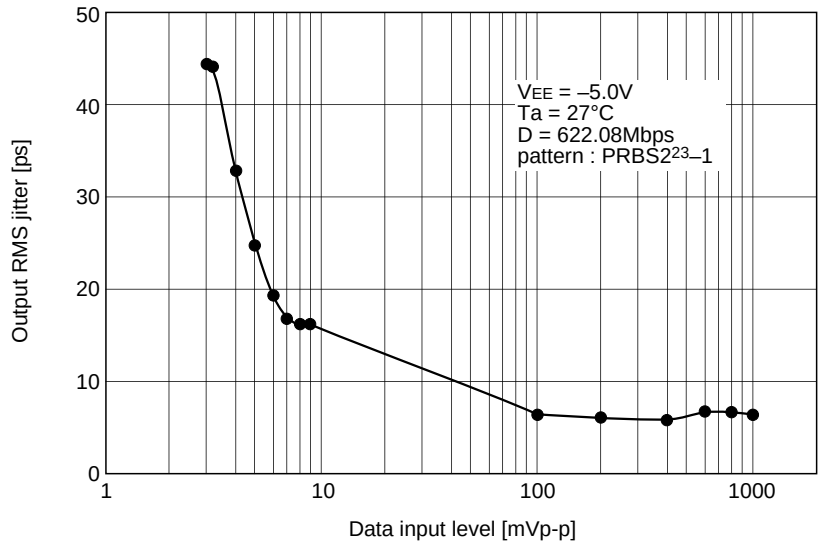
Fig. 5

Example of Representative Characteristics

Bit error rate vs. Data input level for each data rate

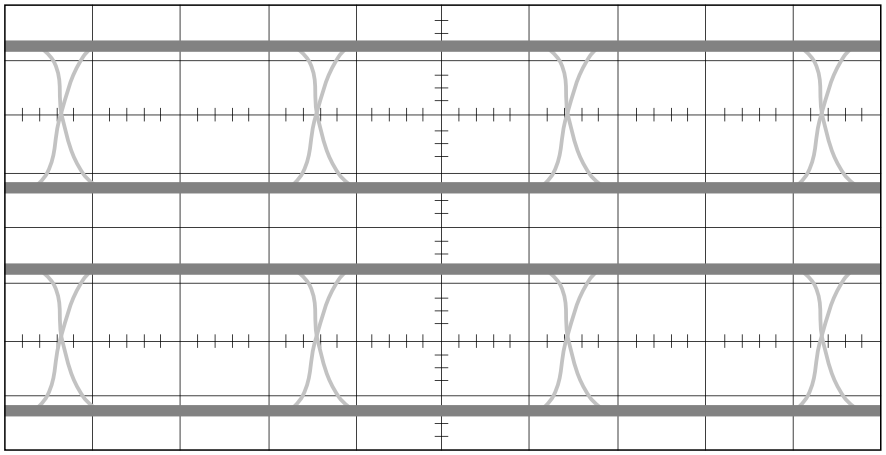


Output RMS jitter vs. Data input level



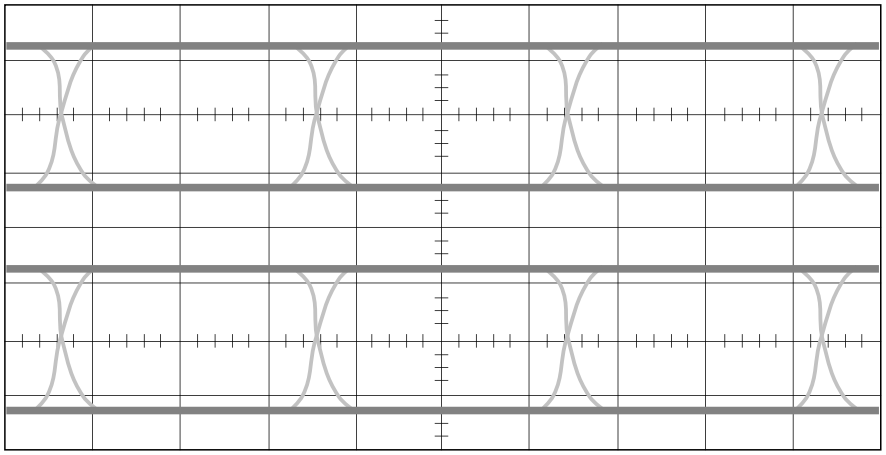
V_{EE} = –5.0V
Ta = 27°C
D = 265.5Mbps
pattern = PRBS2^{23}–1

Y Axis = 300mV/div
X Axis = 1300ps/div



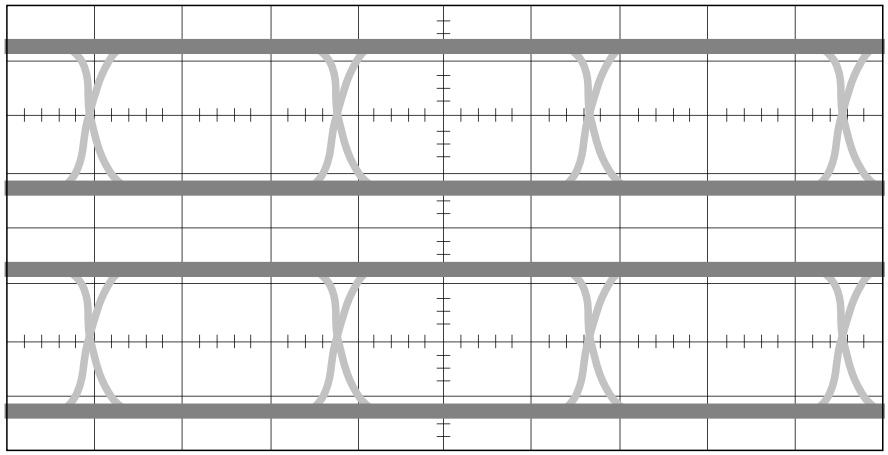
V_{DIN} = 2.0Vp-p

26.1040ns 32.6040ns 39.1040ns



V_{DIN} = 500mVpp

26.1040ns 32.6040ns 39.1040ns

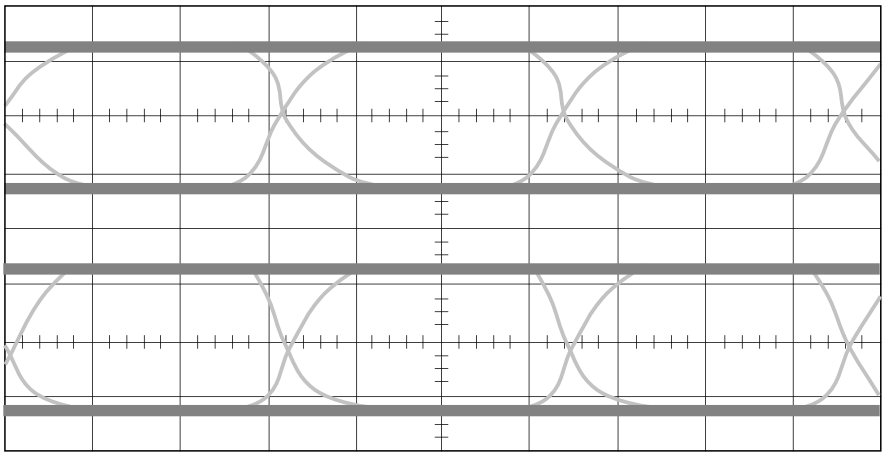


V_{DIN} = 2.5mVpp

26.1040ns 32.6040ns 39.1040ns

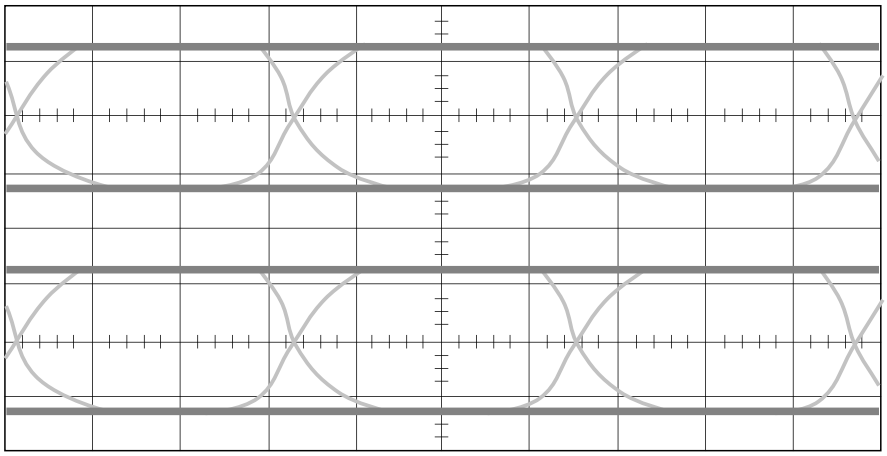
V_{EE} = –5.0V
Ta = 27°C
D = 622.08Mbps
pattern = PRBS2^{23}–1

Y Axis = 300mV/div
X Axis = 500ps/div



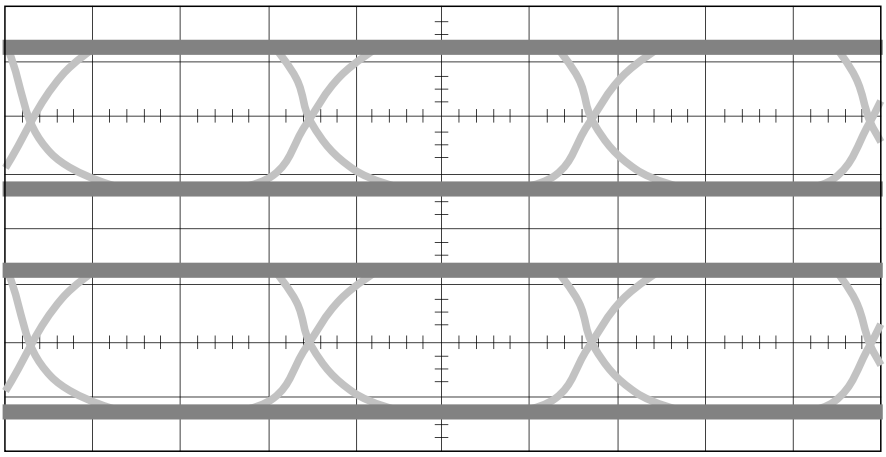
V_{DIN} = 2.0Vp-p

23.7300ns 26.2300ns 28.7300ns



V_{DIN} = 500mVpp

23.6600ns 26.1600ns 28.6600ns

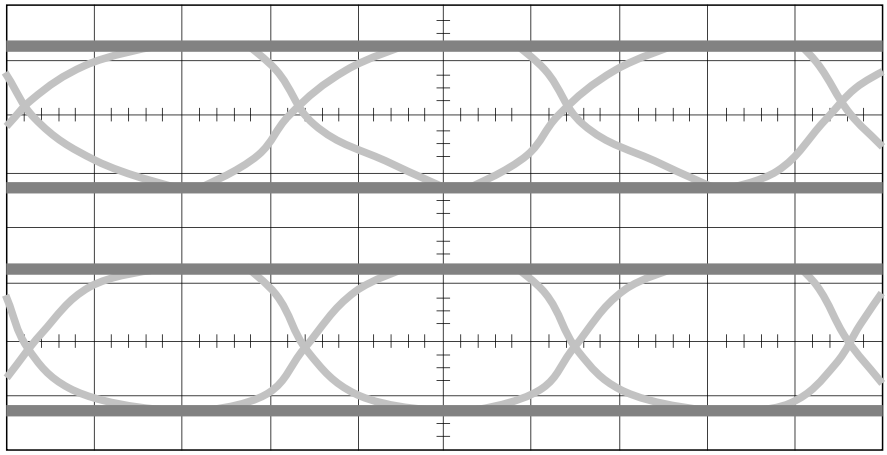


V_{DIN} = 3.0mVpp

23.7500ns 26.2500ns 28.7500ns

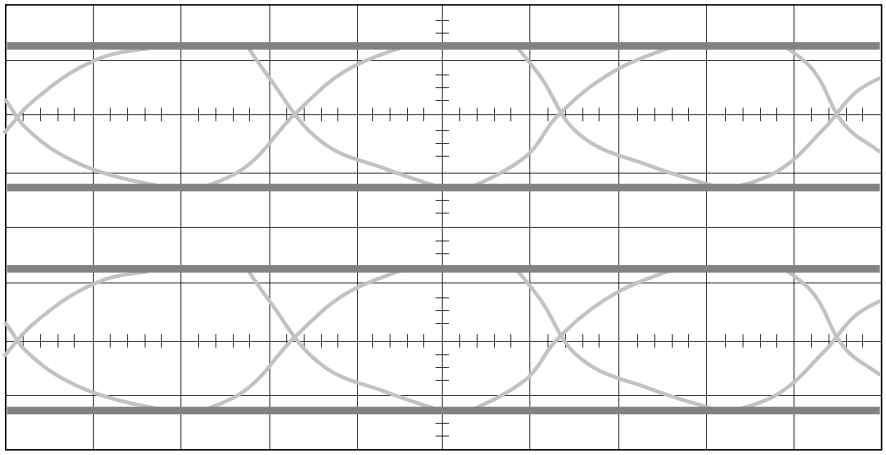
V_{EE} = –5.0V
Ta = 27°C
D = 1062.5Mbps
pattern = PRBS2^{23}–1

Y Axis = 300mV/div
X Axis = 300ps/div



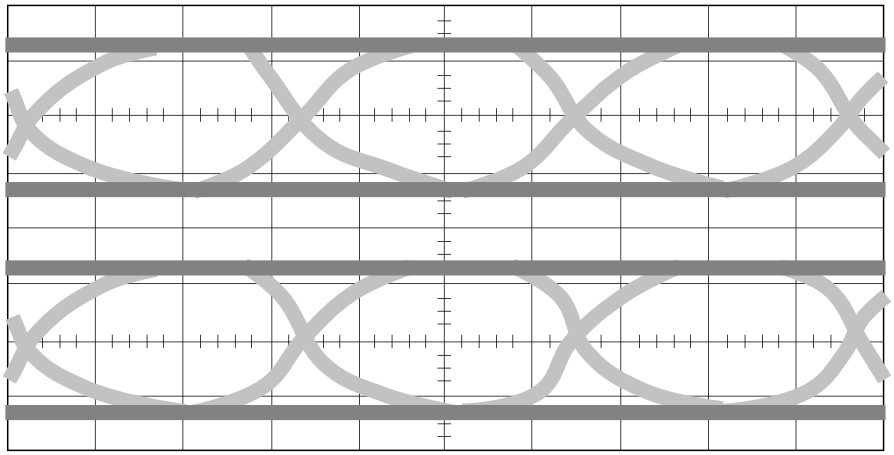
V_{DIN} = 2.0Vp-p

26.4900ns 27.9900ns 29.4900ns



V_{DIN} = 500mVpp

26.4900ns 27.9900ns 29.4900ns

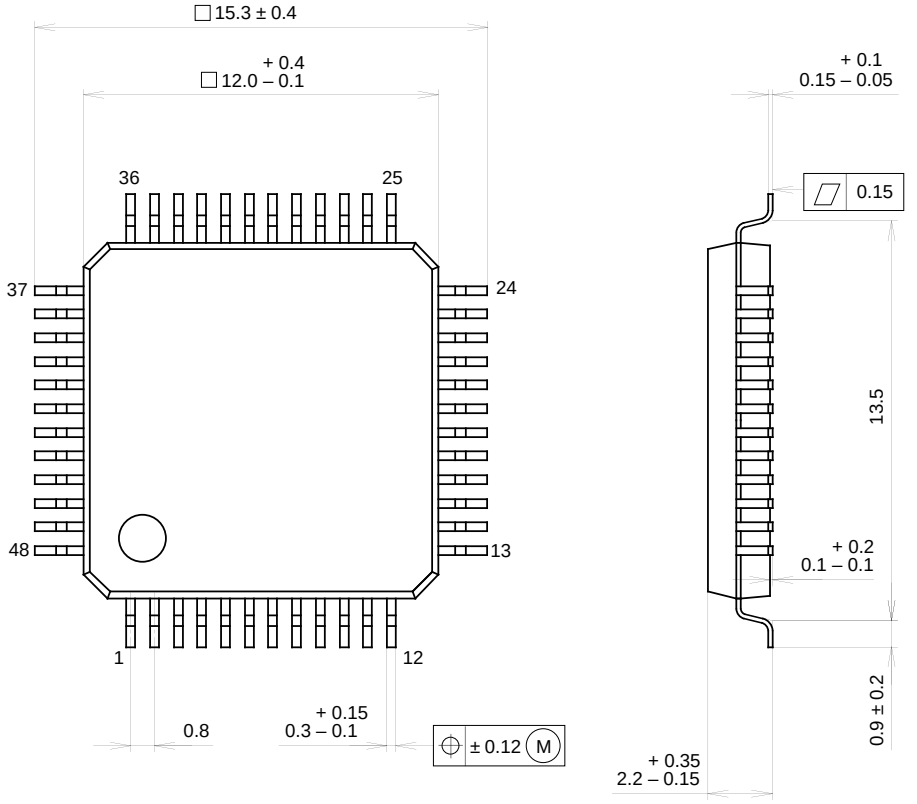


V_{DIN} = 10mVpp

16.3740ns 17.8740ns 19.3740ns

Package Outline Unit: mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	∗QFP048-P-1212-B
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g