

# DATA SHEET

## **GTL2004**

Quad GTL/GTL+ to LVTTTL/TTL  
bidirectional latched translator

Product specification  
Supersedes data of 1999 May 15

1999 Jul 19

# Quad GTL/GTL+ to LVTTTL/TTL bidirectional latched translator

## GTL2004

### FEATURES

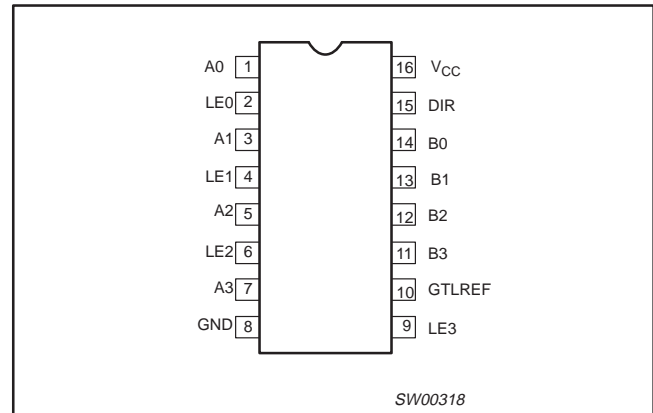
- Operates as a quad GTL/GTL+ sampling receiver or as a LVTTTL/TTL to GTL/GTL+ driver
- Quad bidirectional bus interface
- Separate latch enable for each bit
- Live insertion/extraction permitted
- B outputs include 30Ω series resistance
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per JEDEC Std

### DESCRIPTION

The GTL2004 is a quad translating transceiver designed for 3.3V system interface with a GTL/GTL+ bus.

The direction pin allows the part to function as either a GTL to TTL sampling receiver or as a TTL to GTL interface. Separate latch enables allow sampling and holding of data from the GTL bus.

### PIN CONFIGURATION



### PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	DIR	Direction control input
1, 3, 5, 7	A0 – A3	Data inputs/outputs (A side, GTL)
11, 12, 13, 14	B0 – B3	Data inputs/outputs (B side, TTL)
2, 4, 6, 9	LE0 – LE3	Latch enables
10	GTLREF	GTL reference voltage
8	GND	Ground (0V)
16	V <sub>CC</sub>	Positive supply voltage

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$	TYPICAL		UNIT
			B to A	A to B	
$t_{PLH}$ $t_{PHL}$	Propagation delay An to Bn or Bn to An	$C_L = 50\text{pF}$ ; $V_{CC} = 3.3\text{V}$	2.0 1.8	4.4 4.7	ns
$C_{IN}$	Input capacitance DIR, LEn	$V_I = 0\text{V}$ or $V_{CC}$	3.0	3.0	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O} = 0\text{V}$ or 3.152V	7.2	4.6	pF

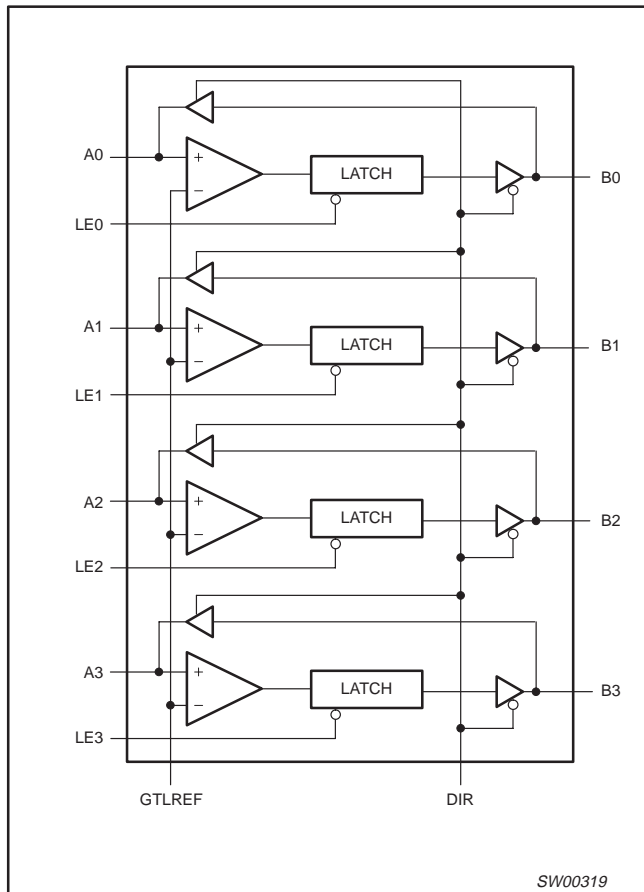
### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
16-Pin Plastic TSSOP Type II	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	GTL2004 PW DH	SOT403-1

# Quad GTL/GTL+ to LVTTTL/TTL bidirectional latched translator

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## LOGIC SYMBOL



## FUNCTION TABLE

INPUT		INPUT/OUTPUT	
DIR	LEn	A	B
L	H	Inputs	An = Bn
L	L	X	NC
H	X	Bn = An	Inputs

H = HIGH voltage level

L = LOW voltage level

X = Don't care

NC = No change

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## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

In accordance with the Absolute Maximum System (IEC 134); voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>	A port	-0.5 to +7.0	V
		B port	-0.5 to +4.6	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	-50	mA
V <sub>O</sub>	DC output voltage <sup>3</sup>	Output in OFF or HIGH state; A port	-0.5 to +7.0	V
		Output in OFF or HIGH state; B port	-0.5 to +4.6	V
I <sub>OL</sub>	Current into any output in the LOW state	A port	128	mA
		B port	80	mA
I <sub>OH</sub>	Current into any output in the HIGH state	A port	-64	mA
T <sub>stg</sub>	Storage temperature range		-60 to +150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS<sup>1</sup>

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage		0		3.6	V
V <sub>TT</sub>	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V <sub>REF</sub>	Supply voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1.0	1.10	
V <sub>I</sub>	Input voltage	A port	0		V <sub>TT</sub>	V
		Except A port	0		5.5	
V <sub>IH</sub>	HIGH-level input voltage	A port	V <sub>REF</sub> + 50mV			V
		Except A port	2			
V <sub>IL</sub>	LOW-level input voltage	A port			V <sub>REF</sub> - 50mV	V
		Except A port			0.8	
I <sub>OH</sub>	HIGH-level output current	B port			-12	mA
I <sub>OL</sub>	LOW-level output current	A port			40	mA
		B port			12	mA
T <sub>amb</sub>	Operating free-air temperature range		-40		85	°C

### NOTE:

- Unused control inputs must be held HIGH or LOW to prevent them from floating.

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## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			-40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>OH</sub>	B port	V <sub>CC</sub> = 3.0 to 3.6V; I <sub>OH</sub> = -100µA	V <sub>CC</sub> -0.2			V
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -12mA	2.0			
V <sub>OL</sub>	A port	V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 40mA			0.4	V
	B port	V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 12mA			0.8	V
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND			± 1	µA
	A port	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>TT</sub> or GND			± 1	
	B port	V <sub>CC</sub> = 0 or 3.6V; V <sub>I</sub> = 5.5			10	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub>			± 1	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 0V			-5	
I <sub>OFF</sub>	A port	V <sub>CC</sub> = 0V; V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5V			± 100	µA
I <sub>EX</sub>	B port	V <sub>O</sub> = 5.5V; V <sub>CC</sub> = 3.0V		50	125	µA
I <sub>CC</sub>	A or B port	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0			3	mA
ΔI <sub>CC</sub> <sup>3</sup>	B port or control inputs	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V			500	µA
C <sub>I</sub>	Control inputs	V <sub>I</sub> = 3.0V or 0		3		pF
C <sub>IO</sub>	B port	V <sub>O</sub> = 3.0V or 0		7.2		pF
	A port	V <sub>O</sub> = V <sub>TT</sub> or 0		4.6		

### NOTES:

- All typical values are measured at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

## AC CHARACTERISTICS (3.3V ± 0.3V RANGE)

SYMBOL	PARAMETER	WAVEFORM	LIMITS (GTL)			LIMITS (GTL+)			UNIT
			V <sub>CC</sub> = 3.3V ± 0.3V V <sub>REF</sub> = 0.8V			V <sub>CC</sub> = 3.3V ± 0.3V V <sub>REF</sub> = 1.0V			
			MIN	TYP <sup>1</sup>	MAX	MIN	TYP <sup>1</sup>	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Bn to An	2		2.0	2.8		2.0	2.8	ns
				1.8	2.5		1.8	2.5	
t <sub>PLH</sub> t <sub>PHL</sub>	An to Bn	3		4.4	6.5		4.4	5.7	ns
				4.7	5.8		4.5	5.1	
t <sub>PLH</sub> t <sub>PHL</sub>	LEn to Bn	1		3.5	4.9		3.5	4.9	ns
				3.4	4.2		3.4	4.2	

### NOTE:

- All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

## AC SETUP REQUIREMENT (3.3V ± 0.3V RANGE)

Over recommended ranges of supply voltage.<sup>1</sup>

SYMBOL	PARAMETER	WAVEFORM	LIMITS (GTL)		LIMITS (GTL+)		UNIT
			V <sub>CC</sub> = 3.3V ± 0.3V V <sub>REF</sub> = 0.8V		V <sub>CC</sub> = 3.3V ± 0.3V V <sub>REF</sub> = 1.0V		
			MIN	MAX	MIN	MAX	
t <sub>S(H)</sub> t <sub>S(L)</sub>	Setup time (An to LEn)	4		1.3 1.5		1.2 1.5	ns
t <sub>H(H)</sub> t <sub>H(L)</sub>	Hold time (An to LEn)	4		0.0 0.0		0.0 0.0	ns
t <sub>w(H)</sub>	LEn pulse width	2		1.1		1.1	ns

### NOTE:

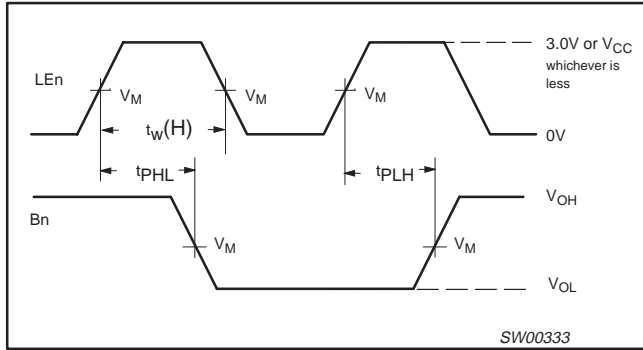
- These parameters are warranted but not production tested.

# Quad GTL/GTL+ to LVTTTL/TTL bidirectional latched translator

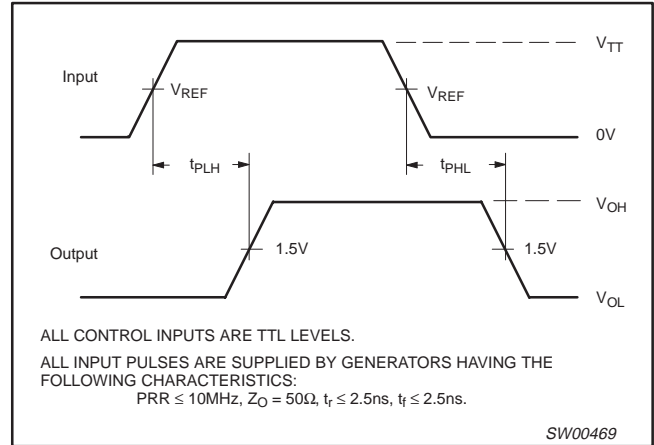
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## AC WAVEFORMS

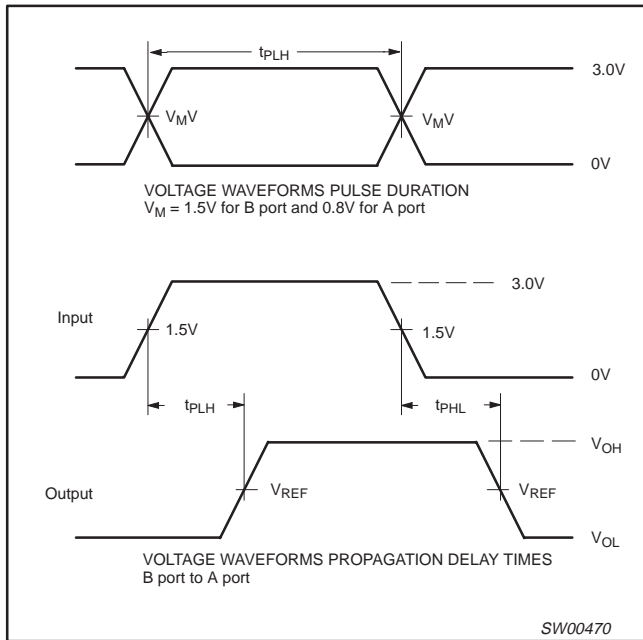
$V_M = 1.5V$  at  $V_{CC} \geq 3.0V$ ,  $V_M = V_{CC}/2$  at  $V_{CC} \leq 2.7V$  for A ports and control pins  
 $V_M = V_{REF}$  for B ports  
 $V_X = V_{OL} + 0.3V$  at A ports  
 $V_Y = V_{OH} - 0.3V$  at A ports  
 $V_X = V_{REF}$  at B ports



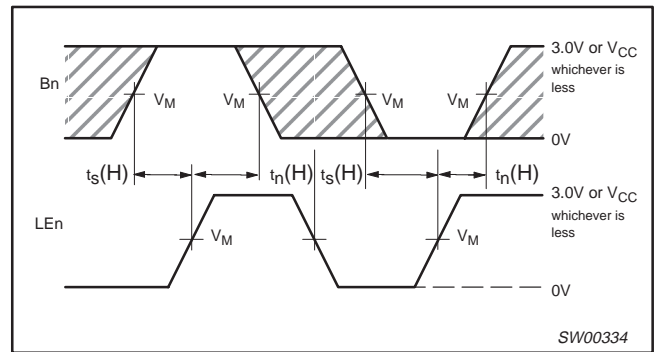
**Waveform 1. Propagation delay, Enable to Output and Enable Pulse Width**



**Waveform 3. Propagation delay A port to B port**



**Waveform 2.**



**Waveform 4. Data Setup and Hold Times**

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## TEST CIRCUIT

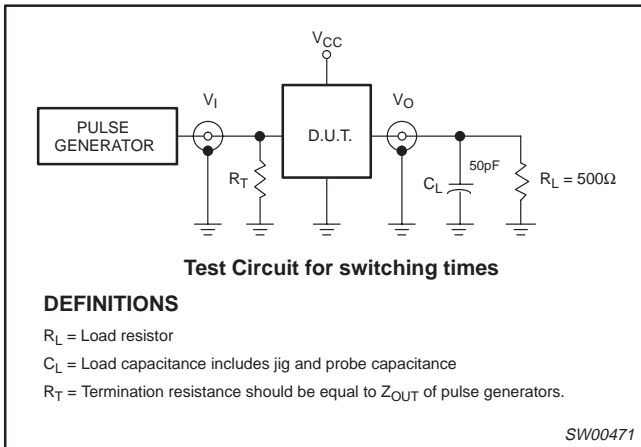


Figure 1. Load circuitry for switching times

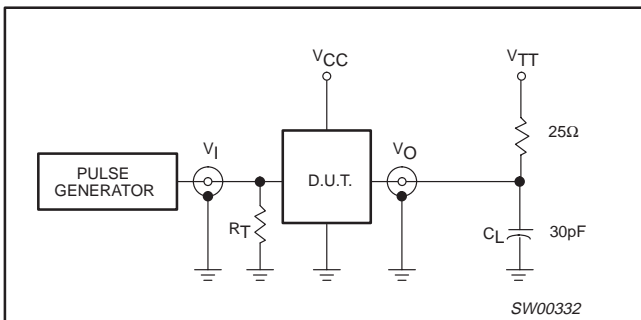


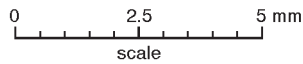
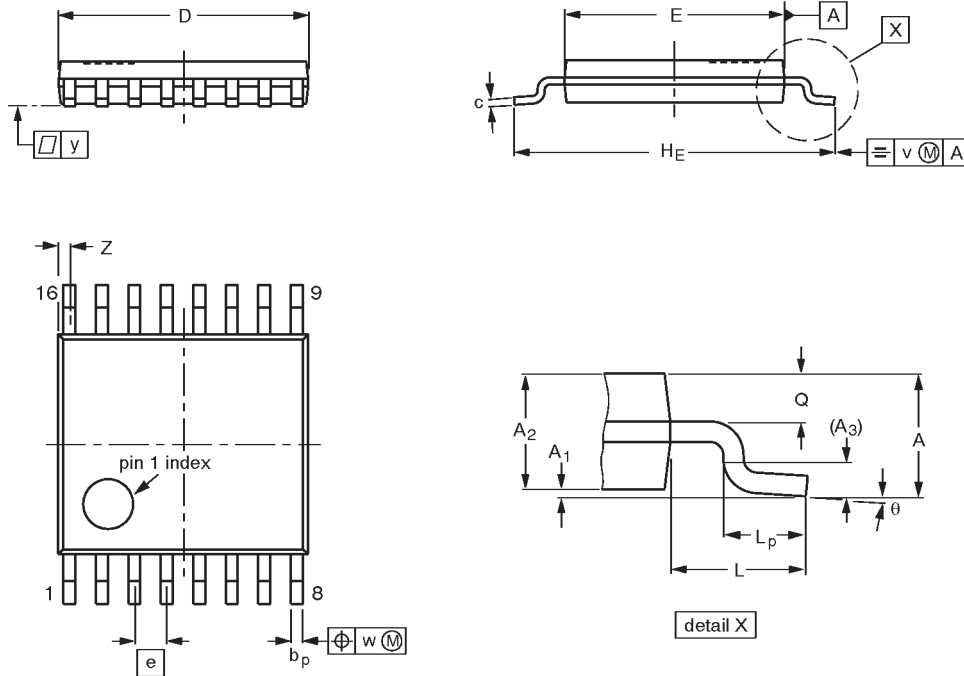
Figure 2. Load circuit for A outputs

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**TSSOP16:** plastic thin shrink small outline package; 16 leads; body width 4.4 mm

**SOT403-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				94-07-12 95-04-04



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**NOTES**

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

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