HIP7030A0

PRELIMINARY

April 1994

J1850 8-Bit 68HC05 Microcontroller Emulator Version

Features

- **HIP7030A2 Microcontroller Emulation**
  - **All HIP7030A2 Hardware and Software Features**
  - **Timing and Performance Equivalent to HIP7030A2**
- **On-Chip Memory**
  - **176 Bytes of RAM - No ROM**
- **Full 8K Byte Address Space Available Externally**
- **Non-Multiplexed External Address and Data Lines**
  - **I/O Memory Interface Matches Industry Standard EPROM/EEPROMS for True Emulation with Two Chips**
- **FS Line Identifies Fetch Cycles for Breakpoint Logic**
- **-40°C to +125°C Operating Range**
- **Single 3.0V to 6.0V Supply**
- **Available in 68 Lead PLCC Packages**

Description

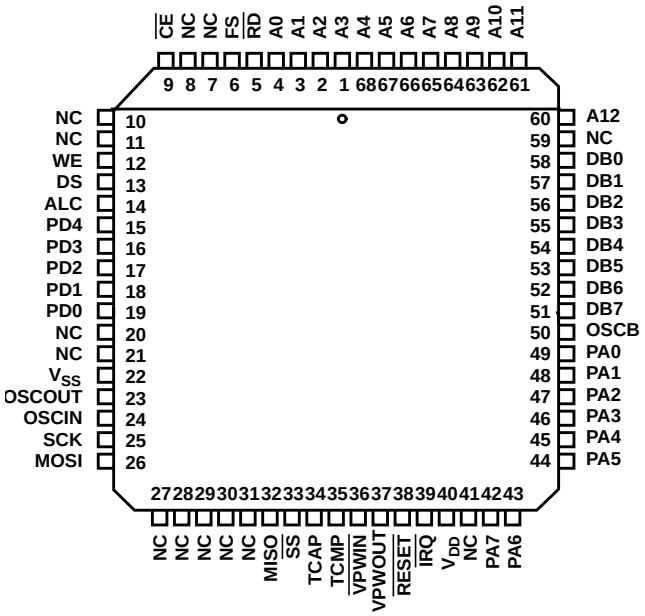
The HIP7030A0 Emulator is functionally equivalent to the HIP7030A2 microcontroller with the addition of external data bus, address bus, and control signals which provide off chip address capability. It is designed to permit prototype and pre-production development of systems for mask programmed applications. The HIP7030A0 is also intended for construction of development systems for the HIP7030A2.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP7030A0M	-40°C to +125°C	68 Lead Plastic LCC

Pinout

HIP7030A0 (PLCC)
TOP VIEW



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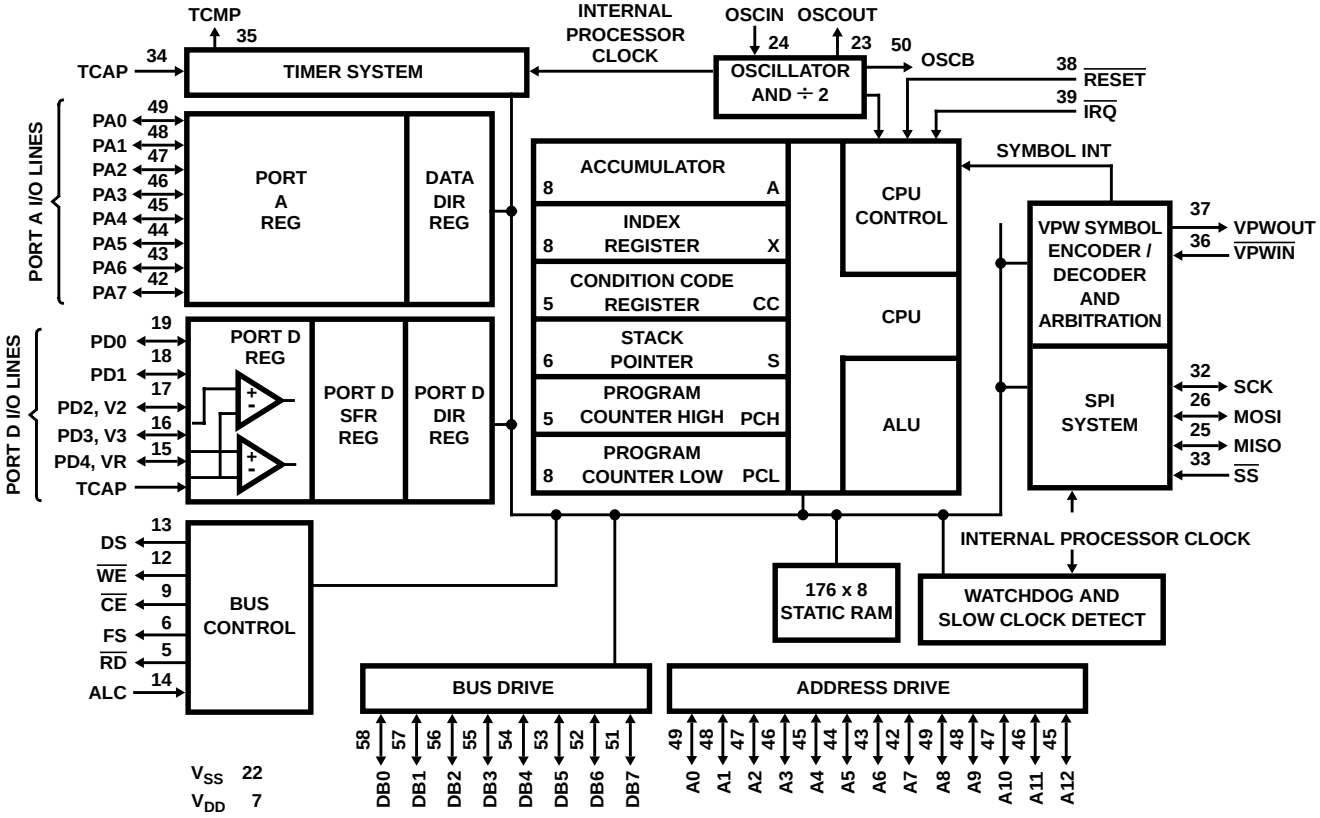
Block Diagram



Absolute Maximum Ratings

DC Supply Voltage, V_{DD} . . . . . -0.5 to +7V
Input Voltage, V_{IN} (Note 1) . . . . . (V_{SS}-0.3) to (V_{DD}+0.3)V
Self-Check Mode ($\overline{IRQ}$ Pin Only), V_{IN} . . (V_{SS}-0.3) to 2•(V_{DD}+0.3)V
Current Drain Per Pin (Excluding V_{DD} and V_{SS}) 25mA

Thermal Information

Thermal Resistance θ_{JA}
Plastic LCC Package . . . . . $55^oC/W$
Maximum Package Power Dissipation, P_D at 125^oC 450mW
Operating Temperature Range . . . . . -40^oC to $+125^oC$
Storage Temperature Range, T_{STG} . . . . . -65^oC to $+150^oC$
Lead Temperature (Soldering 10s) . . . . . $+265^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Control Timing

$V_{DD} = 5V_{DC} \pm 10\%$, $V_{SS} = 0V_{DC}$, $T_A = -40^oC$ to $+125^oC$ Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
FREQUENCY OF OPERATION						
Crystal Option	f_{OSC}		1	-	10	MHz
External Clock Option			1	-	10	MHz
INTERNAL OPERATING FREQUENCY						
Crystal (f_{OSC} + 2)	f_{OP}		0.5	-	5	MHz
External Clock (f_{OSC} + 2)			0.5	-	5	MHz
Cycle Time	t_{CYC}		200	-	-	ns

DC Electrical Specifications

$V_{DD} = 5V_{DC} \pm 10\%$, $V_{SS} = 0V_{DC}$, $T_A = -40^oC$ to $+125^oC$ Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Voltage	V_{OL}	I_{LOAD} < 10mA	-	-	0.1	V
	V_{OH}	I_{LOAD} > -10mA	V_{DD} -0.1	-	-	V
Output High Voltage: A0-A12, DB0-DB7, $\overline{CE}$, $\overline{RD}$, $\overline{WE}$, FS	V_{OH}	I_{LOAD} = 0.8mA	V_{DD} -0.8	-	-	V
Output Low Voltage: A0-A12, DB0-DB7, $\overline{CE}$, $\overline{RD}$, $\overline{WE}$, FS	V_{OH}	I_{LOAD} = 1.6mA	-	-	0.4	V
Input High Voltage: DB0-DB7	V_{IH}		-	0.5•V_{DD}	0.7•V_{DD}	V
Input Low Voltage: DB0-DB7	V_{IL}		0.3•V_{DD}	-	-	V
DB0-7 High Impedance Leakage Current:	I_{IL}		-10	-	+10	µA
Input Current	I_{IN}		-1	-	+1	µA
Capacitance	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
Supply Current: RUN	I_{RUN}		-	8	TBD	mA

NOTES:

1. This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})
2. Characteristics are listed for the signals unique to the Emulator IC. For details on the other signal pins see the HIP7030A2 data sheet.
3. Minimum frequency applies when ALC is low.

Read Cycle Timing (ALC = 0) (See Figure 1) V_{DD} = 5V_{DC} ±10%, V_{SS} = 0V_{DC}, T_A = -40°C to +125°C Unless Otherwise Specified.

NUMBER	SYMBOL	PARAMETER	MIN	MAX	UNITS
	f_{OSC}	OSCB Operating Frequency	1	10	MHz
(1)	t_{CYC}	Read Cycle Time	200	2000	ns
(2)	t_{AVCEL}	Address Setup Time Before $\overline{CE}$	-10	-	ns
(3)	t_{DVCEL}	Access Time From $\overline{CE}$	-	t_{CYC} - 80	ns
(4)	t_{DVRDL}	Access Time From $\overline{RD}$	-	0.75t_{CYC} - 80	ns
(5)	t_{DVAV}	Access Time From Address Change	-	t_{CYC} - 80	ns
(6)	t_{CEHAX}	Address Hold Time After $\overline{CE}$	0	-	ns
(7)	t_{CEHAX}	Data Hold Time After $\overline{CE}$	0	-	ns
(8)	t_{RDLDX}	Data Bus Driven From $\overline{RD}$ (Time to Data Active from High Impedance State)	0	-	ns
(9)	t_{RDHAX}	Data Hold Time After $\overline{RD}$ (Hold Time to High Impedance State)	0	-	ns
(10)	t_{OSCDS}	OSCB to DS Propagation Delay	5	25	ns

NOTE:

Minimum frequency applies when ALC is low.

Write Cycle Timing (ALC = 0) (See Figure 2) V_{DD} = 5V_{DC} ±10%, V_{SS} = 0V_{DC}, T_A = -40°C to +125°C Unless Otherwise Specified.

NUMBER	SYMBOL	PARAMETER	MIN	MAX	UNITS
	f_{OSC}	OSCB Operating Frequency	1	10	MHz
(1)	t_{CYC}	Write Cycle Time	200	2000	ns
(2)	t_{AVCEL}	Address Setup Time Before $\overline{CE}$	-10	-	ns
(3)	t_{AVWEL}	Address Setup Time Before $\overline{WE}$	0.25t_{CYC} - 25	-	-
(4)	t_{WEWE}	$\overline{WE}$ Pulse Width	0.5t_{CYC} - 10	-	ns
(5)	t_{DVWEH}	Data Set-up Time to $\overline{WE}$ Trailing Edge	0.75t_{CYC} - 75	-	ns
(6)	t_{WEHDX}	Data Hold Time After $\overline{WE}$ Trailing Edge	0.25t_{CYC} - 20	-	ns
(7)	t_{WEHAX}	Address Hold Time After $\overline{WE}$ Trailing Edge	0.25t_{CYC} - 20	-	ns
(8)	t_{OSCDS}	OSCB to DS Propagation Delay	5	25	ns

NOTE:

1. Minimum frequency applies when ALC is low.

Read Cycle Timing (ALC = 1) (See Figure 3) V_{DD} = 5V_{DC} ±10%, V_{SS} = 0V_{DC}, T_A = -40°C to +125°C Unless Otherwise Specified.

NUMBER	SYMBOL	PARAMETER	MIN	MAX	UNITS
	f_{OSC}	OSCB Operating Frequency		10	MHz

Read Cycle Timing (ALC = 1) (See Figure 3) V_{DD} = 5V_{DC} ±10%, V_{SS} = 0V_{DC}, T_A = -40°C to +125°C Unless Otherwise Specified.

NUMBER	SYMBOL	PARAMETER	MIN	MAX	UNITS
(1)	t_{CYC}	Read Cycle Time	200	-	ns
(2)	t_{RDOSC}	$\overline{RD}$, FS Setup Time Before OSCB	$0.5t_{CYC}$-25	-	ns
(3)	t_{DVCEL}	Access Time From $\overline{CE}$	-	t_{CYC}-80	ns
(4)	t_{DVOSC}	Access Time From OSCB	-	t_{CYC}-70	ns
(5)	t_{OSCAV}	Address Setup Time Before OSCB	$0.5t_{CYC}$-25	-	ns
(6)	t_{OSCAX}	Address Hold Time After OSCB	$0.5t_{CYC}$	-	ns
(7)	t_{OSCAX}	Data Hold Time After OSCB	10	-	ns
(8)	t_{RDLDX}	Data Bus Driven From $\overline{CE}$ (Time to Data Active from High Impedance State)	0	-	ns
(9)	t_{OSCRD}	$\overline{RD}$, FS Hold Time After OSCB	$0.5t_{CYC}$	-	ns
(10)	t_{OSCDS}	OSCB to DS Propagation Delay	5	25	ns

NOTE:

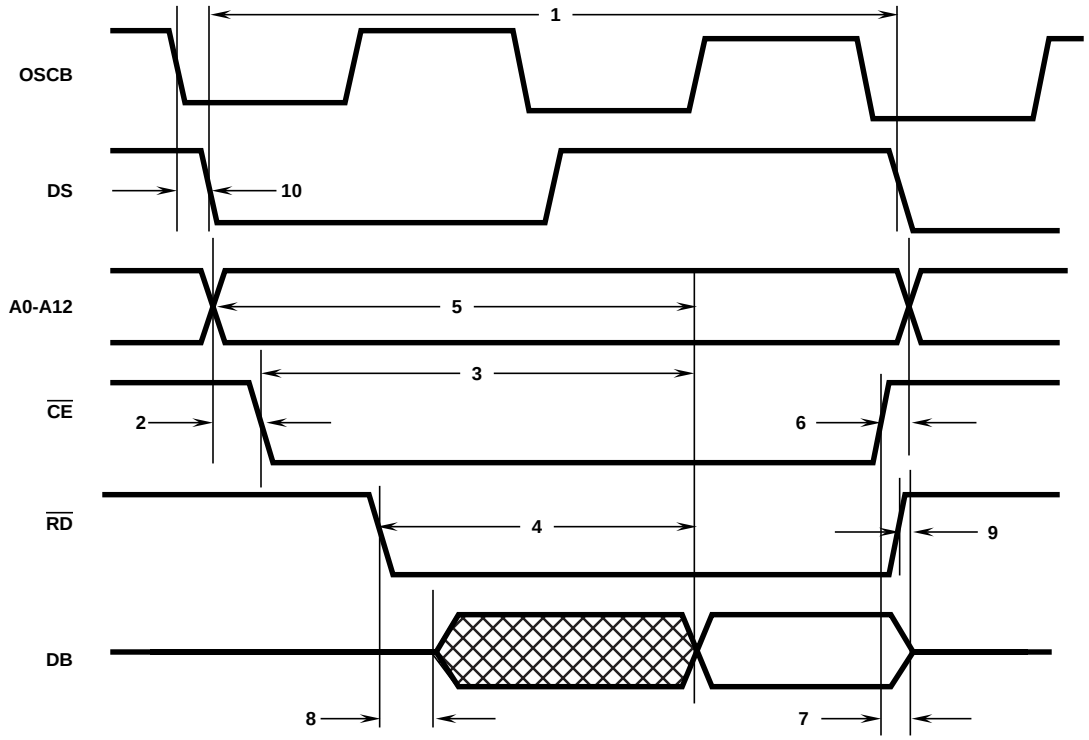
1. Minimum frequency applies when ALC is high.

Write Cycle Timing (ALC = 1) (See Figure 4) V_{DD} = 5V_{DC} ±10%, V_{SS} = 0V_{DC}, T_A = -40°C to +125°C Unless Otherwise Specified.

NUMBER	SYMBOL	PARAMETER	MIN	MAX	UNITS
	f_{OSC}	OSCB Operating Frequency		10	MHz
(1)	t_{CYC}	Write Cycle Time	200	-	ns
(2)	t_{RDOSC}	$\overline{RD}$, FS Setup Time Before OSCB	$0.5t_{CYC}$-25	-	ns
(3)	t_{DVOSC}	Data Setup Time Before OSCB		$0.75t_{CYC}$-95	ns
(4)	t_{OSCAV}	Address Setup Time Before OSCB	$0.5t_{CYC}$-25	-	ns
(5)	t_{OSCAX}	Address Hold Time After OSCB	$0.5t_{CYC}$	-	ns
(6)	t_{OSCAX}	Data Hold Time After OSCB	10	-	ns
(7)	t_{OSCDX}	Data Bus Driven From OSCB (Time to Data Active from High Impedance State)	$.25t_{CYC}$-25	-	ns
(8)	t_{OSCRD}	$\overline{RD}$, FS Hold Time After OSCB	$0.5t_{CYC}$	-	ns
(9)	t_{OSCDS}	OSCB to DS Propagation Delay	5	25	ns

NOTE:

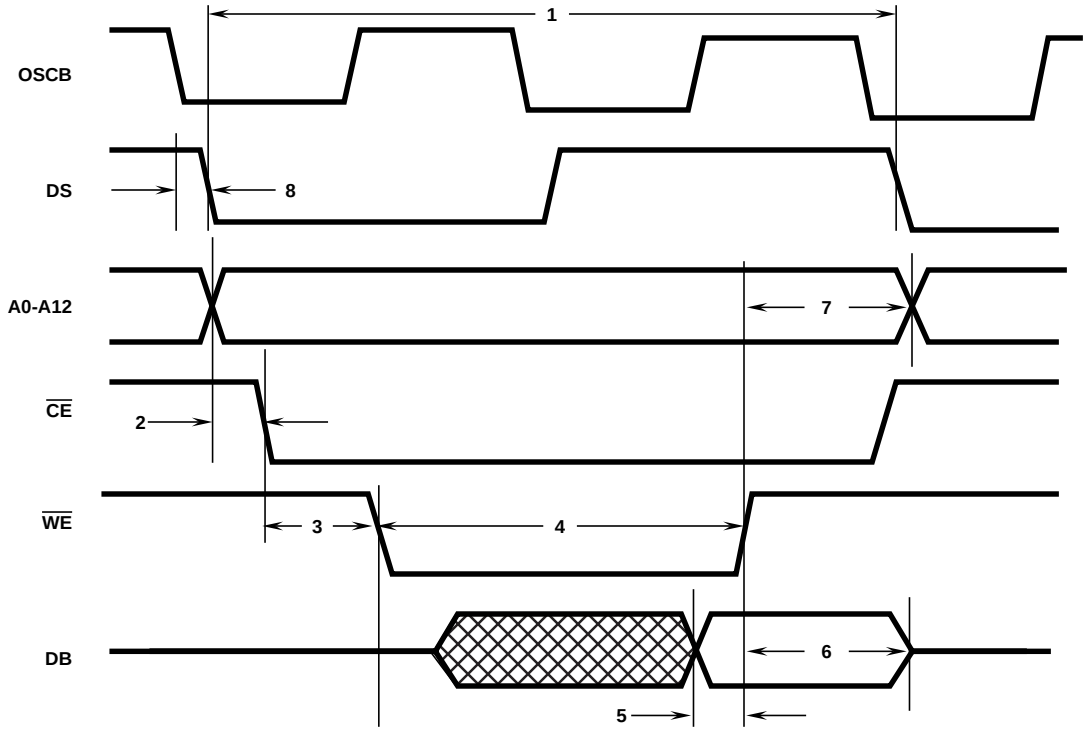
1. Minimum frequency applies when ALC is high.



NOTE:

1. Measurement points are V_{OL}, V_{OH}, V_{IL} and V_{IH}.

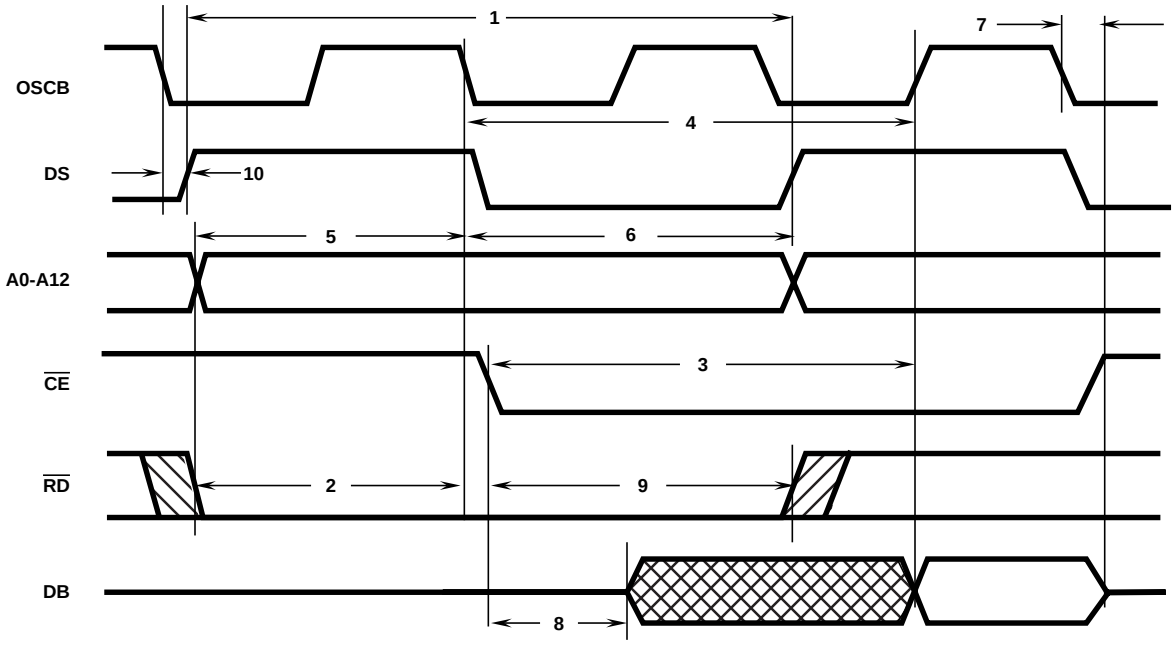
FIGURE 1. READ CYCLE TIMING DIAGRAM (ALC = 0)



NOTE:

1. Measurement points are V_{OL}, V_{OH}, V_{IL} and V_{IH}.

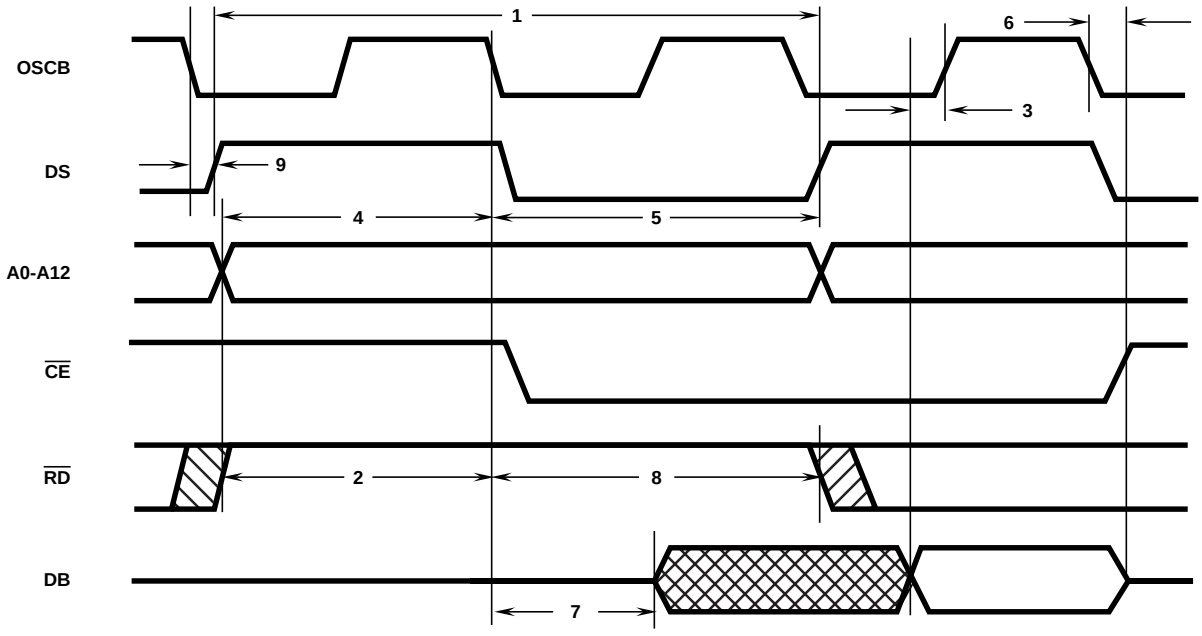
FIGURE 2. WRITE CYCLE TIMING DIAGRAM (ALC = 0)



NOTES:

1. Measurement points are V_{OL}, V_{OH}, V_{IL} and V_{IH}.
2. Timing for FS is identical to RD timing.

FIGURE 3. READ CYCLE TIMING DIAGRAM (ALC = 1)



NOTES:

1. Measurement points are V_{OL}, V_{OH}, V_{IL} and V_{IH}.
2. Timing for FS is identical to RD timing.

FIGURE 4. WRITE CYCLE TIMING DIAGRAM (ALC = 1)

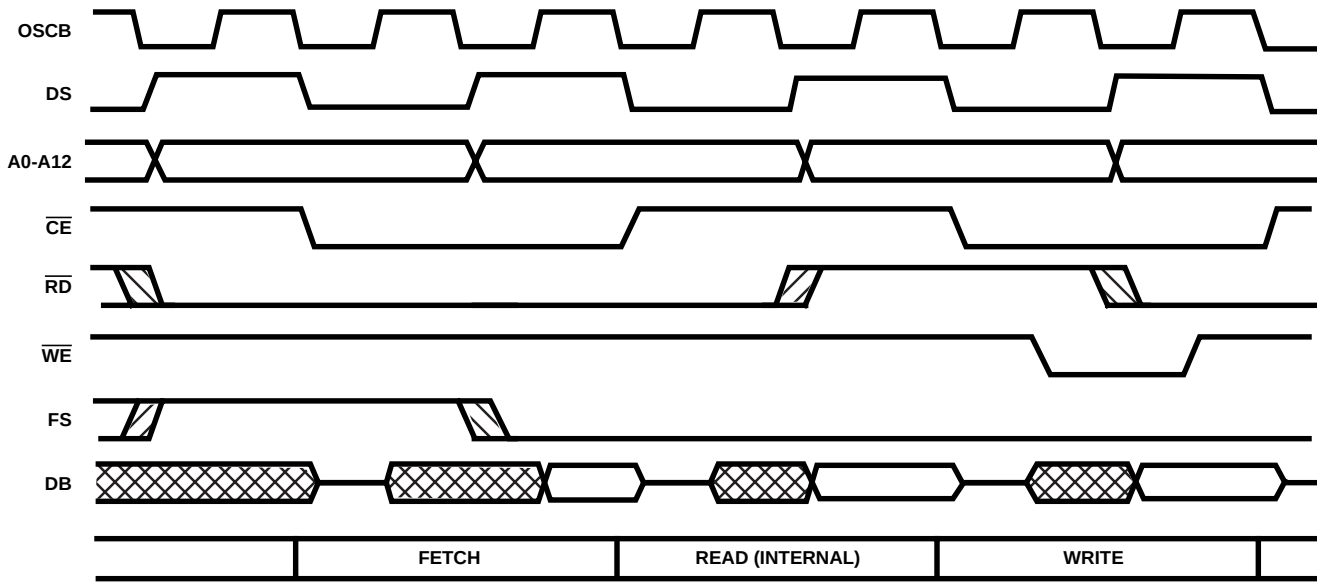


FIGURE 5. SIGNAL TIMING DIAGRAM (ALC = 1)

Functional Pin Description

This section provides a brief description of each of the pins of the HIP7030A0 microcontroller. A more detailed discussion is contained in the HIP7030A2 data sheet.

V_{DD} and V_{SS} (Power)

Power is supplied to the MCU using these two pins. V_{DD} is connected to the positive supply and V_{SS} is connected to the negative supply.

$\overline{IRQ}$ (Maskable Interrupt Request - Input)

The $\overline{IRQ}$ pin is negative edge-sensitive triggering. A high to low transition on the input to the $\overline{IRQ}$ pin will produce an interrupt.

In the event of an interrupt request, the MCU always completes the current instruction before it responds to the request. An internal mask can be used to inhibit the MCU from responding to $\overline{IRQ}$ interrupts.

An edge-sensitive $\overline{IRQ}$ interrupt is generated if the $\overline{IRQ}$ pin is pulled low for at least one t_{ILIH}. The occurrence of the low going pulse is registered in a flip-flop and the $\overline{IRQ}$ interrupt will be recognized even if the $\overline{IRQ}$ pin has returned to a high state before the interrupt can be serviced.

Once the edge-sensitive flip-flop is cleared (it is automatically cleared at the start of the interrupt service routine) the interrupt request is removed until the $\overline{IRQ}$ pin returns to a high level and once again goes low.

$\overline{RESET}$ (Master Reset - Input)

The HIP7030A2 contains an integrated Power-On Reset (POR) circuit and the $\overline{RESET}$ input is therefore not required for start-up. It can be used to reset the MCU internal state and provides for an orderly re-start of the software after initial power-up. A low level on the $\overline{RESET}$ pin will reset the HIP7030A0.

TCAP (Timer Capture - Input)

The TCAP input controls the input capture feature for the on-chip programmable timer system. The TCAP input is also used as the strobe signal to the Port D strobed outputs.

TCMP (Timer Compare - Output)

The TCMP pin provides an output for the output compare feature of the on-chip timer system.

**OSCIN (Oscillator Input - Input),
OSCOUT (Oscillator Output - Output),
OSCB (Oscillator Buffered Output - Output)**

OSCIN is the input and OSCOUT is the output of an inverter/amplifier which can be used to build either a quartz crystal or ceramic resonator based clock oscillator. Alternatively the OSCIN input can be driven from any external clock source which satisfies the CMOS schmitt trigger input level requirements of the OSCIN pin. OSCB is a squared, buffered version of the OSCIN signal, available for driving one external CMOS load. See Electrical Specifications of the HIP7030A2 for output drive and input level specifications.

The fundamental internal clock is derived by a divide-by-two of the external oscillator frequency (fOSC). All other internal clocks are also derived from the external frequency. These clocks include the input to the 16-bit Timer, the SPI Serial Clock (SCK), and the VPW Symbol Encoder/Decoder (SENDEC).

PA0-PA7 (Port A - Input/Output)

These eight I/O lines comprise Port A. The mode (i.e. - input or output) of each pin is software programmable. All Port A I/O lines are configured as inputs during power-on or $\overline{RESET}$.

PD0-PD4 (Port D - Input/Output)

These five I/O lines comprise Port D. As with PA0-PA7, the mode (i.e. - input or output) of each pin is software programmable. In addition a Special Function Register (SFRD) allows configuring PD0 and PD1 as "strobed" outputs, and/or PD2,PD3, and PD4 as inputs to an on-chip analog comparator.

All Port D I/O lines are configured as inputs during power-on or $\overline{\text{RESET}}$.

VPWOUT (Variable Pulse Width Out - Output),
$\overline{\text{VPWIN}}$ (Variable Pulse Width In - Input)

These two lines are used to interface to the J1850 bus transceiver.

VPWOUT is the pulse width modulated output of the SENDEC encoder block.

$\overline{\text{VPWIN}}$ is the inverted input to the SENDEC decoder block.

MISO (Master-in/Slave-out - Input/Output),
MOSI (Master-out/Slave-in - Input/Output),
SCK (Serial Clock - Input/Output),
$\overline{\text{SS}}$ (Slave Select - Input)

These four lines constitute the Serial Peripheral Interface (SPI) communications port. The MCU can be configured as a SPI "master" or as a SPI "slave". In master mode MOSI and SCK function as outputs and MISO functions as an input. In slave mode MOSI and SCK are inputs and MISO is an output. SS is always an input.

Serial data words are transmitted and received over the MISO/MOSI lines synchronously with the SCK clock stream. The word size is fixed at 8 bits. Single buffering is used which results in an inherent inter-byte delay. The master device always provides the synchronizing clock.

A low on the $\overline{\text{SS}}$ line causes the MCU to immediately assume the role of slave, regardless of it's current mode. This allows multi-master systems to be constructed with appropriate arbitration protocols.

ALC (Address Latch Control - Input)

The ALC input controls the timing and function of the address and memory control lines ($\overline{\text{CE}}$, $\overline{\text{RD}}$, $\overline{\text{WE}}$, and FS). For more information on each of these lines refer to the appropriate section.

When ALC is low the address and control lines are produced coincident with data bus transitions of the HIP7030A0's machine cycle. This mode allows direct interfacing to industry standard memory devices. Refer to the timing diagrams in **Electrical Specifications** for more details.

Driving ALC high causes several changes in the behavior of the address and control lines. These changes are intended to facilitate design of development systems for the HIP7030A2. When ALC is high the following occur:

- The Internal RAM is disabled and accesses to RAM space are mapped off-chip.
- A0-A12, FS, and $\overline{\text{RD}}$ are produced t_{CYC} cycle (i.e. 100ns with a 10MHz clock) ahead of data bus transitions of the HIP7030A0's machine cycle. The earlier availability of these address and control lines facilitates implementation of break detection and bus tracing logic. External latching of the address and control signals is required for interfacing to the memory of the development tool. The timing of $\overline{\text{CE}}$ and $\overline{\text{WE}}$ are not affected by ALC, and remain synchronized with data bus transfers.
- The $\overline{\text{RD}}$ signal is no longer gated with $\overline{\text{CE}}$ and is a full cycle wide, when ALC is high. $\overline{\text{RD}}$ indicates whether the ensuing data bus cycle will be a ***read of*** or ***write to*** memory-I/O space. It can be viewed as a R/$\overline{\text{W}}$ signal. $\overline{\text{RD}}$ provides R/$\overline{\text{W}}$ information for all cycles, internal as well as external.
- Resetting the HIP7030A0 with ALC = 1 disables the Slow Clock Detect circuits. The Watchdog can be disabled by writing to the Watchdog Status Register (WSR - location $1E), which has special features when ALC is high. The Slow Clock circuit is permanently disabled when ALC = 1. If the Slow Clock detect circuitry were allowed to run, stopping the CPU clock during breakpoint servicing would not be possible. The watchdog should be reset by the tool while interrogating the CPU.

The ALC input has an integrated pull-down device which allows floating this pin when interfacing to industry standard memory devices.

A0-A12

Address lines 0 through 12. When ALC = 0, A0-A12 are coincident with data bus transfers. When ALC = 1, A0-A12 change t_{CYC} ahead of the data bus transfers and must be externally latched. See the timing diagrams in the **Electrical Specifications** section for more details.

DB0-DB7

Bidirectional 8-bit non-multiplexed data bus lines. The data bus is an input during all reads from external memory-I/O space and during the first t_{CYC} of every machine cycle. At all other times it is an output. See the timing diagrams in the **Electrical Specifications** section for more details.

$\overline{\text{CE}}$ (Chip Enable - Output)

Chip Enable is an output signal used for selecting external memory or I/O. A low level indicates when external memory or I/O is being accessed. Note that the $\overline{\text{CE}}$ signal will not go true when addressing the unused locations of Page 0 I/O space even though the address lines will be valid.

$\overline{\text{RD}}$ (Read - Output)

$\overline{\text{RD}}$ is a status output signal which indicates direction of data flow with respect to external or internal memory space (a low level indicates a read from memory space). A read from internal memory or I/O will place data on the external data

bus. When ALC = 0, $\overline{RD}$ is internally gated with $\overline{CE}$, and generated in synchronization with data bus cycles. With ALC = 0, standard RAM, ROM, and EPROM devices can be directly connected to the HIP7030A0 with no additional components. When ALC = 1, $\overline{RD}$ is not gated by $\overline{CE}$ and is produced t_{CYC} cycle (i.e. 100ns with a 10MHz clock) ahead of data bus transitions of the HIP7030A0's machine cycle.

$\overline{WE}$ (Write Enable - Output)

Write Enable is an active low output pulse for use in writing data to external RAM memory. A low level indicates valid data on the data bus. $\overline{WE}$ is internally gated with $\overline{CE}$ for writing to external memory. Since, in most systems, external memory is substituting for mask programmed ROM, $\overline{WE}$ is frequently not used.

DS (Data Strobe - Output)

The Data Strobe output provides a pulse when address and data are valid. DS can be used to transfer data to or from a peripheral or memory and occurs every cycle and is also used for synchronizing development tools to the oscillator clock. DS is a continuous signal at $f_{OSC} \div 2$, except when the Emulator is in the WAIT or STOP mode. See the timing diagrams in the **Electrical Specifications** section for more details.

FS (Fetch Status - Output)

The FS output signal goes true to indicate an opcode fetch cycle is in progress. When ALC = 0, FS will be coincident with the data transfer of the fetch. When ALC = 1, FS is produced t_{CYC} cycle (i.e. 100ns with a 10MHz clock) ahead of data bus transitions of the HIP7030A0's machine cycle. See the timing diagrams in the **Electrical Specifications** section for more details.

Watchdog Status Register

When ALC is high, the HIP7030A0's Watchdog Status Register (WSR - location $1E) provides the ability to selectively enable and disable the Watchdog Timer logic of the HIP7030A0.

The user of a development tool should be cautioned against accidently clearing the WDE bit of this register during final code prove-out. During initial code development the user may want to intentionally clear this bit to eliminate the need to insert watchdog handling routines. The clearing of the bit must be done following every reset.

Reset presets the WDE bit of the WSR to enable the Watchdog Timer.

7	6	5	4	3	2	1	0
-	-	-	-	-	-	WDE	WDF

WATCHDOG STATUS REGISTER

Bit 7,6,5,4,3,2 - Unused

Bit 1 - WDE

When WDE (WatchDog Enable) is low, the Watchdog Timer is disabled. When ALC is high, WDE is forced high by any reset. The WDE bit should normally be cleared when servicing a breakpoint (if OSCIN is being clocked), to avoid a Watchdog Reset while interrogating the CPU.

The WDE bit controls the Watchdog Reset, but it doesn't inhibit the Watchdog Timer from advancing. Prior to re-enabling the WDE bit, the Watchdog Timer should normally be reset by writing $55, $AA to the Watchdog Reset Register (WDRR, location $1D). This implies that each breakpoint should generate a Watchdog Reset. To verify proper watchdog action the user should run final code with no breaks. In some cases the number of CPU cycles utilized in the break may be low enough to allow the watchdog to run without causing premature watchdog timeouts.

Bit 0 - WDF

The WatchDog flag (WDF), is set when a Watchdog timeout causes a COP Reset. This flag is used to distinguish a Slow Clock Detect from a Watchdog Timeout in the COP Reset service routine.

Writing a 0 to the Watchdog Reset Register (WDRR, location $1D) clears the WDF flag. WDF is cleared by Power-on Reset, but unaffected by all other types of resets. For this reason, WDF should normally be cleared (by writing a 0 to the WDRR) following each read of the WSR.

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