

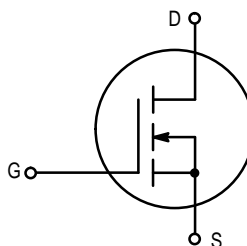
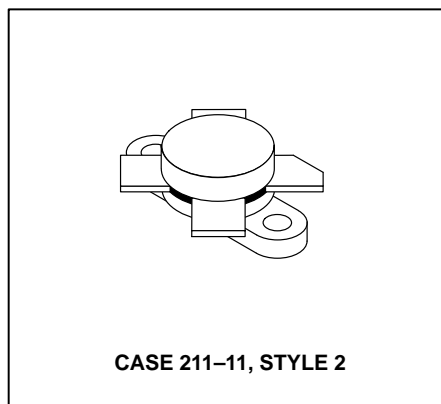
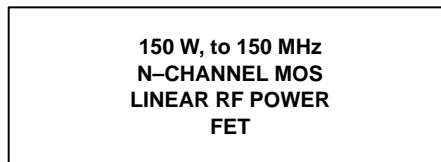
# The RF MOSFET Line

## RF Power Field-Effect Transistor

### N-Channel Enhancement-Mode

Designed primarily for linear large-signal output stages up to 150 MHz frequency range.

- Specified 28 Volts, 30 MHz Characteristics
  - Output Power = 150 Watts
  - Power Gain = 15 dB (Typ)
  - Efficiency = 40% (Typ)
- Superior High Order IMD
- IMD<sub>(d3)</sub> (150 W PEP) — -30 dB (Typ)
- IMD<sub>(d11)</sub> (150 W PEP) — -60 dB (Typ)
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR



#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	65	Vdc
Drain-Gate Voltage	V <sub>DGO</sub>	65	Vdc
Gate-Source Voltage	V <sub>GS</sub>	±40	Vdc
Drain Current — Continuous	I <sub>D</sub>	16	Adc
Total Device Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	300 1.7	Watts W/°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Operating Junction Temperature	T <sub>J</sub>	200	°C

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	0.6	°C/W

**Handling and Packaging** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain–Source Breakdown Voltage ( $V_{GS} = 0, I_D = 100 \text{ mA}$ )	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 28 \text{ Vdc}, V_{GS} = 0$ )	$I_{DSS}$	—	—	5.0	mAdc
Gate–Body Leakage Current ( $V_{GS} = 20 \text{ Vdc}, V_{DS} = 0$ )	$I_{GSS}$	—	—	1.0	$\mu\text{Adc}$

**ON CHARACTERISTICS**

Gate Threshold Voltage ( $V_{DS} = 10 \text{ V}, I_D = 100 \text{ mA}$ )	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage ( $V_{GS} = 10 \text{ V}, I_D = 10 \text{ Adc}$ )	$V_{DS(on)}$	0.1	0.9	1.5	Vdc
Forward Transconductance ( $V_{DS} = 10 \text{ V}, I_D = 5.0 \text{ A}$ )	$g_{fs}$	4.0	7.0	—	mhos

**DYNAMIC CHARACTERISTICS**

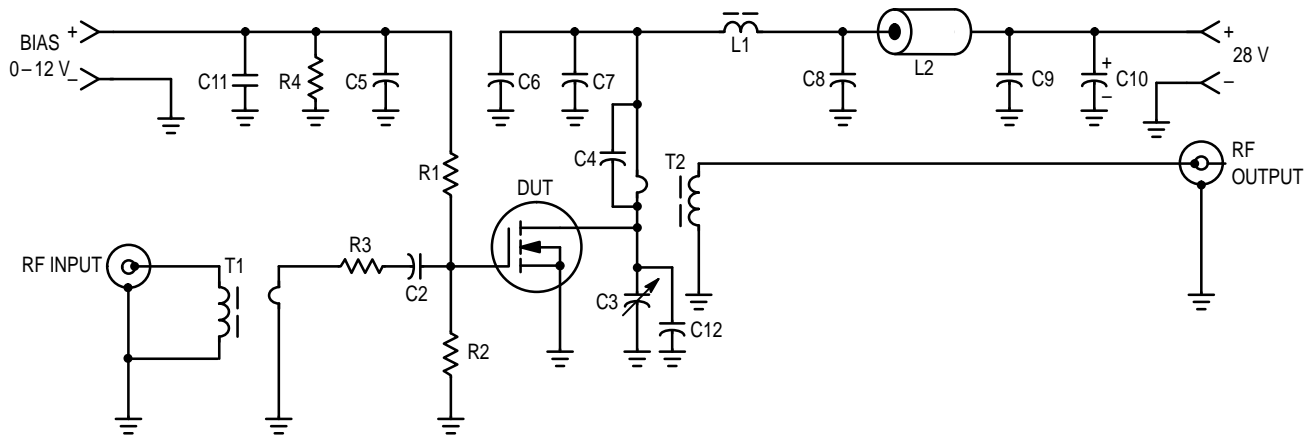
Input Capacitance ( $V_{DS} = 28 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$ )	$C_{iss}$	—	450	—	pF
Output Capacitance ( $V_{DS} = 28 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$ )	$C_{oss}$	—	400	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 28 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$ )	$C_{rss}$	—	75	—	pF

**FUNCTIONAL TESTS (SSB)**

Common Source Amplifier Power Gain ( $V_{DD} = 28 \text{ V}, P_{out} = 150 \text{ W (PEP)}, I_{DQ} = 250 \text{ mA}$ )	(30 MHz) (150 MHz)	$G_{ps}$	— —	15 6.0	— —	dB
Drain Efficiency ( $V_{DD} = 28 \text{ V}, P_{out} = 150 \text{ W (PEP)}, f = 30; 30.001 \text{ MHz}, I_D (\text{Max}) = 6.5 \text{ A}$ )		$\eta$	—	40	—	%
Intermodulation Distortion (1) ( $V_{DD} = 28 \text{ V}, P_{out} = 150 \text{ W (PEP)}, f_1 = 30 \text{ MHz}, f_2 = 30.001 \text{ MHz}, I_{DQ} = 250 \text{ mA}$ )		IMD(d3) IMD(d11)	— —	-30 -60	— —	dB
Load Mismatch ( $V_{DD} = 28 \text{ V}, P_{out} = 150 \text{ W (PEP)}, f = 30; 30.001 \text{ MHz}, I_{DQ} = 250 \text{ mA}, \text{VSWR } 30:1 \text{ at all Phase Angles}$ )		$\psi$	No Degradation in Output Power			

NOTE:

- To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



- C2, C5, C6, C7, C8, C9 — 0.1  $\mu\text{F}$  Ceramic Chip or Monolithic with Short Leads
- C3 — Arco 469
- C4 — 820 pF Unencapsulated Mica or Dipped Mica with Short Leads
- C10 — 10  $\mu\text{F}/100 \text{ V}$  Electrolytic
- C11 — 1  $\mu\text{F}, 50 \text{ V},$  Tantalum
- C12 — 330 pF, Dipped Mica (Short leads)

- L1 — VK200/4B Ferrite Choke or Equivalent, 3.0  $\mu\text{H}$
- L2 — Ferrite Bead(s), 2.0  $\mu\text{H}$
- R1, R2 — 51  $\Omega/1.0 \text{ W}$  Carbon
- R3 — 1.0  $\Omega/1.0 \text{ W}$  Carbon or Parallel Two 2  $\Omega, 1/2 \text{ W}$  Resistors
- R4 — 1 k $\Omega/1/2 \text{ W}$  Carbon
- T1 — 16:1 Broadband Transformer
- T2 — 1:25 Broadband Transformer

**Figure 1. 30 MHz Test Circuit (Class AB)**

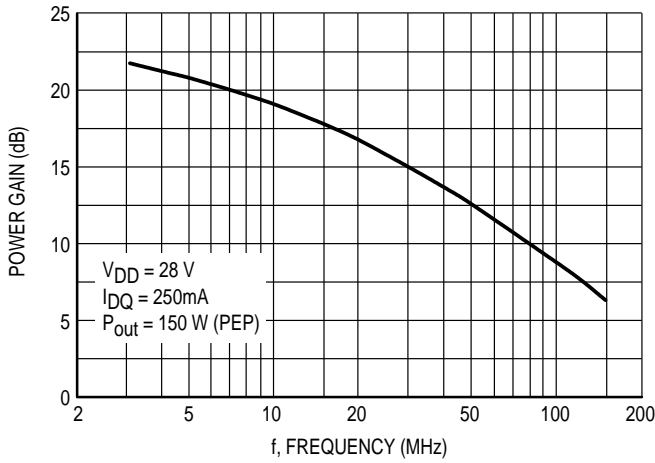


Figure 2. Power Gain versus Frequency

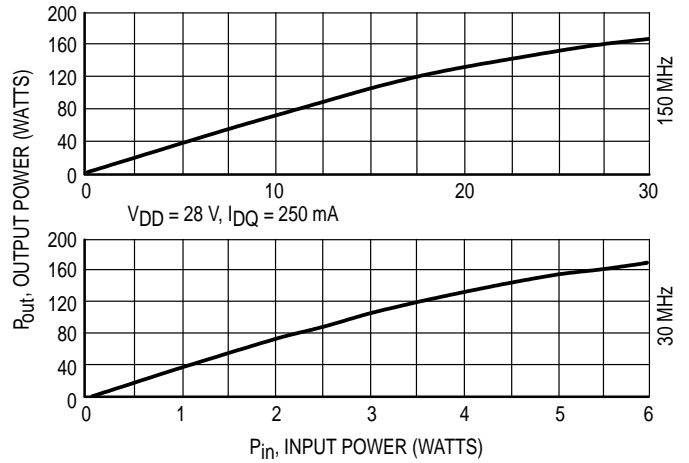


Figure 3. Output Power versus Input Power

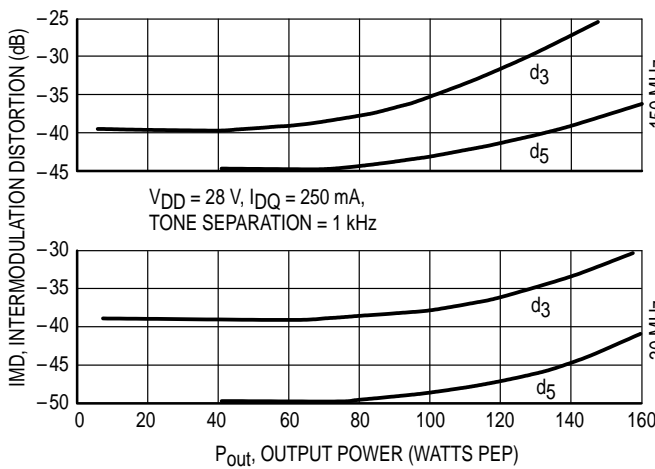


Figure 4. IMD versus  $P_{out}$

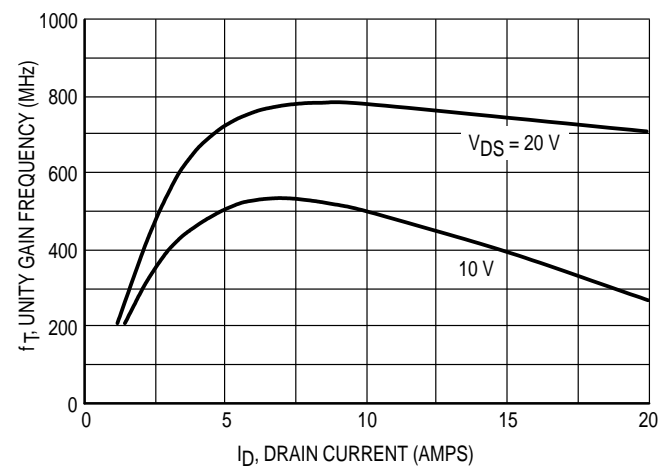


Figure 5. Common Source Unity Gain Frequency versus Drain Current

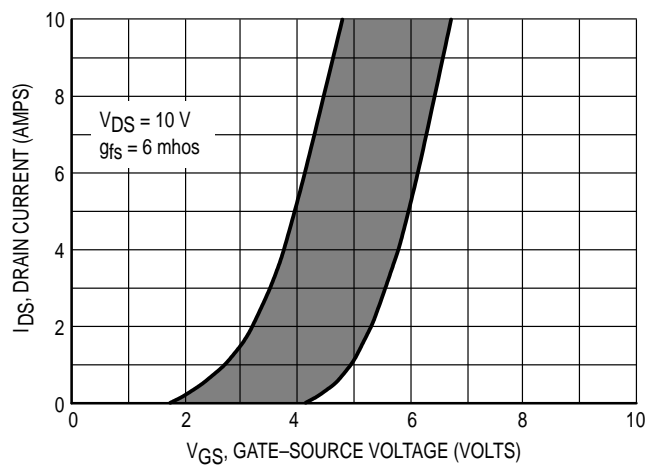
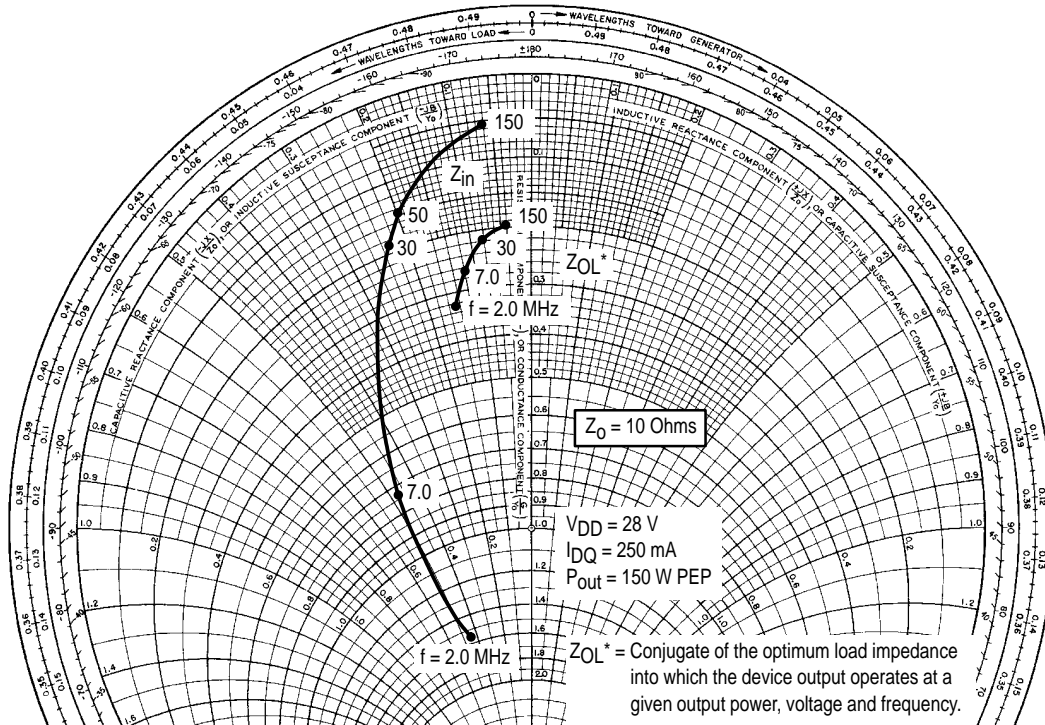
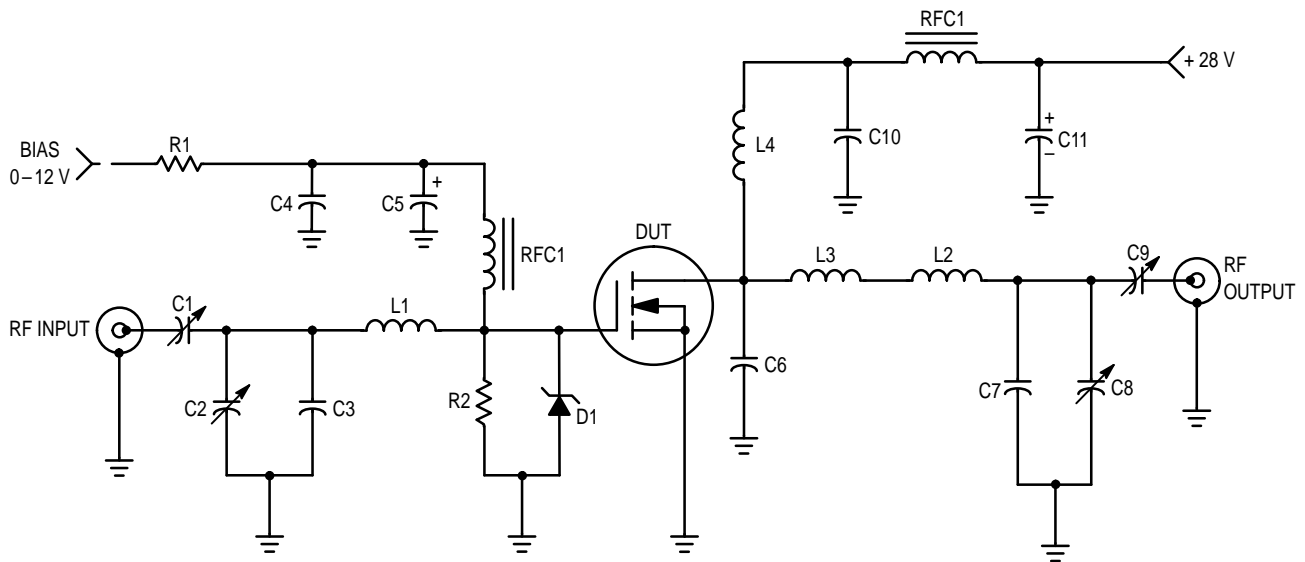


Figure 6. Gate Voltage versus Drain Current



NOTE: Gate Shunted by 25 Ohms.

Figure 7. Series Equivalent Impedance



- C1, C2, C8 — Arco 463 or equivalent
- C3 — 25 pF, Unelco
- C4 — 0.1  $\mu\text{F}$ , Ceramic
- C5 — 1.0  $\mu\text{F}$ , 15 WV Tantalum
- C6 — 15 pF, Unelco J101
- C7 — 25 pF, Unelco J101
- C9 — Arco 262 or equivalent
- C10 — 0.05  $\mu\text{F}$ , Ceramic
- C11 — 15  $\mu\text{F}$ , 35 WV Electrolytic

- L1 — 3/4", #18 AWG into Hairpin
- L2 — Printed Line, 0.200" x 0.500"
- L3 — 7/8", #16 AWG into Hairpin
- L4 — 2 Turns, #16 AWG, 5/16 ID
- RFC1 — 5.6  $\mu\text{H}$ , Molded Choke
- RFC2 — VK200-4B
- R1, R2 — 150  $\Omega$ , 1.0 W Carbon

Figure 8. 150 MHz Test Circuit (Class AB)

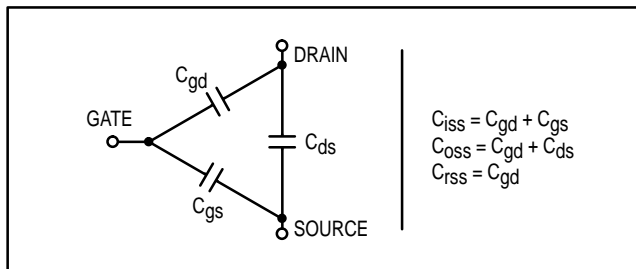
## RF POWER MOSFET CONSIDERATIONS

### MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain ( $C_{gd}$ ), and gate-to-source ( $C_{gs}$ ). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain-to-source ( $C_{ds}$ ).

These capacitances are characterized as input ( $C_{iss}$ ), output ( $C_{oss}$ ) and reverse transfer ( $C_{rss}$ ) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The  $C_{iss}$  can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



### LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to  $f_T$  for bipolar transistors.

Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

### DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance,  $V_{DS(on)}$ , occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs,  $V_{DS(on)}$  has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

### GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of  $10^9$  ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage,  $V_{GS(th)}$ .

**Gate Voltage Rating** — Never exceed the gate voltage rating. Exceeding the rated  $V_{GS}$  can result in permanent damage to the oxide layer in the gate region.

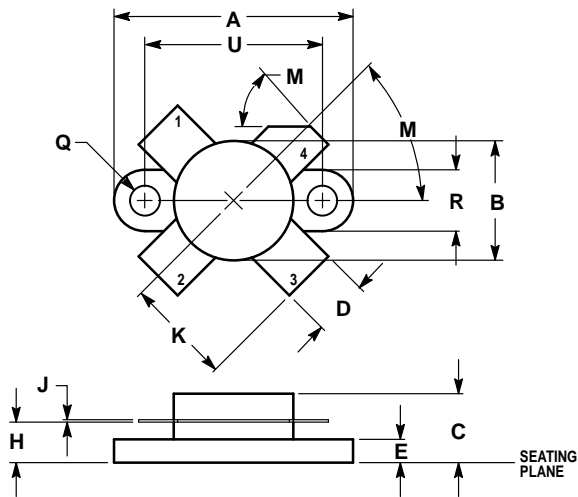
**Gate Termination** — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

**Gate Protection** — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

## EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector .....	Drain
Emitter .....	Source
Base .....	Gate
$V_{(BR)CES}$ .....	$V_{(BR)DSS}$
$V_{CBO}$ .....	$V_{DGO}$
$I_C$ .....	$I_D$
$I_{CES}$ .....	$I_{DSS}$
$I_{EBO}$ .....	$I_{GSS}$
$V_{BE(on)}$ .....	$V_{GS(th)}$
$V_{CE(sat)}$ .....	$V_{DS(on)}$
$C_{ib}$ .....	$C_{iss}$
$C_{ob}$ .....	$C_{oss}$
$h_{fe}$ .....	$g_{fs}$
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$ .....	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

## PACKAGE DIMENSIONS



- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.960	0.990	24.39	25.14
B	0.465	0.510	11.82	12.95
C	0.229	0.275	5.82	6.98
D	0.216	0.235	5.49	5.96
E	0.084	0.110	2.14	2.79
H	0.144	0.178	3.66	4.52
J	0.003	0.007	0.08	0.17
K	0.435	—	11.05	—
M	45°NOM		45°NOM	
Q	0.115	0.130	2.93	3.30
R	0.246	0.255	6.25	6.47
U	0.720	0.730	18.29	18.54

- STYLE 2:  
 PIN 1. SOURCE  
 2. GATE  
 3. SOURCE  
 4. DRAIN

**CASE 211-11  
 ISSUE N**

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