

The RF MOSFET Line
RF Power Field Effect Transistors
N-Channel Enhancement-Mode Lateral MOSFETs

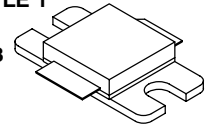
MRF18030ALR3
MRF18030ALSR3

Designed for GSM and EDGE base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. Specified for GSM 1805 - 1880 MHz.

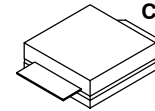
- Typical GSM Performance:
 Power Gain - 14 dB (Typ) @ 30 Watts
 Efficiency - 50% (Typ) @ 30 Watts
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 30 W Output Power
- Excellent Thermal Stability
- Low Gold Plating Thickness on Leads, 40μ" Nominal.
- in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.

1.8 - 1.88 GHz, 30 W, 26 V
GSM/GSM EDGE
LATERAL N-CHANNEL
RF POWER MOSFETs

CASE 465E-04, STYLE 1
NI-400
MRF18030ALR3



CASE 465F-04, STYLE 1
NI-400S
MRF18030ALSR3



MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|------------------|--------------|---------------|
| Drain-Source Voltage | V _{DSS} | 65 | Vdc |
| Gate-Source Voltage | V _{GS} | -0.5, +15 | Vdc |
| Total Device Dissipation @ T _C = 25°C Derate above 25°C | P _D | 83.3 0.48 | Watts W/°C |
| Storage Temperature Range | T _{stg} | - 65 to +150 | °C |
| Operating Junction Temperature | T _J | 200 | °C |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Value | Unit |
|--------------------------------------|------------------|-------|------|
| Thermal Resistance, Junction to Case | R _{θJC} | 2.1 | °C/W |

ESD PROTECTION CHARACTERISTICS

| Test Conditions | Class |
|------------------|--------------|
| Human Body Model | 2 (Minimum) |
| Machine Model | M3 (Minimum) |

NOTE - **CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C, 50 ohm system unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | |
|--|----------------------|----|---|---|------|
| Drain-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 20 μAdc) | V _{(BR)DSS} | 65 | — | — | Vdc |
| Zero Gate Voltage Drain Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc) | I _{DSS} | — | — | 1 | μAdc |
| Gate-Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc) | I _{GSS} | — | — | 1 | μAdc |

ON CHARACTERISTICS

| | | | | | |
|---|---------------------|---|------|-----|-----|
| Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 100 μAdc) | V _{GS(th)} | 2 | 3 | 4 | Vdc |
| Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 250 mAdc) | V _{GS(Q)} | 2 | 3.9 | 4.5 | Vdc |
| Drain-Source On-Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc) | V _{DS(on)} | — | 0.29 | 0.4 | Vdc |
| Forward Transconductance (V _{DS} = 10 Vdc, I _D = 1 Adc) | g _{fs} | — | 2 | — | S |

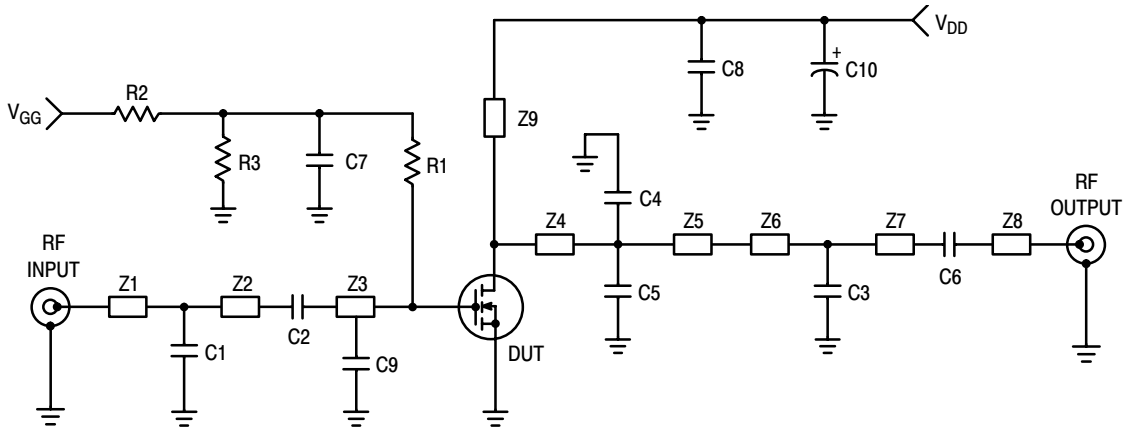
DYNAMIC CHARACTERISTICS

| | | | | | |
|--|------------------|---|-----|---|----|
| Reverse Transfer Capacitance (1) (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc) | C _{rss} | — | 1.3 | — | pF |
|--|------------------|---|-----|---|----|

FUNCTIONAL TESTS (In Motorola Test Fixture) (2)

| | | | | | |
|--|-----------------|---|-----|----|-------|
| Output Power, 1 dB Compression Point (V _{DD} = 26 Vdc, I _{DQ} = 250 mA, f = 1805 - 1880 MHz) | P1dB | 27 | 30 | — | Watts |
| Common-Source Amplifier Power Gain @ 30 W (V _{DD} = 26 Vdc, I _{DQ} = 250 mA, f = 1805 - 1880 MHz) | G _{ps} | 13 | 14 | — | dB |
| Drain Efficiency @ 30 W (V _{DD} = 26 Vdc, I _{DQ} = 250 mA, f = 1805 - 1880 MHz) | η | 46.5 | 50 | — | % |
| Input Return Loss @ 30 W (V _{DD} = 26 Vdc, I _{DQ} = 250 mA, f = 1805 - 1880 MHz) | IRL | — | -12 | -9 | dB |
| Output Mismatch Stress @ 30 W (V _{DD} = 26 Vdc, I _{DQ} = 250 mA, f ₁ = 1805 - 1880 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests) | Ψ | No Degradation In Output Power Before and After Test | | | |

- (1) Part is internally matched both on input and output.
 (2) Device specifications obtained on a Production Test Fixture.



| | | | |
|------------|---|----|--------------------------------------|
| C1 | 1.8 pF, 100B Chip Capacitor | Z1 | 0.874" x 0.087" Microstrip |
| C2 | 0.8 pF, 100B Chip Capacitor | Z2 | 1.094" x 0.087" Microstrip |
| C3 | 1.0 pF, 100B Chip Capacitor | Z3 | 0.257" x 0.633" Microstrip |
| C4, C5 | 1.2 pF, 100B Chip Capacitors | Z4 | 0.189" x 0.394" Microstrip |
| C6, C7, C8 | 8.2 pF, 100B Chip Capacitors | Z5 | 0.335" x 0.394" Microstrip |
| C9 | 0.3 pF, 100B Chip Capacitor | Z6 | 0.484" x 0.087" Microstrip |
| C10 | 220 μ F, 63 V Electrolytic Capacitor | Z7 | 0.877" x 0.087" Microstrip |
| R1 | 1.0 k Ω , 1/8 W Chip Resistor (0805) | Z8 | 0.366" x 0.087" Microstrip |
| R2, R3 | 10 k Ω , 1/8 W Chip Resistors (0805) | Z9 | \approx 0.600" x 0.087" Microstrip |

Figure 1. 1805 - 1880 MHz Test Fixture Schematic

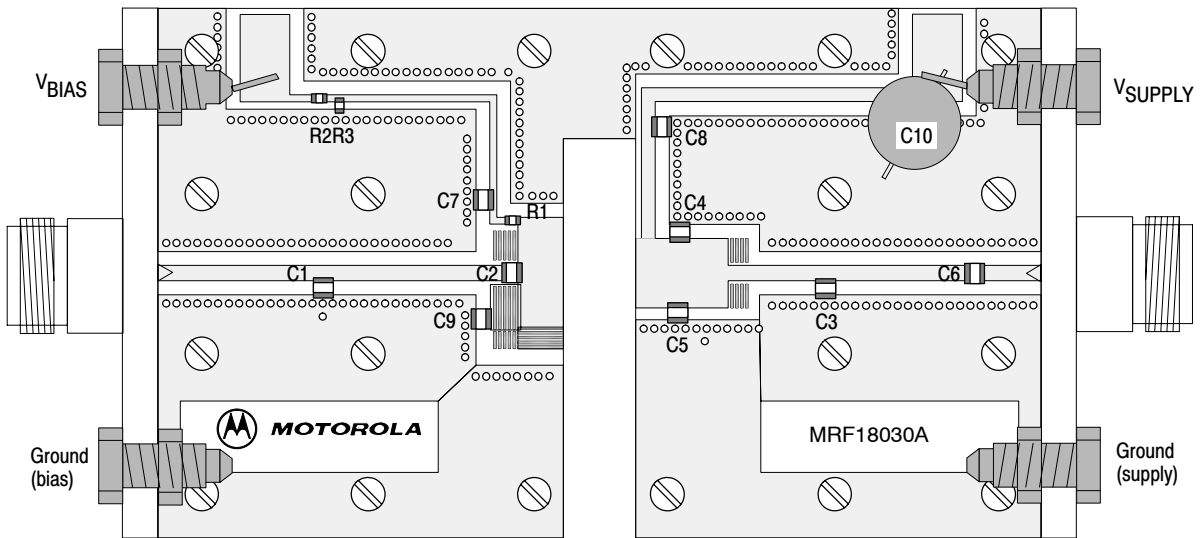


Figure 2. 1805 - 1880 MHz Test Fixture Component Layout

TYPICAL CHARACTERISTICS

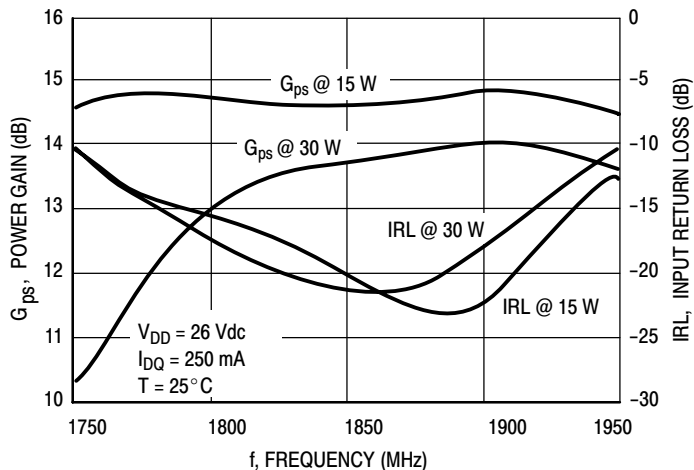


Figure 3. Wideband Gain and IRL at 30 W and 15 W Output Power

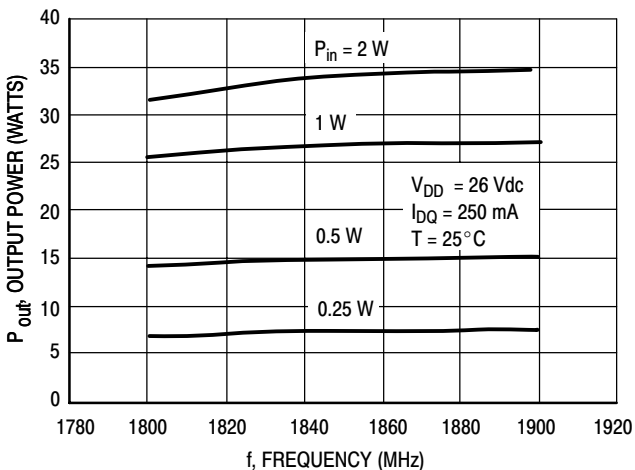


Figure 4. Output Power versus Frequency

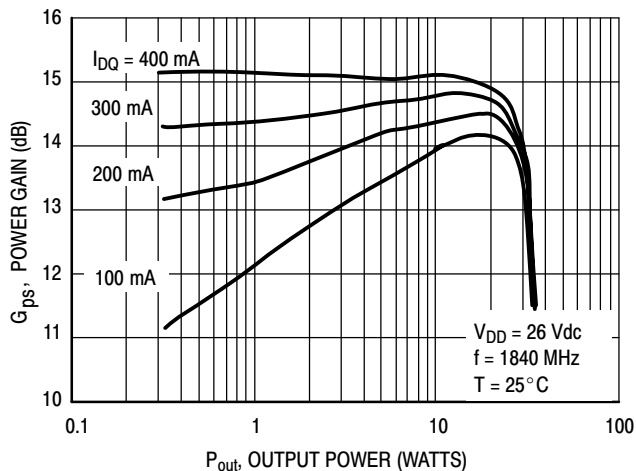


Figure 5. Power Gain versus Output Power

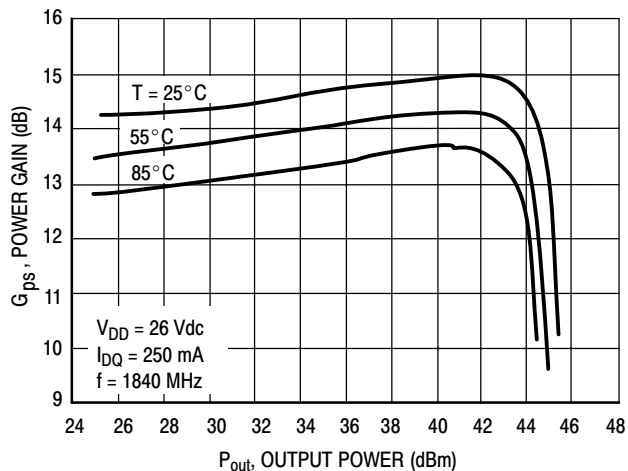


Figure 6. Power Gain versus Output Power

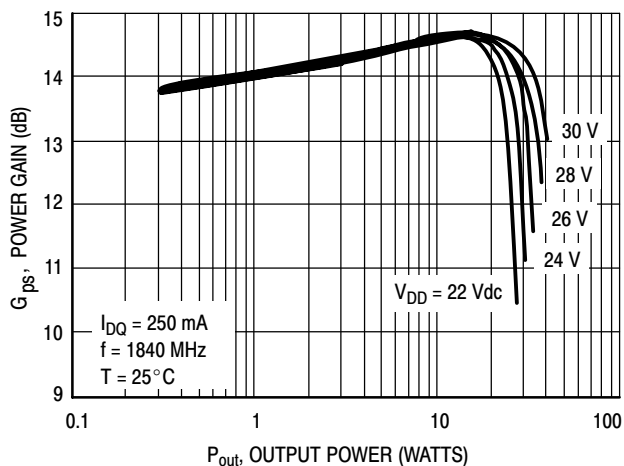


Figure 7. Power Gain versus Output Power

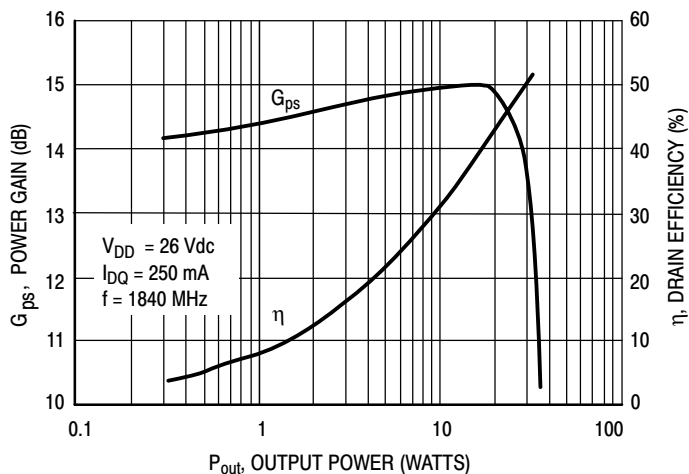
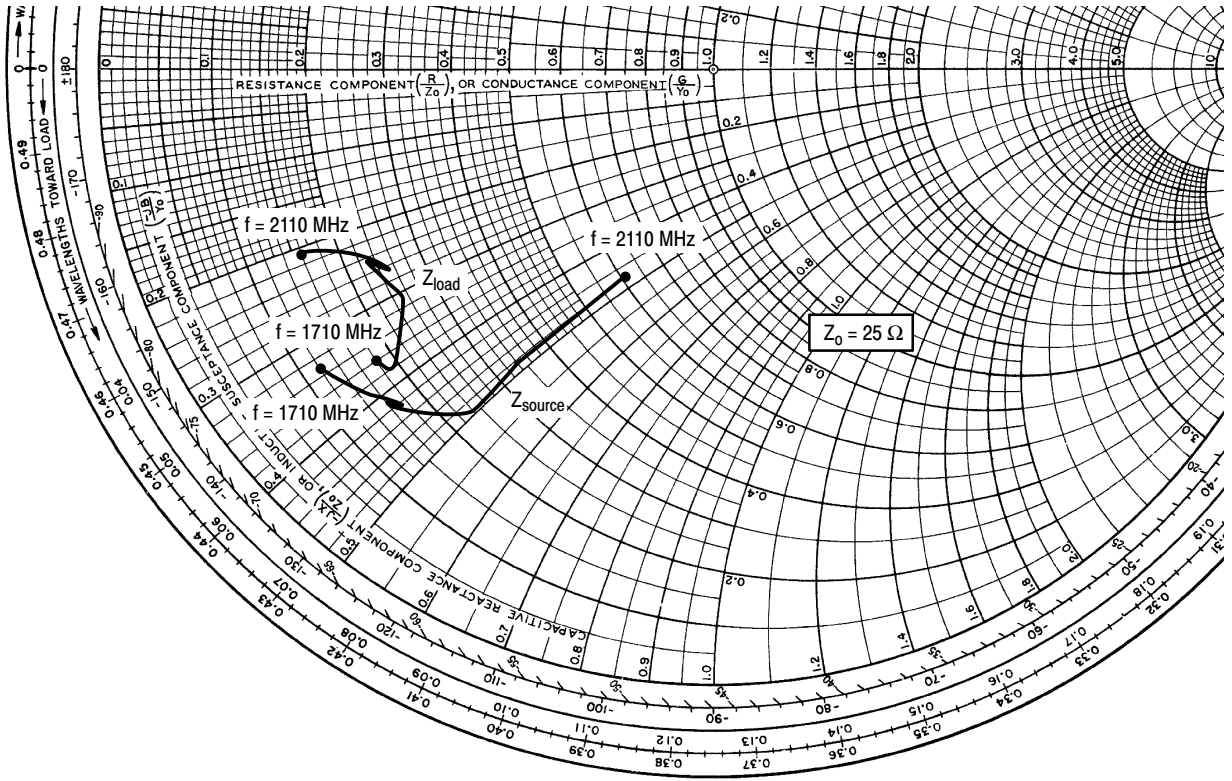


Figure 8. Power Gain and Efficiency versus Output Power



$V_{DD} = 26\text{ V}$, $I_{DQ} = 250\text{ mA}$, $P_{out} = 30\text{ W (CW)}$

| f MHz | Z_{source} Ω | Z_{load} Ω |
|----------|--------------------------|------------------------|
| 1710 | 2.92 - j8.24 | 4.18 - j9.06 |
| 1785 | 3.84 - j9.75 | 4.59 - j9.46 |
| 1805 | 4.15 - j10.38 | 4.98 - j9.06 |
| 1840 | 4.04 - j10.22 | 6.10 - j7.63 |
| 1880 | 6.12 - j12.29 | 5.83 - j6.89 |
| 1960 | 6.20 - j12.29 | 5.55 - j6.33 |
| 1990 | 8.61 - j12.10 | 5.93 - j6.66 |
| 2110 | 15.19 - j11.85 | 3.82 - j5.33 |

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

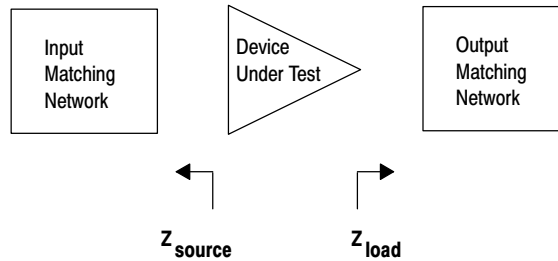


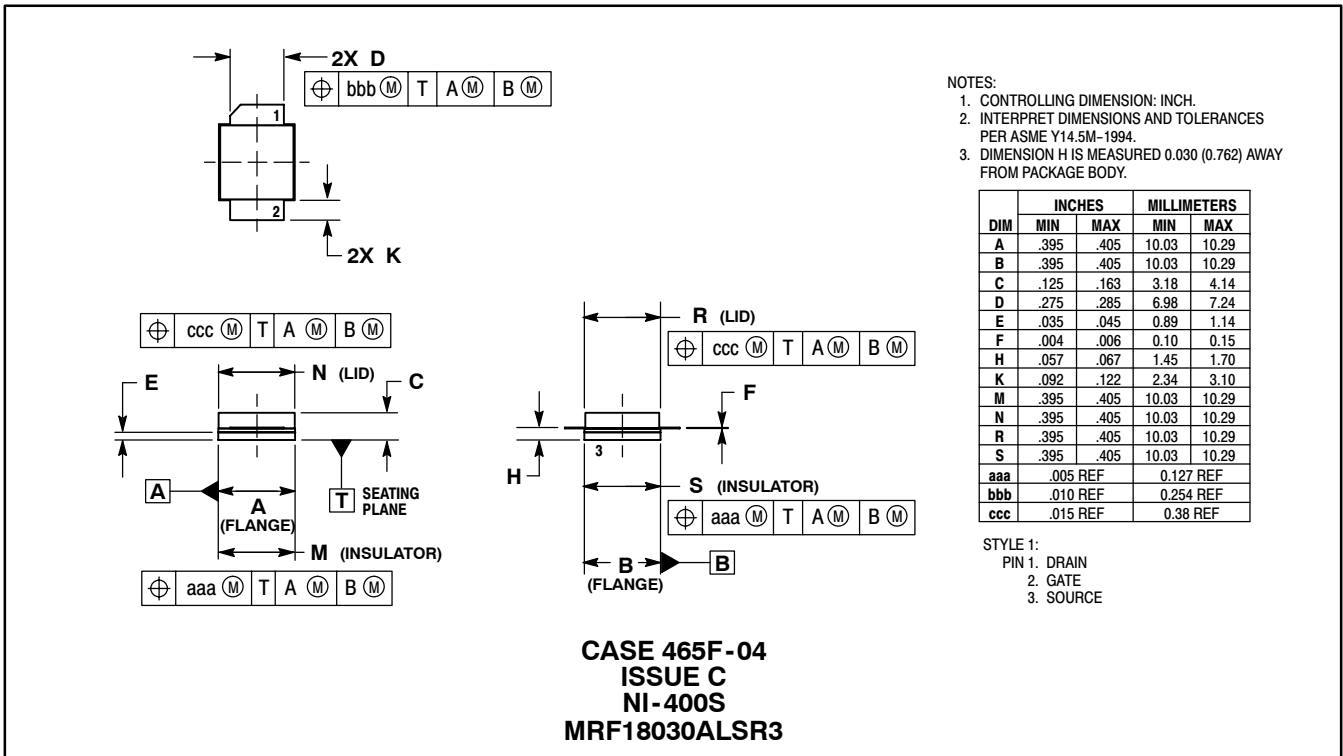
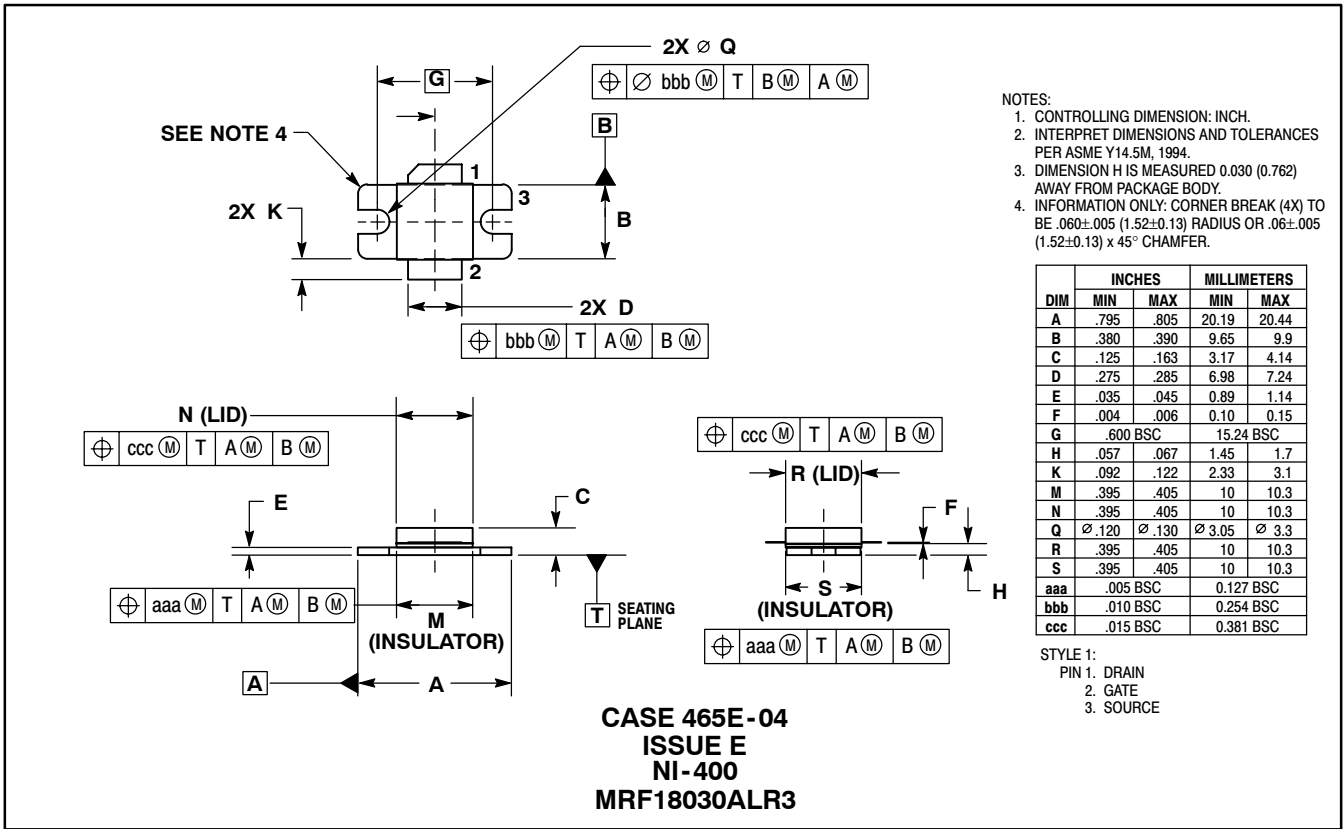
Figure 9. Series Equivalent Source and Load Impedance

NOTES

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PACKAGE DIMENSIONS

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