Wireless Components

PLL-Frequency Synthesizer

PMB 2304R Version 2.1

Specification June 2002

preliminary

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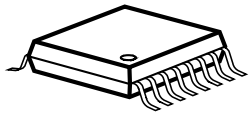
Productinfo

General Description

The PMB 2304R PLL is a high speed CMOS IC, especially designed for use in battery powered radio equipment and mobile telephones and serves as a functional replacement of the PMB 2307R. The primary applications are in digital cellular and cordless systems e.g. GSM 900/1800/1900 and DECT systems. The wide range of dividing ratios also allows application in analog systems.

Package:



Features

- Low operating current consumption (typically 3.5 mA)
- High input sensitivity, high input frequencies (220 MHz)
- Extremely fast phase detector without dead zone
- Linearization of the phase detector output by current sources
- Synchronous programming of the counters (N-, N/A-, R-counters) and system parameters
- Fast modulus switchover for 65-MHz operation
- Switchable modulus trigger edge
- Serial control (3-wire bus: data, clock, enable) for fast programming (f_{max} ~ 10 MHz)
- Large dividing ratios for small channel spacing
  A counter 0 to 127
  N counter 3 to 16.383
  R counter 3 to 65.535
- Serial control (3-wire bus: data, clock, enable) for fast programming (f_{max} ~ 10 MHz)
- Switchable polarity and phase detector current programmable
- 2 Multifunction outputs
  f_{rn}, f_{vn} outputs of the R- and N/A- counters for test
- Output port
  (e.g. for standby of the prescaler)
- External current setting for PD output
- Lock detect output with quasidigital lock detect

Application

- GSM 900 / 1800 / 1900
- DECT
- Analog systems

Ordering Information

Type	Ordering Code	Package
PMB 2304R	Q67106-H9100	P-TSSOP-16

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2 Product Description

Contents of this Chapter

2.1 Overview

The PMB 2304R PLL is a high speed CMOS IC, especially designed for use in battery powered radio equipment and mobile telephones and serves as a functional replacement of the PMB 2307R. The primary applications are in digital cellular and cordless systems e.g. GSM 900/1800/1900 and DECT systems. The wide range of dividing ratios also allows application in analog systems.

2.2 Features

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- High input sensitivity, high input frequencies (220 MHz)
- Extremely fast phase detector without dead zone
- Linearization of the phase detector output by current sources
- Synchronous programming of the counters (N-, N/A-, R-counters) and system parameters
- Fast modulus switchover for 65-MHz operation
- Switchable modulus trigger edge
- Serial control (3-wire bus: data, clock, enable) for fast programming (f_{max} ~ 10 MHz)
- Large dividing ratios for small channel spacing
  A counter 0 to 127
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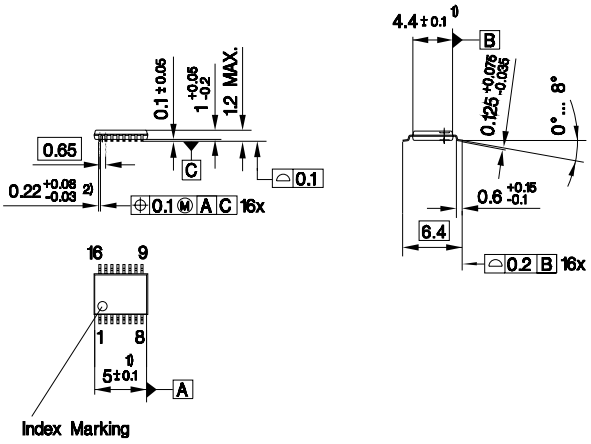
- Output port (e.g. for standby of the prescaler)
- External current setting for PD output
- Lock detect output with quasidigital lock detect

2.3 Application

- GSM 900 / 1800 / 1900
- DECT
- Analog systems

2.4 Package Outlines

P-TSSOP-16

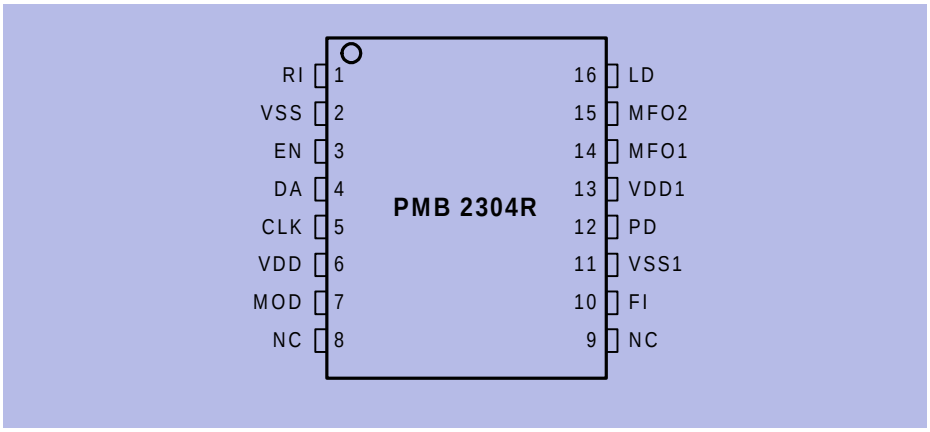


1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

3 Functional Description

Contents of this Chapter

3.1 Pin Configuration

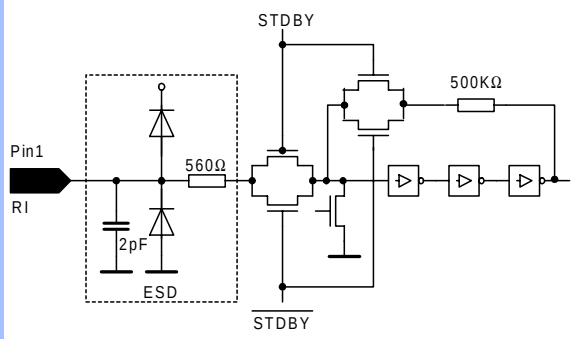


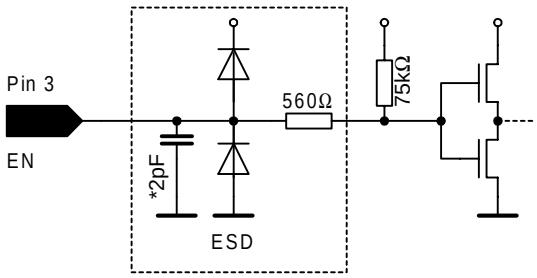
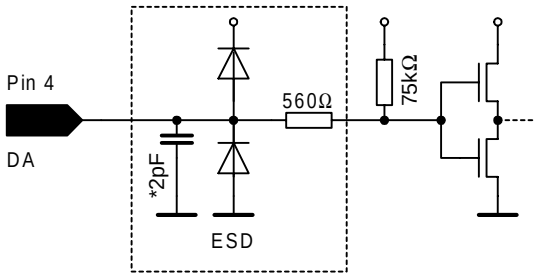
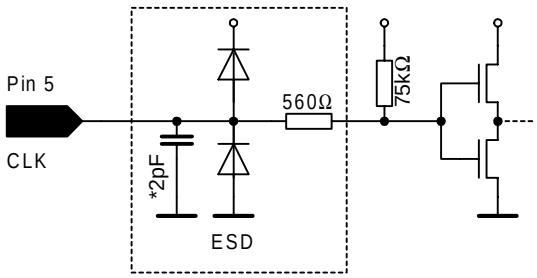
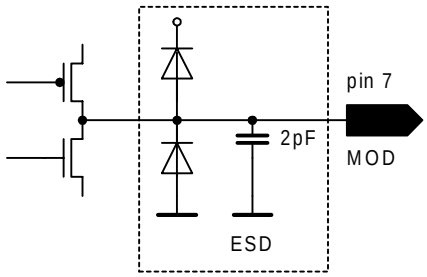
Pin_config.wmf

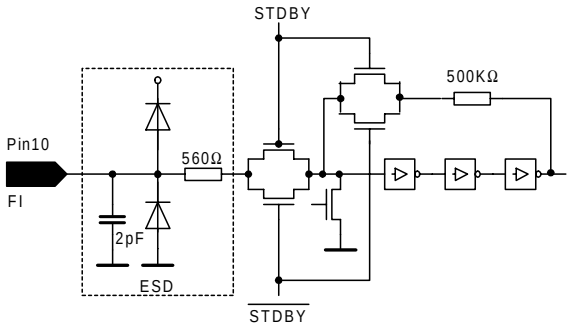
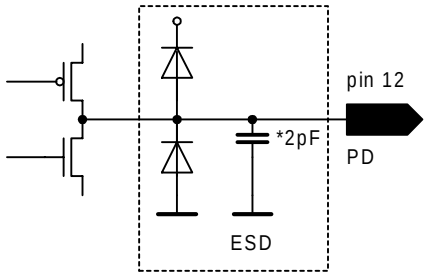
Figure 3-1 Pin Configuration

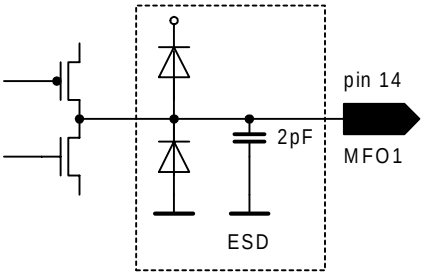
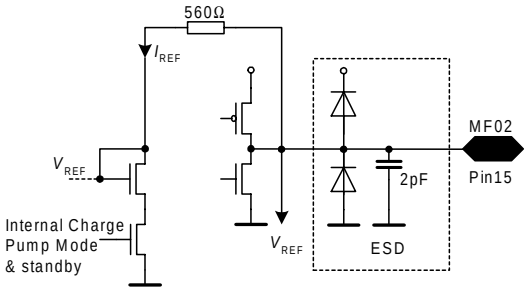
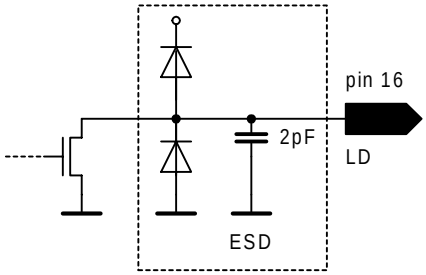
3.2 Pin Definition and Function

Table 3-1 Pin Definition and Function

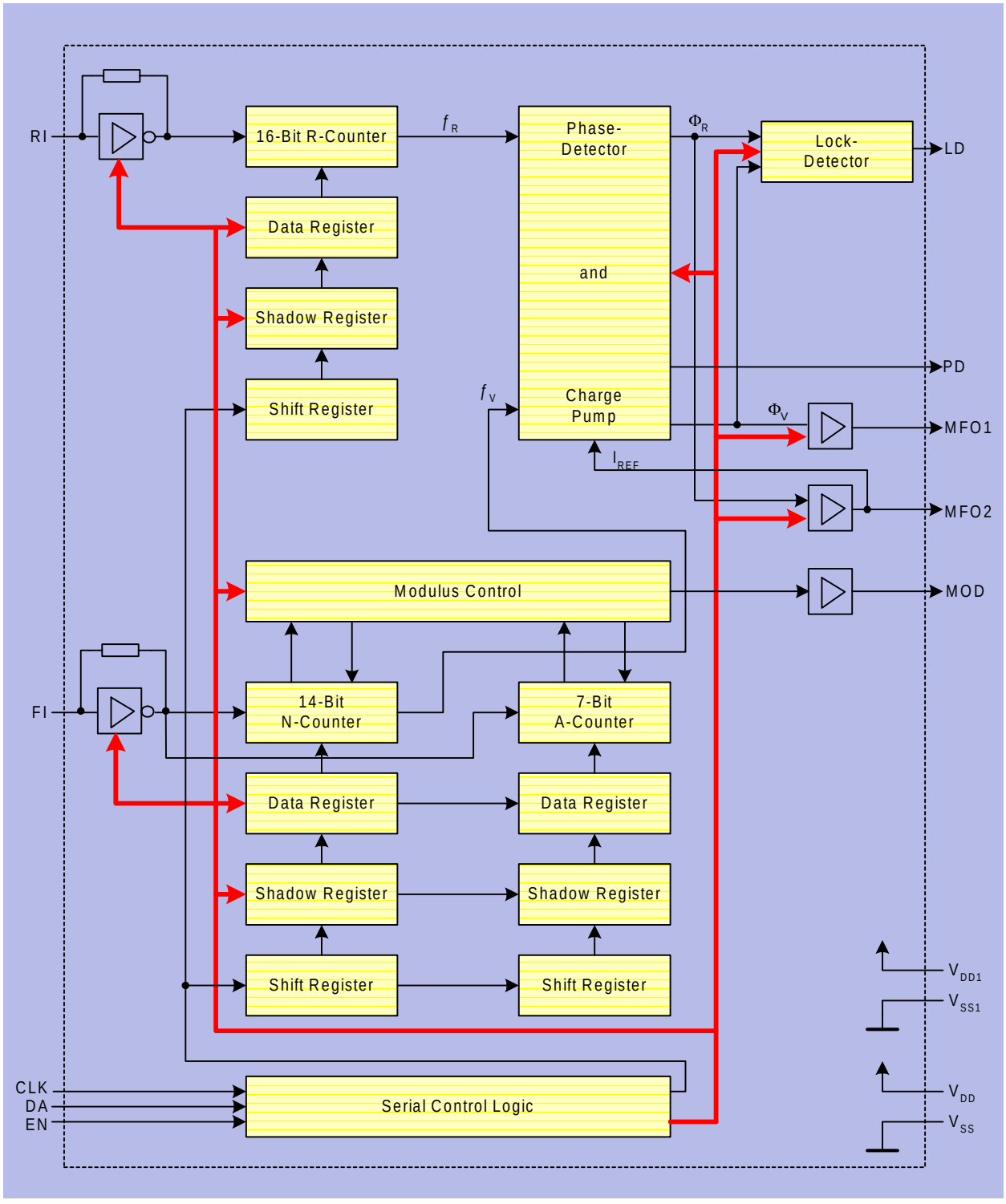
Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	RI		**Reference Frequency** Input with highly sensitive preamplifier for 16-bit R-counter. With small input signals AC coupling must be set up, where DC coupling can be used for large input signals.
2	V_{SS}		Ground for serial control logic.

3	EN		**3-Line Bus: Enable** Enable line of the serial control with internal pull-up resistor. When EN = H the input signals CLK and DA are disabled internally. When EN = L the serial control is activated. The received data are transferred into the latches with the positive edge of the EN-signal.
4	DA		**3-Line Bus: Data** Serial data input with internal pull-up resistor. The last two bits before the EN-signal define the destination address. In a byte-oriented data structure the transmitted data have to end with the EN-signal, i.e. bits to be filled in (don't care) are transmitted first.
5	CLK		**3-Line Bus: Clock** Clock line with internal pull-up resistor. The serial data are read into the internal shift register with the positive edge (see pulse diagram for serial data control).
6	V_{DD}		Positive supply voltage for serial control logic.
7	MOD		**Modulus Control Output** for external dual modulus prescaler. The modulus output is low at the beginning of the cycle. When the A-counter has reached its set value, MOD switches to high. When the N-counter has reached its set value, MOD switches to low again, and the cycle starts from the top. When the prescaler has the counter factor P or P + 1 (P for MOD = H, P +1 for MOD = L), the overall divider factor is NP + A. The value of the A-counter must be smaller than that of the N-counter. The trigger edge of the modulus signal to the input signal can be selected (see programming tables and MODA, B) according to the needs of the prescaler. In single modulus operation and for standby operation in dual modulus operation, the output is low.

8	NC		not connected
9	NC		not connected
10	FI		**VCO-Frequency** Input with highly sensitive preamplifier for 14-bit N-counter and 7-bit A-counter. With small input signals AC coupling must be set up, where DC coupling can be used for large input signals.
11	V_{SS1}		Ground for the preamplifiers, counters, phase detector and charge pump. (**Note: The pins V_{DD} and V_{DD1} respectively V_{SS} and V_{SS1} have to have the same supply voltage**.)
12	PD	 * Only this pin has limited build-in ESD protection	**Phase Detector** Tristate charge pump output. The integrated, positive and negative current sources can be programmed with respect to their current density by means of the serial control. Activation and deactivation depend on the phase relationship of the scaled-down input signals FI:N, RI:R. (See phase detector output waveforms.) frequency$f_V < f_R$ or f_V lagging:p-channel current source active frequency$f_V > f_R$ or f_R leading:n-channel current source active frequency$f_V = f_R$ and PLL locked:current sources are switched off, PD-output is tristate In standby mode the PD-output is set to tristate. The assignment of the current sources to the output signals of the phase detector can be swapped in it's polarity, i.e. the sign of the phase detector constant can be controlled.
13	V_{DD1}		Positive supply voltage for the preamplifiers, counters, phase detector and charge pump.

14	MFO1		**Multifunction Output** for the signals f_{RN}, $\Phi_{V,}$, Φ_{VN}, and port1. –The signal f_{RN} is the divided signal of the reference frequency. The L-time corresponds to $1/f_{RI}$ respectively –In the port function the port 1 output signal is assigned to the information of the programmed status. The output switches with the rising edge of the EN-signal The standby mode does not affect the port function.
15	MFO2		**Multifunction I/O-Pin** for the external reference current setting I_{REF} and the signals Φ_{RN} and f_{VN} (in testmode). –The signal f_{VN} is the divided signal of FI-input. The L-time corresponds to $1/f_{FI}$ respectively. Output levels are not specified, the signal should only be used for test purpose. –In the internal charge pump mode the reference current I_{REF} at MFO2 determines the value of the PD-output current.
16	LD		**Lock Detector Output** (open drain). Unipolar output of the phase detector in the form of a pulse-width modulated signal. The LD-pulse width corresponds to the phase difference. In the locked state the LD-signal is at H-level. For standby mode see Standby Table. Only for ABL status 11 no gating of ABL impulse is performed.

3.3 Functional Block Diagram



Funct_block.wmf

Figure 3-2 Functional Block Diagram

3.4 General Description

The circuit consists of a reference-, A- and N-counter, a dual modulus control logic, a phase detector with charge pump output and a serial control logic. The setting of the operating mode and the selection of the counter ratios is done serially at the ports CLK, DA and EN.

The operating modes allow the selection of single or dual operation, asynchronous or synchronous data acquisition, 4 different antibacklash-impulse times, 8 different PD-output current modes, polarity setting of the PD-output signal, adjustment of the trigger-edge of the MOD-output signal, 2 standby modes and the control of the multifunction outputs MFO1 and MFO2.

The reference frequency is applied at the RI-input and divided by the R-counter. It's maximum value is 100 MHz. The VCO-frequency is applied at the FI-input and divided by the N- or N/A-counter according to single or dual mode operation. The maximum value at FI is 220 MHz at single-, and 65 MHz at dual mode operation.

The phase and frequency sensitive phase detector produces an output signal with adjustable anti-backlash impulses in order to prevent a dead zone for very small phase deviations. Phase differences of less than 100 ps can be resolved. In general the shortest anti-backlash pulse gives the best system performance.

3.5 Programming

Programming of the IC is done by a serial data control. The contents of the message are assigned to the functional units according to the address. Single or dual mode operation as well as asynchronous or synchronous data acquisition is set by status 2 and should therefore precede the programming of the counters.

3.6 Data acquisition

The PMB 2304R offers the possibility of synchronous data acquisition to avoid error signals at the phase detector due to non-corresponding dividing factors in the counters produced by asynchronous loading.

Synchronous programming guarantees control during changes of frequency or channel. That means that the state of the phase detector or the phase difference is kept maintained, and in case of "lock in", the control process starts with the phase difference "zero".

This is done as follows:

1. Setting of synchronous data acquisition by status 2.
2. Programming of the R-counter, status 1 (optional)-data is being loaded into shadow registers.
3. Programming of the N- or N/A-counter-data is being loaded into shadow registers, the EN-signal starts the synchronous loading procedure.
4. Synchronous programming – which means data transfer of all data from the shadow registers to the data registers – takes place at that point in time when the respective counter reaches “zero + 1”, the maximum repetition rate for channel change is therefore f_{FI}:N.
5. Transfer of status 1 information into the corresponding data register is tied to the N-counter loading, but follows the loading of the N-data register in the distance of one N-counter dividing ratio, this guarantees that for example a new PD-current value becomes valid at the same time when the counters are loaded with the new data.

Synchronous avoids additional phase error caused by programming. Synchronous data acquisition is of especial advantage, when large steps in frequency are to be made in a short time. For this purpose a high reference frequency can be programmed in order to achieve rapid – “rough” – transient response. This method increases the fundamental frequency nearly by the square route of the reference frequency relation. When rough lock is achieved, another synchronous data transfer is needed to switch back to the original channel spacing. A “fine” lock in will finish the total step response. It may not be necessary to change reference frequency, but it make sense to perform synchronous data acquisition in any case. Especially for GSM, PCN, PCS, DECT, DAMPS, PHP systems the synchronous mode should be used to get best performance of the PMB 2304R.

Standby Condition:

The PMB 2304R has two standby modes (standby 1, 2) to reduce the current consumption.

Standby 1 switches off the whole circuit, the current consumption is reduced below 1 µA.

Standby 2 switches off the counters, the charge pump and the outputs, only the preamplifiers stay active.

For the influence on the output signals **see standby table (5-10).**

f_{RN}, f_{VN}, Φ_{RN}, Φ_{VN} are the inverted signals of f_R, f_V,Φ_R, Φ_V.

4 Applications

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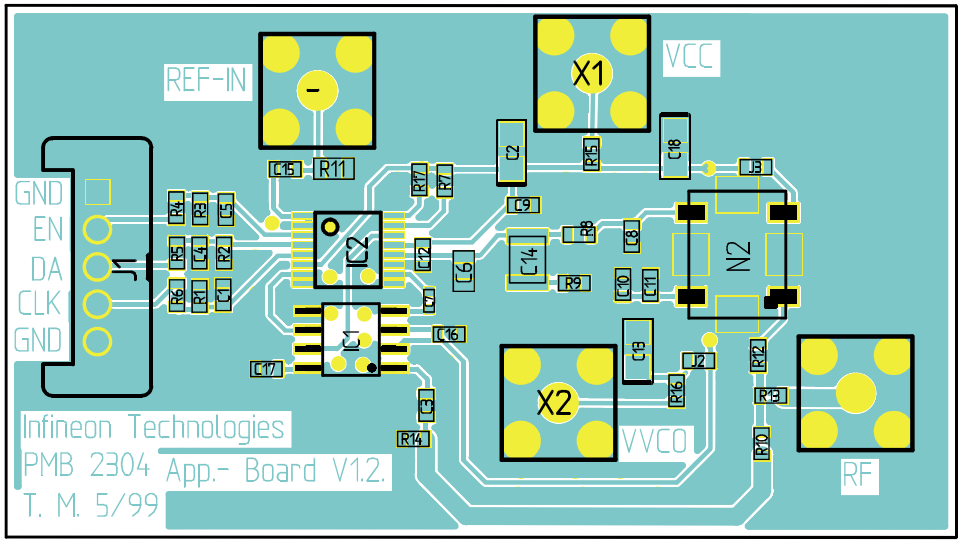
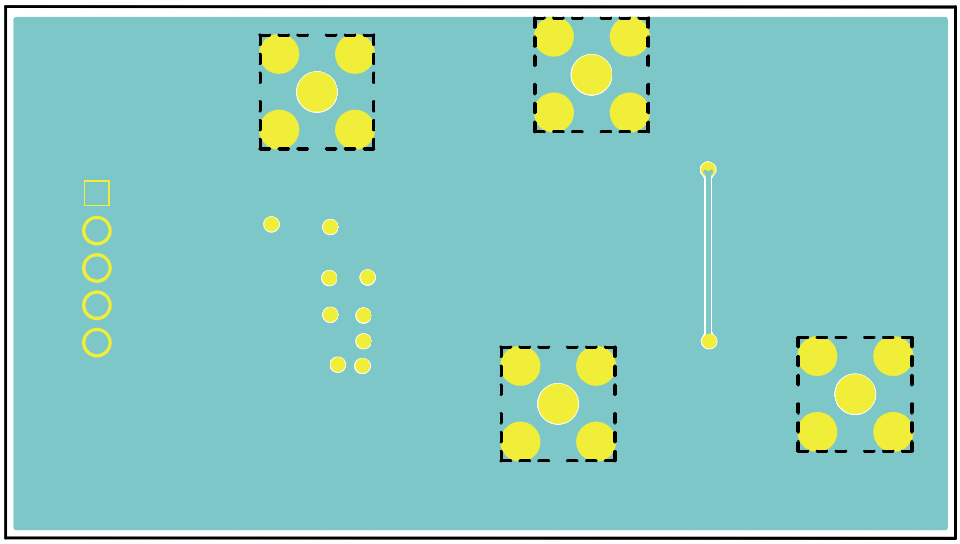
4.1 PCB Layout



oben.wmf

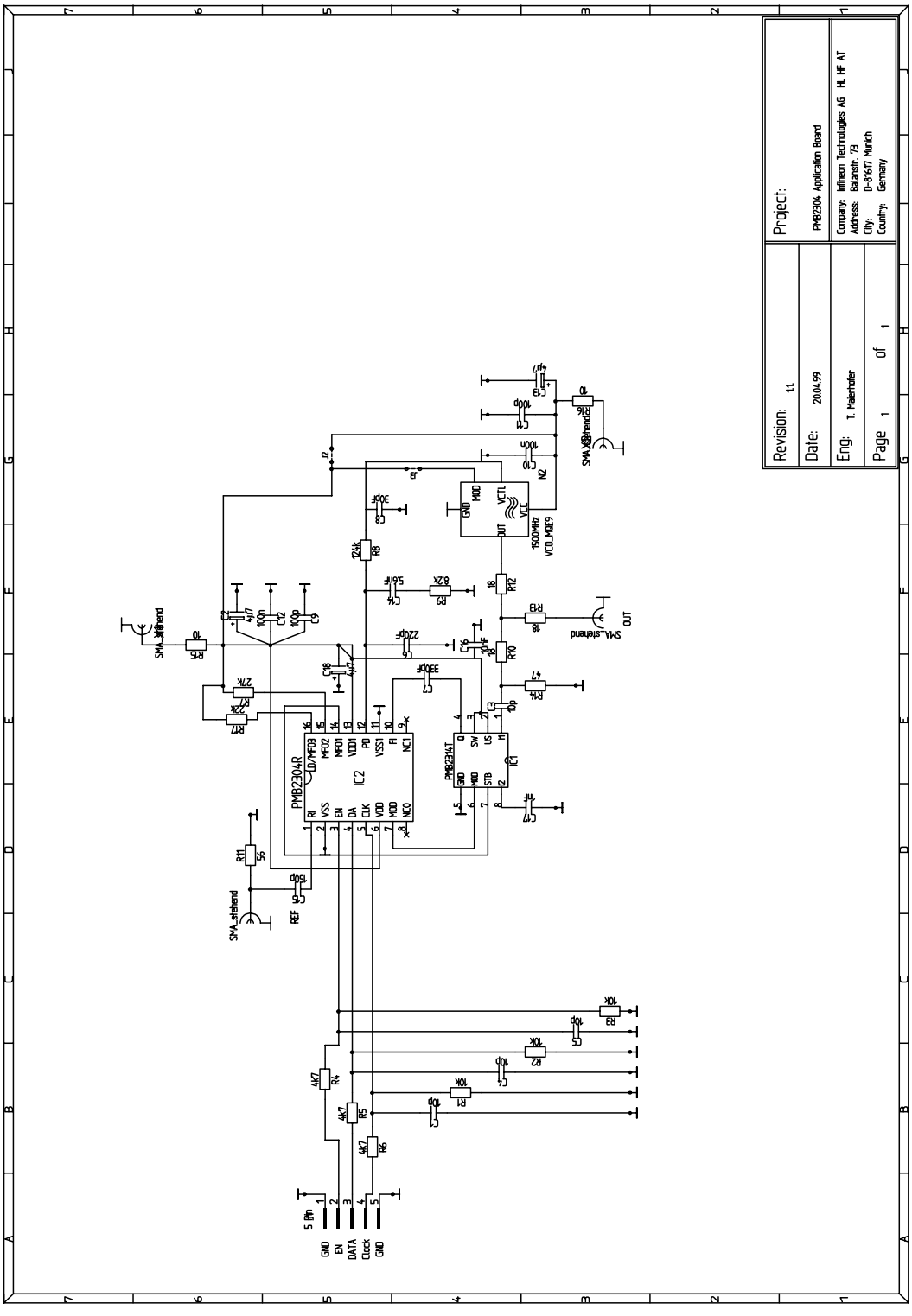
Figure 4-1 Top Side



unten.wmf

Figure 4-2 Bottom Side

4.2 Application Board



stromlauf.wmf

Figure 4-3 Application board

4.3 Bill of material

Table 4-1

Nr	Reference	Symbol name	Technology
1	C1	CAP	10p
2	C2	CAPELK	4µ7
3	C3	CAP	10p
4	C4	CAP	10p
5	C5	CAP	10p
6	C6	CAP	220pF
7	C7	CAP	330pF
8	C8	CAP	30pF
9	C9	CAP	100p
10	C10	CAP	100n
11	C11	CAP	100p
12	C12	CAP	100n
13	C13	CAPELK	4µ7
14	C14	CAP	5.6nF
15	C15	CAP	150p
16	C16	CAP	10nF
17	C17	CAP	1nF
18	C18	CAPELK	4µ7
19	IC1	PMB2314T	PMB2314T
20	IC2	PMB2305	PMB2304R
21	J1	CON-5	5 Pin
22	J2	JUMP-2SMD0603	JUMPER_2SMD06031
23	J3	JUMP-2SMD0603	JUMPER_2SMD06031
24	N2	VCO2	1500MHz
25	R1	RES	10k
26	R2	RES	10k
27	R3	RES	10k
28	R4	RES	4k7
29	R5	RES	4k7
30	R6	RES	4k7
31	R7	RES	27k
32	R8	RES	124k

33	R9	RES	8.2k
34	R10	RES	18
35	R11	RES	56
36	R12	RES	18
37	R13	RES	18
38	R14	RES	47
39	R15	RES	10
40	R16	RES	10
41	R17	RES	22k
42		SMA	SMA_stehend
43	-	SMA	SMA_stehend
44	X1	SMA	SMA_stehend
45	X2	SMA	SMA_stehend

5 Reference

Contents of this Chapter

5.1 Electrical Data

5.1.1 Absolute Maximum Range

WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Table 5-1 Absolute Maximum Range

Parameter	Symbol	Limit Values min	Limit Values max	Unit	Remarks
Supply Voltage	V_{DD}	-0.3	6	V	
Input Voltage	V_I	-0.3	V_{DD} + 0.3	V	
Output Voltage	V_Q	GND	V_{DD}	V	
Power dissipation per output	P_Q		10	mW	
Total power dissipation	P_{tot}		300	mW	
Ambient temperature	T_A	-40	85	°C	in operation
Storage temperature	T_{stg}	-50	125	°C	
Thermal Resistance	R_{thJA}		180	K/W	
ESD Integrity except @Pin 12 (PD) (according to MIL833 Method 3015.7)	V_{ESD}		1	KV	
ESD Integrity except @Pin 12 (PD) (according to MIL833 Method 3015.7)	V_{ESD}		400	V	

5.1.2 Operating Ratings

Within the operating ratings the IC operates as described in the circuit description. The AC/DC characteristic limits are not guaranteed.

Table 5-2 Operating Ratings, Supply Voltage V_{VCC}= 2.7 V .. 4.5 V, Ambient temp. T_{AMB}= -30°C ... + 85°C

Parameter	Symbol	Limit Values		Unit	Test Conditions	L	Item
		min	max				
Supply Voltage	V_{DD}	2.7	5.5	V			
Input frequency dual	f_{FI}	0.1	65	MHz	V_{DD} = 4.5...5.5V		
Input frequency single HF-mode	f_{FI}	0.1	220	MHz	V_{DD} = 4.5...5.5V		
Input frequency single LF-mode	f_{FI}	0.1	90	MHz	V_{DD} = 4.5...5.5V		
Input reference frequency	f_{RI}		100	MHz	V_{DD} = 4.5...5.5V		
Input frequency dual mode	f_{FI}	0.1	30	MHz	V_{DD} = 2.7V		
Input frequency single HF-mode	f_{FI}	0.1	90	MHz	V_{DD} = 2.7V		
Input frequency single LF-mode	f_{FI}	0.1	35	MHz	V_{DD} = 2.7V		
Input reference frequency	f_{RI}		20	MHz	V_{DD} = 2.7V		
PD-output current	/ I_{PD}		4	mA			
PD-output voltage	V_{PD}	0.5	V_{DD} - 0.5	V	V_{DD} = 4.5- 5.5V		
PD-output voltage	VPD	0.5	V_{DD} - 0.5	c	V_{DD} = 2.7V		
Ambient temperature	T_A	-40	85	°C			

5.1.3 Typical Supply Current I_{DD}

All pins are protected against ESD. Unused inputs without pullup resistors must be connected to either V_{DD} or V_{SS}.

Table 5-3 Typical Supply Current I_{DD}

Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min		max				
Supply voltage	V_{DD}	2.7	5	5.5	V			
Supply current:						f_{FI} = 50MHz		
single mode HF	I_{DD}	1.63	2.6	2.94	mA	V_{FI} = 150mVrms		
dual mode	I_{DD}	1.76	2.80	3.17	mA	f_{RI} = 10MHz		
standby 2	I_{DD}	0.11	0.62	0.75	mA	V_{RI} = 150mVrms		
standby 1	I_{DD}			1	µA	I_{PD} = 0.25mA I_{ref} = 100 µA		

5.1.4 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Table 5-4 AC/DC Characteristics with Ambient temp. T_{amb}= -20 .. 85 °C, Supply Voltage V_{VCC} = 2.7 .. 4.5V

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Input Signals DA, CLK, EN (with internal pull-up resistors)								
H-input voltage	V_{IH}	0.7- V_{DD}		V_{DD}	V			1.1
L-input voltage	V_{IL}			0.3- V_{DD}	V			1.2
Input capacity	C_I			5	pF			
H-input current	I_H			10	µA	V_I = V_{DD} = 5.5V		1.3
L-input current	I_L	-60			µA	V_I = GND		1.4
Input Signal RI								
Input voltage	V_I	100			mVrms	f = 4...100MHz, V_{DD} = 4.5V		2.1
Input voltage	V_I	100			mVrms	f = 4...30MHz, V_{DD} = 2.7V		2.2
Slew rate		4			V/µs	V_{DD} = 2.7...5.5V		2.3
Input capacity	C_I			3	pF			
H-input current	I_H			30	µA	V_I = V_{DD} = 5.5V		2.4
L-input current	I_L	-30			µA	V_I = GND		2.5
Input Signal FI (dual mode)								
Input voltage	V_I	180			mVrms	f = 4...65MHz, V_{DD} = 4.5V		3.1
Input voltage	V_I	50			mVrms	f = 10...25MHz, V_{DD} = 2.7V		3.2
Slew rate		4			V/µs	V_{DD} = 2.7...5.5V		3.3
Input capacity	C_I			3	pF			
H-input current	I_H			30	µA	V_I = V_{DD} = 5.5V		3.4
L-input current	I_L	-30			µA	V_I = GND		3.5
Input Signal FI (single HF-mode)								
Input voltage	V_I	200			mVrms	f = 4...200MHz, V_{DD} = 4.5V		4.1
Input voltage	V_I	200			mVrms	f = 4...90MHz, V_{DD} = 2.7V		4.2
Input voltage	V_I	50			mVrms	f = 10...40MHz, V_{DD} = 4.5V		4.3
Slew rate		4			V/µs	V_{DD} = 2.7...5.5V		4.4
Input capacity	C_I			3	pF			
H-input current	I_H			30	µA	V_I = V_{DD} = 5.5V		4.5
L-input current	I_L	-30			µA	V_I = GND		4.6

Table 5-4 AC/DC Characteristics with Ambient temp. T_{amb}= -20 .. 85 °C, Supply Voltage V_{VCC} = 2.7 .. 4.5V								
	Symbol	**Limit Values**			Unit	**Test Conditions**	**L**	**Item**
		min	typ	max				
Input Signal FI (single LF-mode)								
Input voltage	V_I	100			mVrms	f = 4...90MHz, V_{DD} = 4.5V		5.1
Input voltage	V_I	100			mVrms	f = 4...35MHz, V_{DD} = 2.7V		5.2
Slew rate		4			V/µs	V_{DD} = 2.7...5.5V		5.3
Input capacity	C_I			3	pF			
H-input current	I_H			30	µA	V_I = V_{DD} = 5.5V		5.4
L-input current	I_L	-30			µA	V_I = GND		5.5
Output Current /I_{PD}/								
Current mode:								6.1
"0.175 mA"	I_{PROG}	-20%	0.175	+20%	mA	V_{DD} = 4.5...5.5V V_{PD} = V_{DD}/2 I_{REF} = 100µA		6.2
"0.25 mA"	I_{PROG}	-20%	0.25	+20%	mA			6.3
"0.35 mA"	I_{PROG}	-20%	0.35	+20%	mA			6.4
"0.5 mA"	I_{PROG}	-20%	0.5	+20%	mA			6.5
"0.7 mA"	I_{PROG}	-20%	0.7	+20%	mA			6.6
"1.0 mA"	I_{PROG}	-15%	1.0	+15%	mA			6.7
"1.4 mA"	I_{PROG}	-15%	1.0	+15%	mA	V_{DD} = 4.5V		6.8
"2.0 mA"	I_{PROG}	-10%	2.0	+10%	mA			6.9
Standby"	/I_{PD}/		0.1	1	nA		■	6.10
Output Tolerance I_{PD}								
ΔI_{PD} / I_{PROG}		-10%	-5%	+0%		V_{PD} = V_{DD}/2, V_{DD} = 2.7V		7.1
ΔI_{PD} / I_{PROG}			±2.5%			V_{PD} = 0.5...2.2V, V_{DD} = 2.7V		7.2
Input Voltage MFO2 (Internal charge pump mode)								
Reference voltage	V_{REF}	0.9	1.1	1.3	V	V_{DD} = 2.7...5.5V I_{REF} = 100µA		8.1
Output Signal MFO1 (push pull)								
H-output voltage	V_{QH}	V_{DD} - 1			V	V_{DD} = 4.5...5.5V,I_{QH}= -2mA		9.1
L-output voltage	V_{QL}			1	V	V_{DD} = 4.5...5.5V,I_{QL}= 2mA		9.2
H-output voltage	V_{QH}	V_{DD} - 1			V	V_{DD} = 2.7V,I_{QH}=-1.2mA		9.3
L-output voltage	V_{QL}			1	V	V_{DD} = 2.7V,I_{QL}=1.2mA		9.4
Rise time	t_R		2.5	10	ns	V_{DD} = 4.5...5.5V,C_I= 10pF		9.5
Fall time	t_F		2.0	10	ns	V_{DD} = 4.5...5.5V,C_I= 10p		9.6
Rise time	t_R		5	12	ns	V_{DD} = 2.7V,C_I=10pF		9.7
Fall time	t_F		4	12	ns	V_{DD} = 2.7V,C_I=10pF		9.8

Table 5-4 AC/DC Characteristics with Ambient temp. T_{amb}= -20 .. 85 °C, Supply Voltage V_{VCC} = 2.7 .. 4.5V								
	Symbol	**Limit Values**			Unit	**Test Conditions**	**L**	**Item**
		min	typ	max				
Output Signal MFO2 (push pull)								
H-output voltage	V_{QH}	V_{DD} - 1			V	V_{DD} = 4.5...5.5V,I_{QH}= 2mA		10.1
L-output voltage	V_{QL}			1	V	V_{DD} = 4.5...5.5V,I_{QL}= 2mA		10.2
H-output voltage	V_{QH}	V_{DD} - 1			V	V_{DD} = 2.7V,I_{QH}= 1.2mA		10.3
L-output voltage	V_{QL}			1	V	V_{DD} = 2.7V,I_{QL}= 1.2mA		10.4
Rise time	t_R		2	10	ns	V_{DD} = 4.5...5.5V,C_l= 10pF		10.5
Fall time	t_F		2	10	ns	V_{DD} = 4.5...5.5V,C_l= 10p		10.6
Rise time	t_R		3	10	ns	V_{DD} = 2.7V,C_l=10pF		10.7
Fall time	t_F		3	10	ns	V_{DD} = 2.7V,C_l=10pF		10.8
Output Signal LD (n-channel open drain)								
L-output voltage	V_{QL}			0.4	V	V_{DD} = 2.7...5.5V, I_{QL} = 0.3mA		11.1
H-output current	I_{QH}			5	µA	V_{DD} = 2.7...5.5V		11.2
Fall time	t_F		3	10	ns	V_{DD} = 4.5...5.5V,C_l=10pF		11.3
Fall time	t_F		5	12	ns	V_{DD} = 2.7V,C_l=10pF		11.4
Output Signal MOD (push pull)								
H-output voltage	V_{QH}	V_{DD}-0.4			V	V_{DD} = 4.5...5.5V, I_{QH} = -0.5mA		12.1
L-output voltage	V_{QL}			0.4	V	V_{DD} = 4.5...5.5V I_{QL} = 0.5mA		12.2
H-output voltage	V_{QH}	V_{DD}-0.4			V	V_{DD} = 2.7V, I_{QH} = - 0.3mA		12.3
L-output voltage	V_{QL}			0.4	V	V_{DD} = 2.7V, I_{QL}= 0.3mA		12.4
Rise time	t_R		1.5	3	ns	V_{DD} = 4.5...5.5V, C_l = 5pF		12.5
Fall time	t_F		1.3	3	ns	V_{DD} = 4.5...5.5V, C_l = 5pF		12.6
Propagation delay time H-L to FI	t_{DQHL}		8	12	ns	V_{DD} = 4.5...5.5V, C_l = 5pF		12.7
Propagation delay time L-H to FI	t_{DQHL}		8	12	ns	V_{DD} = 4.5...5.5V, C_l = 5pF		12.8
Rise time	t_R		3.2	5	ns	V_{DD} = 2.7V, C_l = 5pF		12.9
Fall time	t_F		2	5	ns	V_{DD} = 2.7V, C_l = 5pF		12.10
Propagation delay time H-L to FI	t_{DQHL}		15		ns	V_{DD} = 2.7V, C_l = 5pF		12.11
Propagation delay time L-H to FI	t_{DQHL}		15		ns	V_{DD} = 2.7V, C_l = 5pF		12.12

■ This value is only guaranteed in lab.

5.2 Phase detector outputs

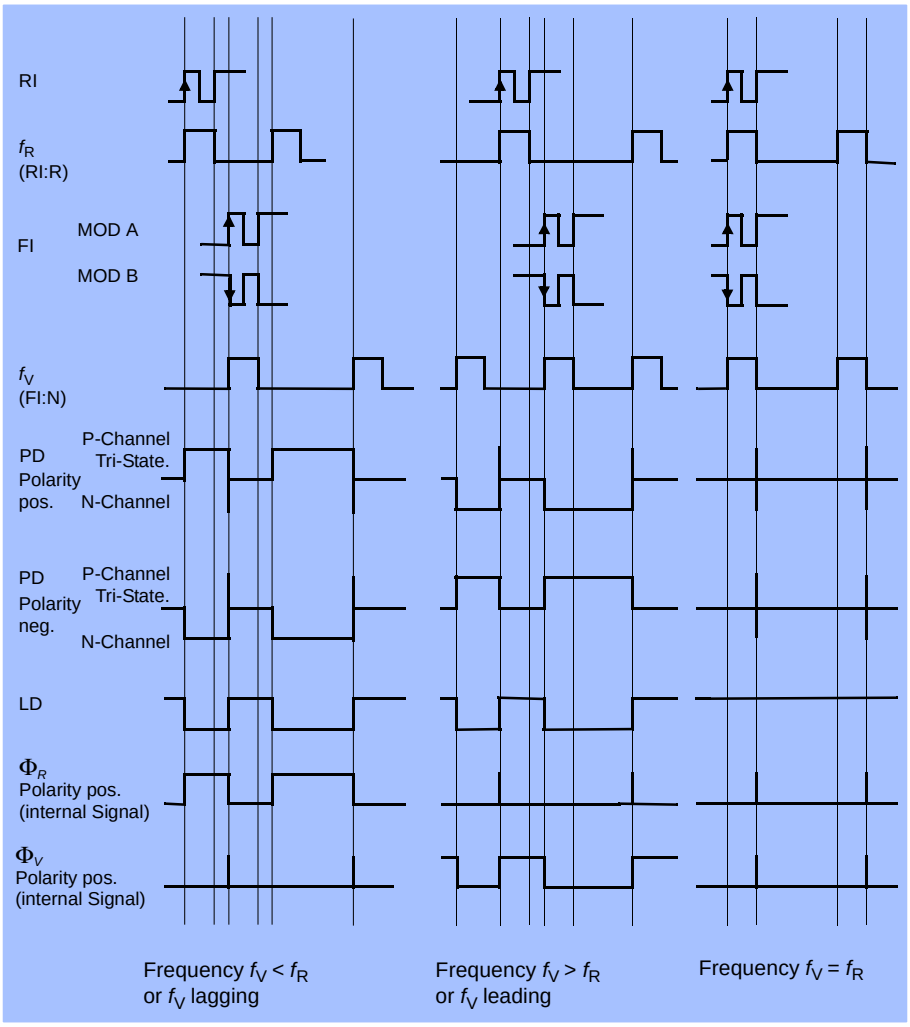


Figure 5-1 Phase detector output signals

5.3 Serial Control Data Format

Table 5-5 Serial Control Data Format (status 1,2)

Status 1		Status 2		
			0	1
	Data acquisition mode	1	asynchronous	synchronous
	Mode 1	2	see table	
	Mode 2	3	see table	
	PD-polarity	4	negative	positive
	Standby 1	5	standby	active
	Standby 2	6	standby	active
	Anti-backlash pulse width 1	7	see table	
	Anti-backlash pulse width 2	8	see table	
	Preamplifier select	9	see table	
	Single / dual mode	10	single	dual
1	Port 1	11	low	high
2	PD-current 1	12	see table	
3	PD-current 2	13	see table	
4	PD-current 3	14	see table	
5	0 Address 0	15		
6	0 1	16		
EN		EN		

Table 5-6 Serial Control Data Format (N-, N/A-counter)

Dual Mode				Single Mode
1	MSB	A-Counter		
2				
3				
4				
5				
6				
7	LSB			
8	MSB	N-Counter	MSB	1
9				2
10				3
11				4
12				5
13				6
14				7
15				8
16				9
17				10
18				11
19				12
20				13
21	LSB		LSB	14
22	1	Address	1	15
23	0		0	16
EN				EN

Table 5-7 Serial Control Data Format (R-counter)

1	MSB	R-Counter	
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16	LSB		
17	1	Address	
18	1		
EN			

5.4 Programming Tables

Table 5-8

Status Bits

Anti-Backlash Pulse Width 2	Anti-Backlash Pulse Width 1	t_W (typ.) [ns]	
0	0	1.3	V_{DD} = 5V
0	1	5	
1	0	10	not recommended
1	1	13*	any application where continuous lock detect is required

* No ABL gating performed
* In general the shortest anti-backlash pulse gives the best system performance

.

Table 5-9

Status Bits		Preamplifier Function Mode
Single/Dual Mode	Preamplifier Select	
0	0	FI-input frequency,single HF-mode
0	1	FI-input frequency,single LF-mode
1	0	FI-input frequency, dual-mode, FI-trigger edge LH, MOD A
1	1	FI-input frequency, dual-mode, FI-trigger edge HL, MOD B

Table 5-10 Standby Table

	Output Pins					
Status	MFO1		MFO2	LD	PD	MOD
	Φ_V	Φ_{VN}				
Standby 1	low	high	high	resistive	tristate	low
Standby 2	low	high	high	resistive	tristate	low

Table 5-11			
Status Bits			**PD-Current Mode**
PD-Current 3	**PD-Current 2**	**PD-Current 1**	**Ipd/mA**
0	0	0	0.175
0	0	1	0.25
0	1	0	0.35
0	1	1	0.5
1	0	0	0.7
1	0	1	1
1	1	0	1.4
1	1	1	2

Table 5-12				
Status Bits		**Multifunction Output**		
Mode 2	**Mode 1**	**MFO 1**	**MFO 2**	**Remarks**
0	0	f_{RN}	f_{VN}	test mode
0	1	Φ_V	Φ_{RN}	external charge pump mode 1
1	0	Φ_{VN}	Φ_{RN}	external charge pump mode 2
1	1	Port 1	I_{ref}	internal charge pump mode

5.5 Pulse Diagram

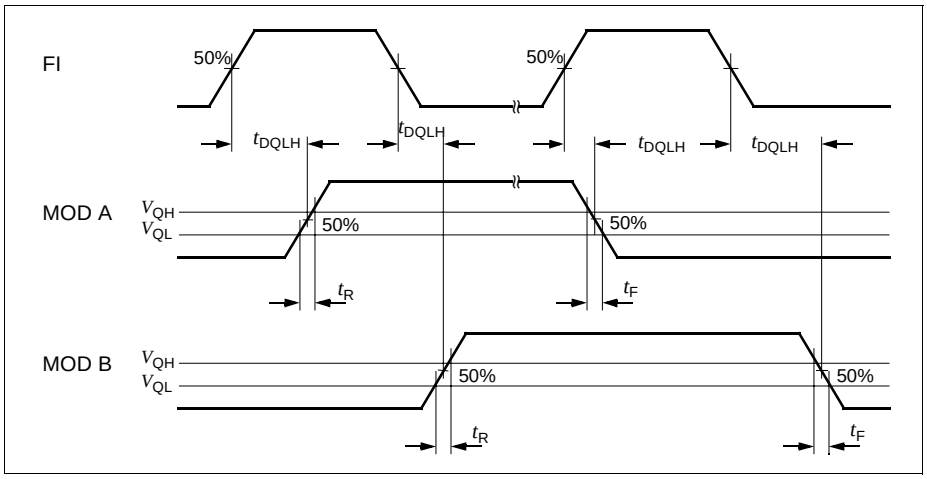


Figure 5-2 Pulse diagram

5.6 Serial Control Data Input Timing

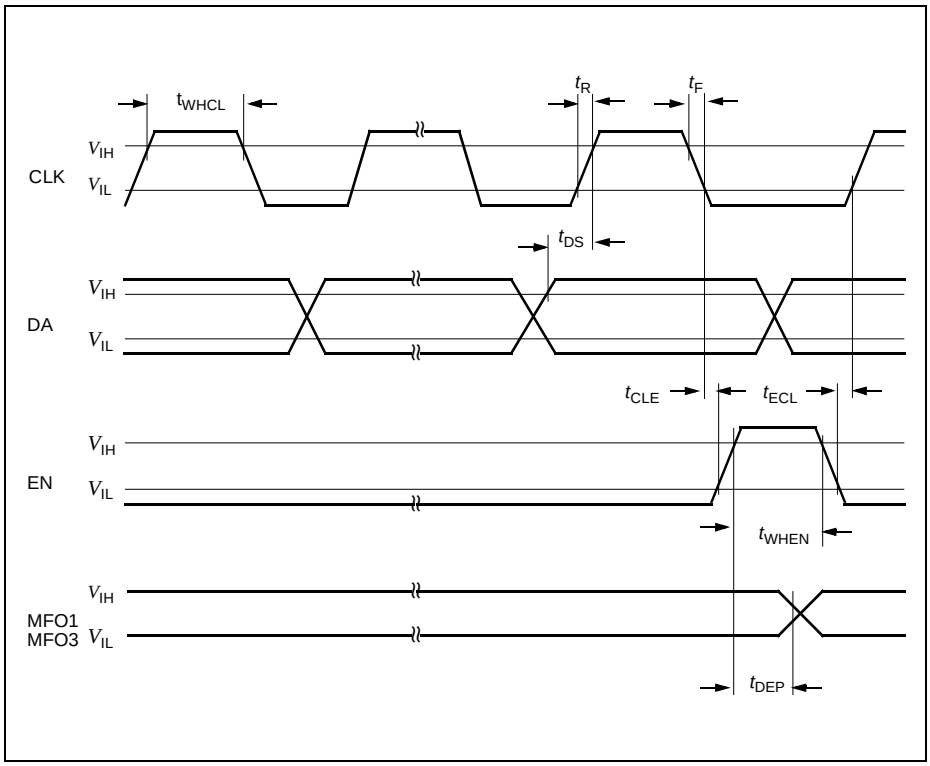


Figure 5-3 Serial Control Data Input Timing

Table 5-13

Parameter	Symbol	Limit Values		Unit
		min	max	
Clock frequency	f_{CL}		12	MHz
H-pulsewidth (CL)	t_{WHCL}	40		ns
Data setup	t_{DS}	20		ns
Setup time-clock enable	t_{CLE}	20		ns
Setup time enable-clock	t_{ECL}	20		ns
H-pulsewidth (enable)	t_{WHEN}	40		ns
Rise, fall time	t_R, t_F		10	µs
Propagation delay time EN-PORT	t_{DEP}		1	µs

5.7 Diagram Input Sensitivity FI

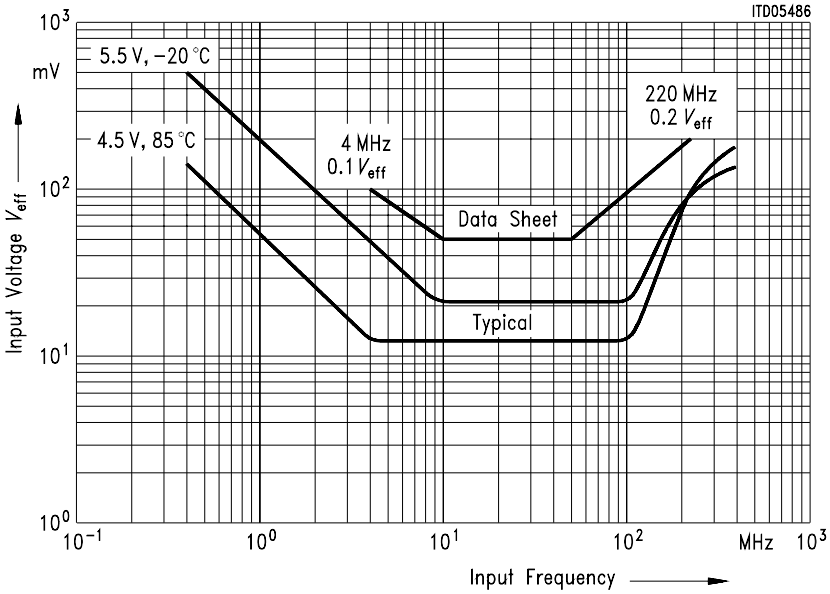


Figure 5-4 Input sensitivity FI (single HF-mode)