

FEATURES

- 2.5ns typical propagation delay
- Low power
- Differential PECL inputs
- 24mA TTL outputs
- Flow-through pinouts
- Available in 8-pin SOIC package

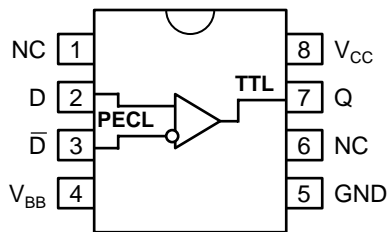
DESCRIPTION

The SY10/100ELT21 are single differential PECL-to-TTL translators. Because PECL (Positive ECL) levels are used, only +5V and ground are required. The small outline 8-lead SOIC package and low skew single gate design make the ELT21 ideal for applications that require the translation of a clock or data signal where minimal space, low power, and low cost are critical.

The V_{BB} output allow differential single-ended, or AC-coupled interface to the device. If used, the V_{BB} output should be bypassed to V_{CC} with a $0.01\mu\text{F}$ capacitor.

The ELT21 is available in both ECL standards: the 10ELT is compatible with positive ECL 10H logic levels, while the 100ELT is compatible with positive ECL 100K logic levels.

PIN CONFIGURATION/BLOCK DIAGRAM



**SOIC
TOP VIEW**

PIN NAMES

Pin	Function
Q	TTL Output
D, /D	Differential PECL Inputs
V_{CC}	+5.0V Supply
V_{BB}	Reference Output
GND	Ground

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{CC}	Power Supply Voltage	-0.5 to +7.0	V
V _I	PECL Input Voltage	0V to V _{CC} +0.5	V
V _O	Voltage Applied to Output at HIGH State	-0.5 to +5.5	V
I _O	Current Applied to Output at LOW State	Twice the Rated I _{OL}	mA
T _{store}	Storage Temperature	-65 to +150	°C
T _A	Operating Temperature	-40 to +85	°C

TRUTH TABLE

D	/D	Q
L	H	L
H	L	H
Open	Open	L

NOTE:

- Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TTL DC ELECTRICAL CHARACTERISTICSV_{CC} = 4.75V to 5.25V

Symbol	Parameter	T _A = -40°C		T _A = 0°C		T _A = +25°C			T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
I _{OS}	Output Short Circuit Current	-80	-200	-80	-200	-80	—	-200	-80	-200	mA	V _{OUT} = 0V
I _{CC}	Power Supply Current	—	20	—	20	—	14	20	—	20	mA	—
V _{OH}	Output HIGH Voltage	2.5	—	2.5	—	2.5	—	—	2.5	—	V	I _{OH} = -3.0mA I _{OH} = -15mA
		2.0	—	2.0	—	2.0	—	—	2.0	—	V	
V _{OL}	Output LOW Voltage	—	0.5	—	0.5	—	—	0.5	—	0.5	V	I _{OL} = 24mA

PECL DC ELECTRICAL CHARACTERISTICSV_{CC} = 4.75V to 5.25V

Symbol	Parameter	T _A = -40°C		T _A = 0°C		T _A = +25°C			T _A = +85°C		Unit	Condition	
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
I _{IH}	Input HIGH Current	—	150	—	150	—	—	150	—	150	μA		
I _{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	—	0.5	—	μA		
V _{IH}	Input HIGH Voltage ⁽²⁾	10ELT	3770	4110	3830	4160	3870	—	4190	3940	4280	mV	
		100ELT	3835	4120	3835	4120	3835	—	4120	3835	4120		
V _{IL}	Input LOW Voltage ⁽²⁾	10ELT	3050	3500	3050	3520	3050	—	3520	3050	3555	mV	
		100ELT	3190	3525	3190	3525	3190	—	3525	3190	3525		
V _{BB}	Reference Output ⁽²⁾	10ELT	3570	3700	3620	3730	3650	—	3750	3690	3810	mV	
		100ELT	3620	3740	3620	3740	3620	—	3740	3620	3740		

NOTES:

- These values are for V_{CC} = 5.0V. Level Specifications will vary 1:1 V_{CC}.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 4.75V$ to $5.25V$

Symbol	Parameter	TA = -40°C		TA = 0°C		TA = +25°C			TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Output Q	2.0	3.0	2.0	3.0	2.0	—	3.0	2.0	3.0	ns	$C_L = 50pF$
t_{skpp}	Part-to-Part Skew ^(1, 2)	—	0.5	—	0.5	—	—	0.5	—	0.5	ns	$C_L = 50pF$
f_{MAX}	Maximum Input Frequency (2, 3, 4)	160	—	160	—	160	—	—	160	—	MHz	$C_L = 50pF$
V_{CMR}	Common Mode Range	2.4	V_{CC}	2.4	V_{CC}	2.4	—	V_{CC}	2.4	V_{CC}	V	
V_{PP}	Minimum Peak-to-Peak Input ⁽⁵⁾	200	—	200	—	200	—	—	200	—	mV	
t_r t_f	Output Rise/Fall Time (1.0V to 2.0V)	—	1.5	—	1.5	—	—	1.5	—	1.5	ns	$C_L = 50pF$

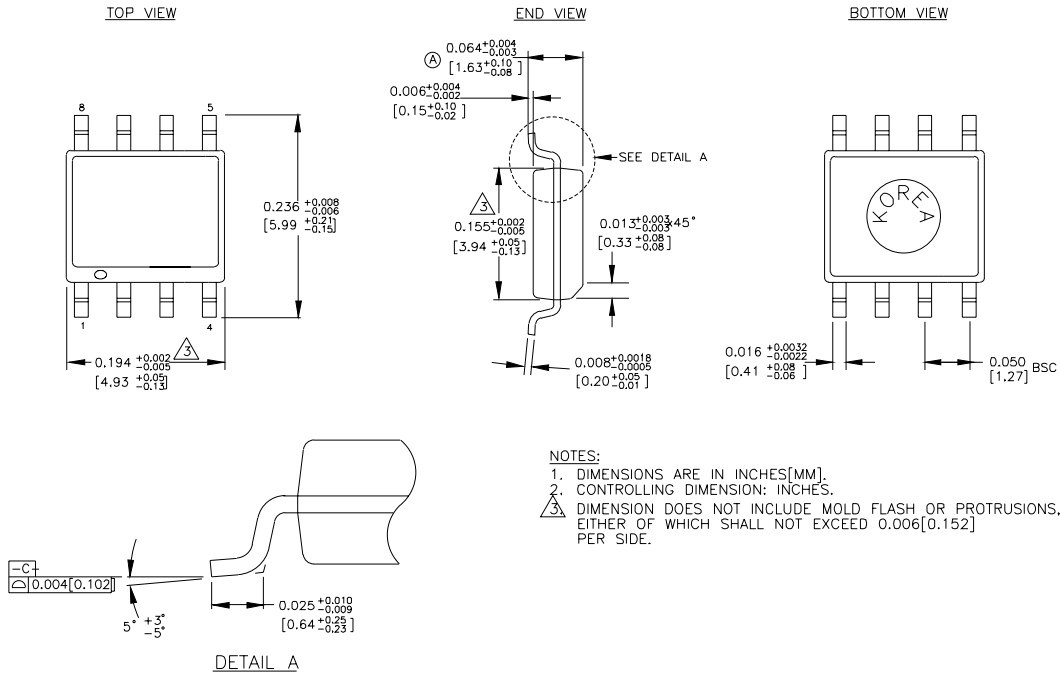
NOTES:

1. Part-to-Part Skew considering HIGH-to-HIGH transitions at common V_{CC} levels.
2. These parameters are guaranteed, but not tested.
3. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
4. The f_{MAX} value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.
5. 200mV input guarantees full logic at output.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	Vcc Range (V)
SY10ELT21ZC	Z8-1	Commercial	+4.75 to +5.25
SY10ELT21ZCTR	Z8-1	Commercial	+4.75 to +5.25
SY100ELT21ZC	Z8-1	Commercial	+4.75 to +5.25
SY100ELT21ZCTR	Z8-1	Commercial	+4.75 to +5.25

8 LEAD SOIC .150" WIDE (Z8-1)



Rev. 03

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