SONY

CXD3511Q

Digital Signal Driver/Timing Generator

Description

The CXD3511Q incorporates digital signal processor type RGB driver, color shading correction, selectable delay line and timing generator functions onto a single IC. Operation is possible with a system clock up to 200 [MHz] (max.). This IC can process video signals in bands up to UXGA standard, and can output the timing signals for driving various Sony LCD panels such as SXGA and XGA.

Features

- Various picture quality adjustment functions such as user adjustment, white balance adjustment and gamma correction
- OSD MIX, black frame processing, mute and limiter functions
- LCD panel color shading correction function
- Selectable delay line
- Drives various Sony data projector LCD panels such as SXGA and XGA
- Controls the CXA3512R and CXA3562R sample-and-hold drivers
- Line inversion and field inversion signal generation
- Supports AC drive of LCD panels during no signal

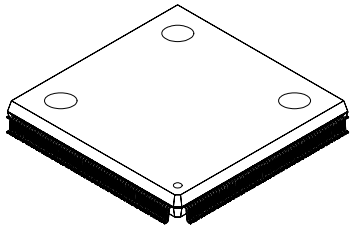
Applications

LCD projectors and other video equipment

Structure

Silicon gate CMOS IC

240 pin QFP (Plastic)



Absolute Maximum Ratings (V_{SS} = 0V)

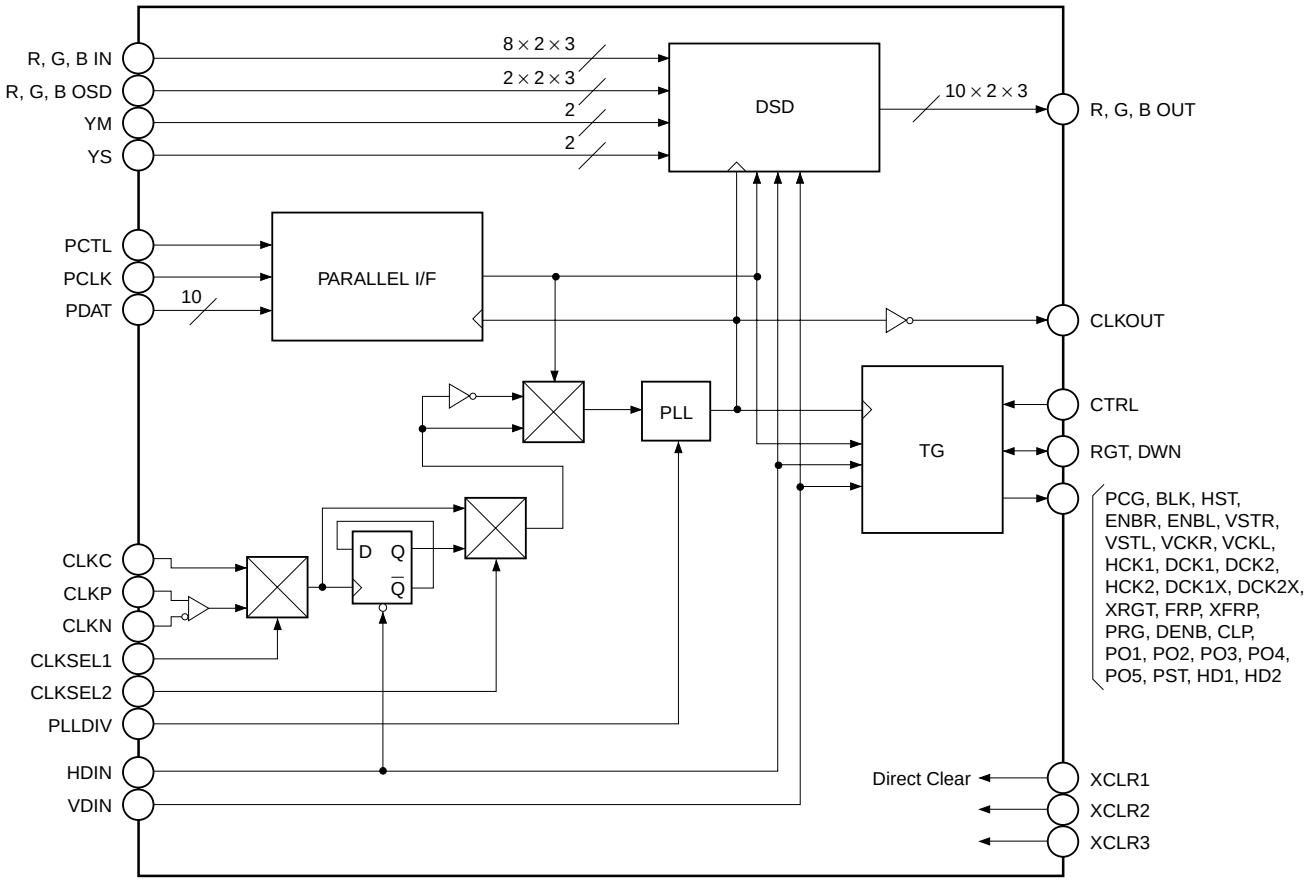
• Supply voltage	V_{DD1}	V_{SS} – 0.5 to +3.0	V
	V_{DD2}	V_{SS} – 0.5 to +4.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD1} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD1} + 0.5	V
• Storage temperature	Tstg	–55 to +125	°C
• Junction temperature	Tj	125	°C

Recommended Operating Conditions

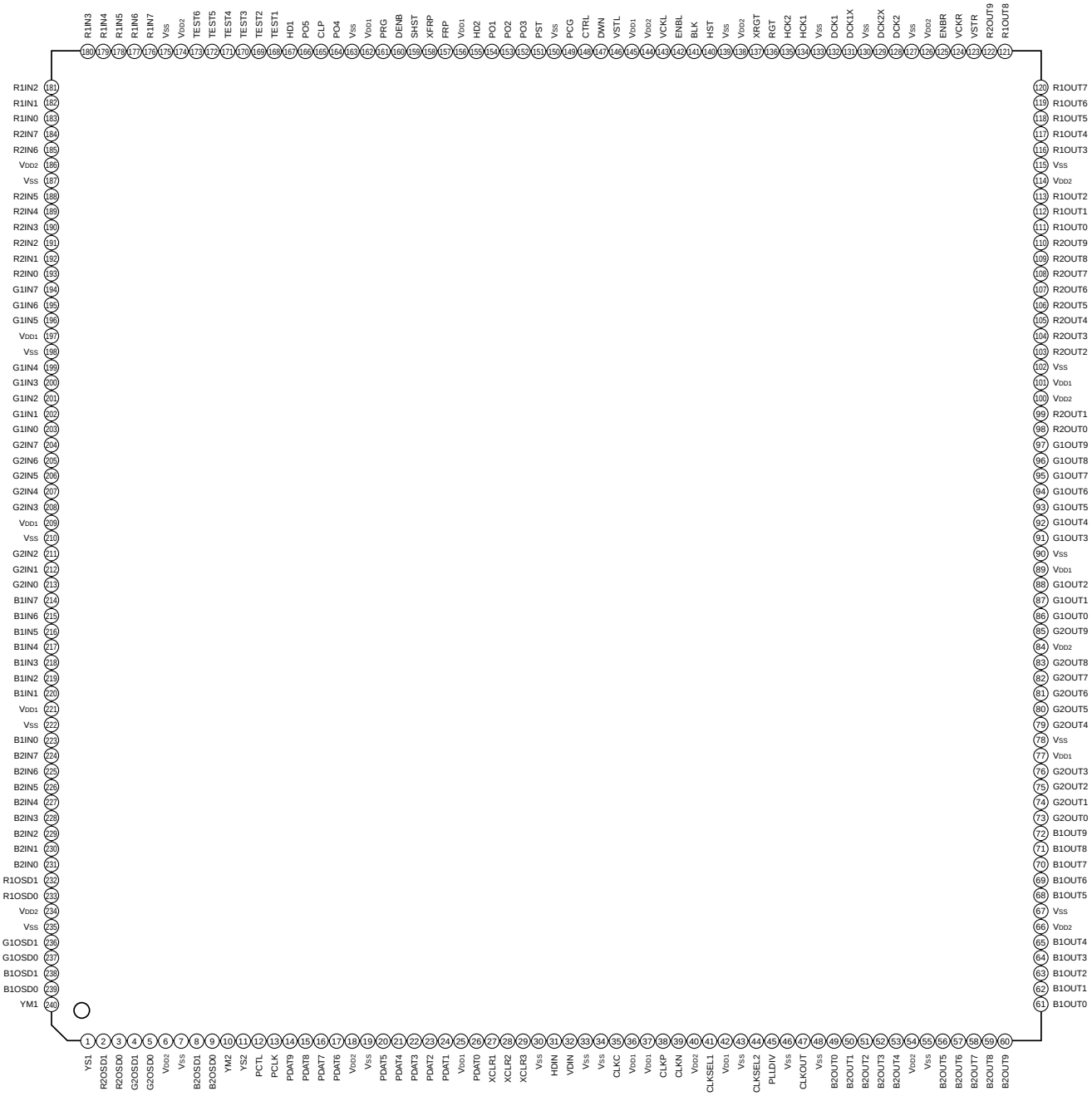
• Supply voltage	V_{DD1}	2.3 to 2.7	V
	V_{DD2}	3.0 to 3.6	V
• Operating temperature	Topr	–20 to +75	°C

E00Y06-PS

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description	Input pin processing for open status
1	YS1	I	OSD YS input (port 1)	L
2	R2OSD1	I	OSD Red data input (port 2)	—
3	R2OSD0	I	OSD Red data input (port 2)	—
4	G2OSD1	I	OSD Green data input (port 2)	—
5	G2OSD0	I	OSD Green data input (port 2)	—
6	V_{DD2}	—	I/O power supply	—
7	V_{SS}	—	GND	—
8	B2OSD1	I	OSD Blue data input (port 2)	—
9	B2OSD0	I	OSD Blue data input (port 2)	—
10	YM2	I	OSD YM input (port 2)	L
11	YS2	I	OSD YS input (port 2)	L
12	PCTL	I	Parallel I/F control signal input	H
13	PCLK	I	Parallel I/F clock input	—
14	PDAT9	I	Parallel I/F data input	—
15	PDAT8	I	Parallel I/F data input	—
16	PDAT7	I	Parallel I/F data input	—
17	PDAT6	I	Parallel I/F data input	—
18	V_{DD2}	—	I/O power supply	
19	V_{SS}	—	GND	—
20	PDAT5	I	Parallel I/F data input	—
21	PDAT4	I	Parallel I/F data input	—
22	PDAT3	I	Parallel I/F data input	—
23	PDAT2	I	Parallel I/F data input	—
24	PDAT1	I	Parallel I/F data input	—
25	V_{DD1}	—	Internal operation power supply	—
26	PDAT0	I	Parallel I/F data input	—
27	XCLR1	I	External clear (Low: reset)	H
28	XCLR2	I	External clear (Low: reset)	H
29	XCLR3	I	External clear (Low: reset)	H
30	V_{SS}	—	GND	—
31	HDIN	I	Horizontal sync signal input	—
32	VDIN	I	Vertical sync signal input	—
33	V_{SS}	—	GND	—
34	V_{SS}	—	GND	—
35	CLKC	I	Clock input (CMOS input)	—
36	V_{DD1}	—	Internal operation power supply	—
37	V_{DD1}	—	Internal operation power supply	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
38	CLKP	I	Clock input (small-amplitude differential input, positive polarity)	—
39	CLKN	I	Clock input (small-amplitude differential input, negative polarity)	—
40	V_{DD2}	—	I/O power supply	—
41	CLKSEL1	I	Input clock selection. (High: CLKC, Low: CLKP, CLKN)	L
42	V_{DD1}	—	Internal operation power supply	—
43	V_{SS}	—	GND	—
44	CLKSEL2	I	Internal clock path selection. (High: no frequency division, Low: frequency division)	L
45	PLLDIV	I	Internal PLL setting. (High: 55MHz or less, Low: 55MHz or more)	L
46	V_{SS}	—	GND	—
47	CLKOUT	O	Internal clock output (inverted output)	—
48	V_{SS}	—	GND	—
49	B2OUT0	O	Blue data output (port 2)	—
50	B2OUT1	O	Blue data output (port 2)	—
51	B2OUT2	O	Blue data output (port 2)	—
52	B2OUT3	O	Blue data output (port 2)	—
53	B2OUT4	O	Blue data output (port 2)	—
54	V_{DD2}	—	I/O power supply	—
55	V_{SS}	—	GND	—
56	B2OUT5	O	Blue data output (port 2)	—
57	B2OUT6	O	Blue data output (port 2)	—
58	B2OUT7	O	Blue data output (port 2)	—
59	B2OUT8	O	Blue data output (port 2)	—
60	B2OUT9	O	Blue data output (port 2)	—
61	B1OUT0	O	Blue data output (port 1)	—
62	B1OUT1	O	Blue data output (port 1)	—
63	B1OUT2	O	Blue data output (port 1)	—
64	B1OUT3	O	Blue data output (port 1)	—
65	B1OUT4	O	Blue data output (port 1)	—
66	V_{DD2}	—	I/O power supply	—
67	V_{SS}	—	GND	—
68	B1OUT5	O	Blue data output (port 1)	—
69	B1OUT6	O	Blue data output (port 1)	—
70	B1OUT7	O	Blue data output (port 1)	—
71	B1OUT8	O	Blue data output (port 1)	—
72	B1OUT9	O	Blue data output (port 1)	—
73	G2OUT0	O	Green data output (port 2)	—
74	G2OUT1	O	Green data output (port 2)	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
75	G2OUT2	O	Green data output (port 2)	—
76	G2OUT3	O	Green data output (port 2)	—
77	V_{DD1}	—	Internal operation power supply	—
78	V_{SS}	—	GND	—
79	G2OUT4	O	Green data output (port 2)	—
80	G2OUT5	O	Green data output (port 2)	—
81	G2OUT6	O	Green data output (port 2)	—
82	G2OUT7	O	Green data output (port 2)	—
83	G2OUT8	O	Green data output (port 2)	—
84	V_{DD2}	—	I/O power supply	—
85	G2OUT9	O	Green data output (port 2)	—
86	G1OUT0	O	Green data output (port 1)	—
87	G1OUT1	O	Green data output (port 1)	—
88	G1OUT2	O	Green data output (port 1)	—
89	V_{DD1}	—	Internal operation power supply	—
90	V_{SS}	—	GND	—
91	G1OUT3	O	Green data output (port 1)	—
92	G1OUT4	O	Green data output (port 1)	—
93	G1OUT5	O	Green data output (port 1)	—
94	G1OUT6	O	Green data output (port 1)	—
95	G1OUT7	O	Green data output (port 1)	—
96	G1OUT8	O	Green data output (port 1)	—
97	G1OUT9	O	Green data output (port 1)	—
98	R2OUT0	O	Red data output (port 2)	—
99	R2OUT1	O	Red data output (port 2)	—
100	V_{DD2}	—	I/O power supply	—
101	V_{DD1}	—	Internal operation power supply	—
102	V_{SS}	—	GND	—
103	R2OUT2	O	Red data output (port 2)	—
104	R2OUT3	O	Red data output (port 2)	—
105	R2OUT4	O	Red data output (port 2)	—
106	R2OUT5	O	Red data output (port 2)	—
107	R2OUT6	O	Red data output (port 2)	—
108	R2OUT7	O	Red data output (port 2)	—
109	R2OUT8	O	Red data output (port 2)	—
110	R2OUT9	O	Red data output (port 2)	—
111	R1OUT0	O	Red data output (port 1)	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
112	R1OUT1	O	Red data output (port 1)	—
113	R1OUT2	O	Red data output (port 1)	—
114	V_{DD2}	—	I/O power supply	—
115	V_{SS}	—	GND	—
116	R1OUT3	O	Red data output (port 1)	—
117	R1OUT4	O	Red data output (port 1)	—
118	R1OUT5	O	Red data output (port 1)	—
119	R1OUT6	O	Red data output (port 1)	—
120	R1OUT7	O	Red data output (port 1)	—
121	R1OUT8	O	Red data output (port 1)	—
122	R1OUT9	O	Red data output (port 1)	—
123	VSTR	O	Vertical display start timing pulse output	—
124	VCKR	O	Vertical display transfer clock output	—
125	ENBR	O	Gate enable pulse output	—
126	V_{DD2}	—	I/O power supply	—
127	V_{SS}	—	GND	—
128	DCK2	O	DCK2 pulse output	—
129	DCK2X	O	DCK2X pulse output	—
130	V_{SS}	—	GND	—
131	DCK1X	O	DCK1X pulse output	—
132	DCK1	O	DCK1 pulse output	—
133	V_{SS}	—	GND	—
134	HCK1	O	Horizontal display transfer clock output 1	—
135	HCK2	O	Horizontal display transfer clock output 2	—
136	RGT	I/O	Horizontal scan direction switching signal I/O	—
137	XRGT	O	Horizontal scan direction switching signal output (reversed polarity of RGT)	—
138	V_{DD2}	—	I/O power supply	—
139	V_{SS}	—	GND	—
140	HST	O	Horizontal display start timing pulse output	—
141	BLK	O	BLK pulse output	—
142	ENBL	O	Gate enable pulse output	—
143	VCKL	O	Vertical display transfer clock output	—
144	V_{DD2}	—	I/O power supply	—
145	V_{DD1}	—	Internal operation power supply	—
146	VSTL	O	Vertical display start timing pulse output	—
147	DWN	I/O	Vertical scan direction switching signal I/O	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
148	CTRL	I	Scan direction control method switching (Low: internal register, High: external)	L
149	PCG	O	Collective precharge timing pulse output	—
150	V_{SS}	—	GND	—
151	PST	O	Dot sequential precharge start timing pulse output	—
152	PO3	O	Parallel output 3	—
153	PO2	O	Parallel output 2	—
154	PO1	O	Parallel output 1	—
155	HD2	O	Horizontal auxiliary pulse output 2	—
156	V_{DD1}	—	Internal operation power supply	—
157	FRP	O	AC drive inversion timing pulse output	—
158	XFRP	O	AC drive inversion timing pulse output (reversed polarity of FRP)	—
159	SHST	O	SHST pulse output	—
160	DENB	O	DENB pulse output	—
161	PRG	O	2-step precharge timing pulse output	—
162	V_{DD1}	—	Internal operation power supply	—
163	V_{SS}	—	GND	—
164	PO4	O	Parallel output 4	—
165	CLP	O	CLP pulse output	—
166	PO5	O	Parallel output 5	—
167	HD1	O	Horizontal auxiliary pulse output 1	—
168	TEST1	—	Test pin (Connect to GND.)	—
169	TEST2	—	Test pin (Connect to GND.)	—
170	TEST3	—	Test pin (Connect to V_{DD2}.)	—
171	TEST4	—	Test pin (Connect to V_{DD2}.)	—
172	TEST5	—	Test pin (Connect to V_{DD2}.)	—
173	TEST6	—	Test pin (Connect to V_{DD2}.)	—
174	V_{DD2}	—	I/O power supply	—
175	V_{SS}	—	GND	—
176	R1IN7	I	Red data input (port 1)	—
177	R1IN6	I	Red data input (port 1)	—
178	R1IN5	I	Red data input (port 1)	—
179	R1IN4	I	Red data input (port 1)	—
180	R1IN3	I	Red data input (port 1)	—
181	R1IN2	I	Red data input (port 1)	—
182	R1IN1	I	Red data input (port 1)	—
183	R1IN0	I	Red data input (port 1)	—
184	R2IN7	I	Red data input (port 2)	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
185	R2IN6	I	Red data input (port 2)	—
186	V_{DD2}	—	I/O power supply	—
187	V_{SS}	—	GND	—
188	R2IN5	I	Red data input (port 2)	—
189	R2IN4	I	Red data input (port 2)	—
190	R2IN3	I	Red data input (port 2)	—
191	R2IN2	I	Red data input (port 2)	—
192	R2IN1	I	Red data input (port 2)	—
193	R2IN0	I	Red data input (port 2)	—
194	G1IN7	I	Green data input (port 1)	—
195	G1IN6	I	Green data input (port 1)	—
196	G1IN5	I	Green data input (port 1)	—
197	V_{DD1}	—	Internal operation power supply	—
198	V_{SS}	—	GND	—
199	G1IN4	I	Green data input (port 1)	—
200	G1IN3	I	Green data input (port 1)	—
201	G1IN2	I	Green data input (port 1)	—
202	G1IN1	I	Green data input (port 1)	—
203	G1IN0	I	Green data input (port 1)	—
204	G2IN7	I	Green data input (port 2)	—
205	G2IN6	I	Green data input (port 2)	—
206	G2IN5	I	Green data input (port 2)	—
207	G2IN4	I	Green data input (port 2)	—
208	G2IN3	I	Green data input (port 2)	—
209	V_{DD1}	—	Internal operation power supply	—
210	V_{SS}	—	GND	—
211	G2IN2	I	Green data input (port 2)	—
212	G2IN1	I	Green data input (port 2)	—
213	G2IN0	I	Green data input (port 2)	—
214	B1IN7	I	Blue data input (port 1)	—
215	B1IN6	I	Blue data input (port 1)	—
216	B1IN5	I	Blue data input (port 1)	—
217	B1IN4	I	Blue data input (port 1)	—
218	B1IN3	I	Blue data input (port 1)	—
219	B1IN2	I	Blue data input (port 1)	—
220	B1IN1	I	Blue data input (port 1)	—
221	V_{DD1}	—	Internal operation power supply	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
222	V_{SS}	—	GND	—
223	B1IN0	I	Blue data input (port 1)	—
224	B2IN7	I	Blue data input (port 2)	—
225	B2IN6	I	Blue data input (port 2)	—
226	B2IN5	I	Blue data input (port 2)	—
227	B2IN4	I	Blue data input (port 2)	—
228	B2IN3	I	Blue data input (port 2)	—
229	B2IN2	I	Blue data input (port 2)	—
230	B2IN1	I	Blue data input (port 2)	—
231	B2IN0	I	Blue data input (port 2)	—
232	R1OSD1	I	OSD red data input (port 1)	—
233	R1OSD0	I	OSD red data input (port 1)	—
234	V_{DD2}	—	I/O power supply	—
235	V_{SS}	—	GND	—
236	G1OSD1	I	OSD green data input (port 1)	—
237	G1OSD0	I	OSD green data input (port 1)	—
238	B1OSD1	I	OSD blue data input (port 1)	—
239	B1OSD0	I	OSD blue data input (port 1)	—
240	YM1	I	OSD YM input (port 1)	L

* H: Pull-up, L: Pull-down

Electrical Characteristics

DC Characteristics

(Topr = –20 to +75°C, V_{SS} = 0V)

Item	Symbol	Applicable pins	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD1}	—		2.3	2.5	2.7	V
	V_{DD2}	—	—	3.0	3.3	3.6	
Input voltage 1	V_{IH1}	*1	CMOS input cell	2.0	—	V_{DD2} + 0.3	
	V_{IL1}			–0.3	—	0.8	
Input voltage 2	V_{IH2}	HDIN, VDIN, PCTL, PCLK, PDAT0 to PDAT9	CMOS Schmitt trigger input cell	0.8V_{DD2}	—	V_{DD2} + 0.3	
	V_{IL2}			–0.3	—	0.2V_{DD2}	
Input voltage 3	VC*2	CLKP, CLKN	Small-amplitude differential input	1.718	2.0	2.281	
	V_{IH3}			1.868	VC + 0.4	V_{DD2}	
	V_{IL3}			V_{SS}	VC – 0.4	2.131	
Output voltage	V_{OH}	All output pins	—	V_{DD2} – 0.5	—	V_{DD2}	
	V_{OL}		—	V_{SS}	—	0.2	
Current consumption	P_D*3	—	CLKP = 200MHz	—	2600	3120	mW

*1 Input pins other than those indicated in items Input voltage 2 and Input voltage 3.

*2 V_{IH3} > VC (max.) and V_{IL3} < VC (min.).

*3 Tj [°C] ≥ Toprmax [°C] + θja [°C/W] × P_D [W].
(Tj = 125 [°C], Toprmax = 75 [°C], θja = 16 [°C/W], when mounted on a 4-layer substrate)

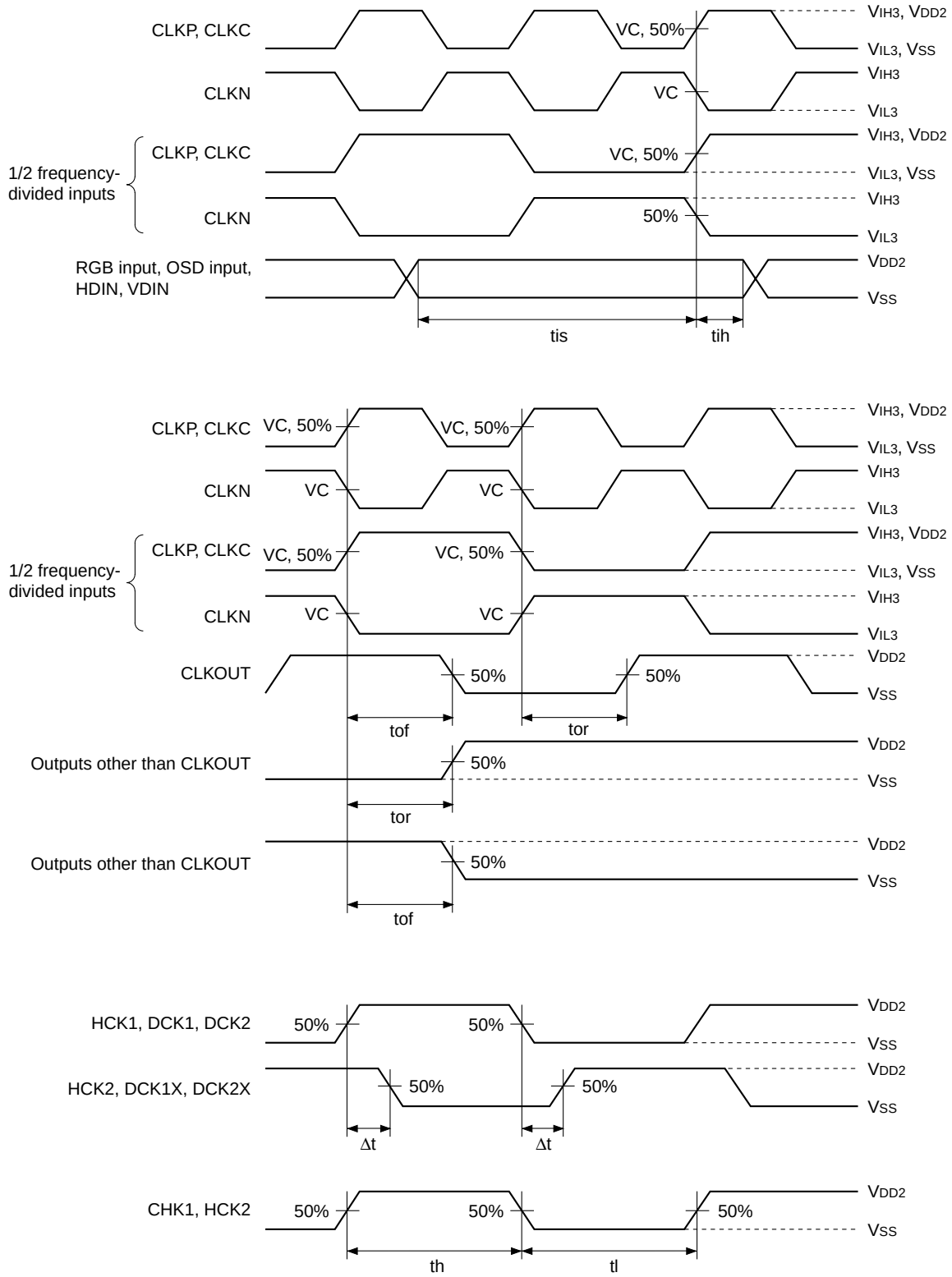
AC Characteristics

(Topr = –20 to +75°C, V_{DD1} = 2.5 ± 0.2V, V_{DD2} = 3.3 ± 0.3V, V_{SS} = 0V)

Item	Symbol	Applicable pins	Conditions	Min.	Typ.	Max.	Unit
Clock input period	—	CLKP, CLKN, CLKC	—	5	—	—	ns
Input setup time	tis	RGB input, OSD input, HDIN, VDIN	—	2.5	—	—	
Input hold time	tih		—	1.5	—	—	
Output rise/fall delay time	tor/tof	*4	CL = 20pF	2	5	10	
Output rise/fall delay time	tor/tof	RGB output	CL = 20pF	2	4	8	
Output rise/fall delay time	tor/tof	CLKOUT	CL = 50pF	1.5	4.5	8.5	
Cross-point time difference	Δt	HCK1, HCK2, DCK1, DCK1X, DCK2, DCK2X	CL = 20pF	–5	—	5	
HCK1 duty	th/(th + tl)	HCK1	CL = 20pF	48	50	52	%
HCK2 duty	tl/(th + tl)	HCK2	CL = 20pF	48	50	52	
Phase compensation PLL operating frequency	—	—	PLLDIV = L	55	—	100	MHz
			PLLDIV = H	27.5	—	55	

*4 Output pins other than RGB output, CLKOUT, PO1 to PO5, RGT, XRGT and DWN.

Timing Definition

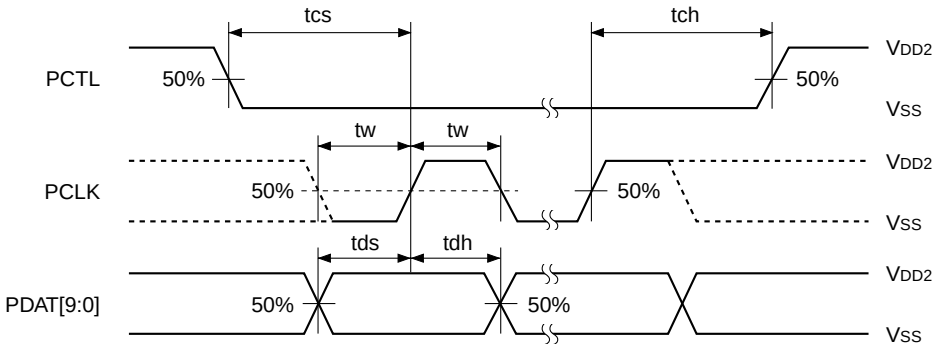


Parallel I/F Block AC Characteristics (Topr = –20 to +75°C, V_{DD1} = 2.5 ± 0.2V, V_{DD2} = 3.3 ± 0.3V, V_{SS} = 0V)

Item	Symbol	Min.	Typ.	Max.
PCTL setup time with respect to rise of PCLK	tcs	8T*5	—	—
PCTL hold time with respect to rise of PCLK	tch	8T	—	—
PDAT[9:0] setup time with respect to rise of PCLK	tds	4T	—	—
PDAT[9:0] hold time with respect to rise of PCLK	tdh	4T	—	—
PCLK pulse width	tw	4T	—	—

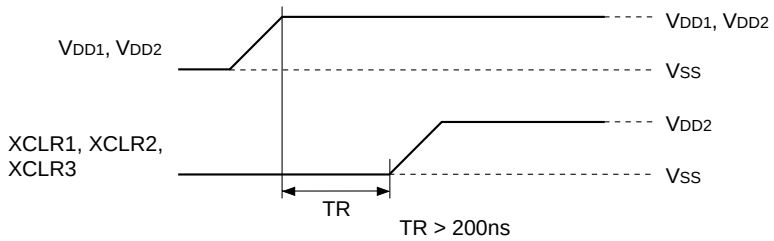
*5 T: Master clock (CLKP, CLKN, CLKC) period [ns]

Timing Definition



Power-on and Initialization of Internal Circuit

As for this IC, two systems of supply voltage should be turned on simultaneously. The initialization of the internal circuit should be also performed by maintaining the system clear pin at low during the specified time after setting the supply voltage in the range of recommended operating conditions and stabilizing as shown in the figure below. Keep in mind that the internal circuit may not be initialized correctly if system clear cancellation is performed before the supply voltage is set in the range of the recommended operating conditions.



Description of Operation

1. Description of Input Pins

(a) System clear pins (XCLR1, XCLR2 and XCLR3)

All internal circuits are initialized by setting XCLR1 (Pin 27) low. In addition, the internal PLL is initialized by setting XCLR2 (Pin 28) low, and RGB output is initialized (preset) by setting XCLR3 (Pin 29) low.
Initialization should be performed when power is turned on. There are no particular restrictions on the initialization order.

(b) Sync signal input pins (HDIN and VDIN)

Horizontal and vertical separate sync signals are input to HDIN (Pin 31) and VDIN (Pin 32), respectively. The CXD3511Q supports only non-interlace sync signals with a dot clock of 200MHz or less.

(c) Master clock input pins (CLKP/CLKN and CLKC)

Phase comparison is performed by an external circuit and a clock synchronized to the sync signal is input. The master clock input pins have two systems consisting of CLKP/CLKN (Pins 38 and 39) for small-amplitude differential input (center level: 2.0V, amplitude: ±0.4V), and CLKC (Pin 35) for CMOS level input. In addition, be sure to make the number of dot clocks in 1H as even number.
Note that if there is an odd number of dot clocks, the internal phase compensation PLL will not operate properly.

(d) Clock selection pins (CLKSEL1 and CLKSEL2)

The master clock input pins can input either the system dot clock or the 1/2 frequency-divided clock. The internal clock path is selected according to CLKSEL1 (Pin 41) and CLKSEL2 (Pin 44).

Symbol	Function	Setting	
		L	H
CLKSEL1	Input clock selection	CLKP/CLKN input	CLKC input
CLKSEL2	Clock input pin selection	Dot clock input	1/2 frequency-divided clock input

(e) PLL setting pin (PLLDIV)

PLLDIV (Pin 45) sets the divider setting of the internal phase compensation PLL circuit. Set PLLDIV low when the internal clock frequency is 55 to 100MHz, or high when 27.5 to 55MHz. In addition, note that the frequency of the clock input to the CXD3511Q must be within the phase compensation PLL operating range, even during free running.

(f) RGB signal input pins (R1IN, R2IN, G1IN, G2IN, B1IN and B2IN)

These pins input RGB signals that have been demultiplexed to 1:2. The Red signal is input to R1IN (Pins 176 to 183) and R2IN (Pins 184, 185 and 188 to 193), the Green signal to G1IN (Pins 194 to 196 and 199 to 203) and G2IN (Pins 204 to 208 and 211 to 213), and the Blue signal to B1IN (Pins 214 to 220 and 223) and B2IN (Pins 224 to 231).

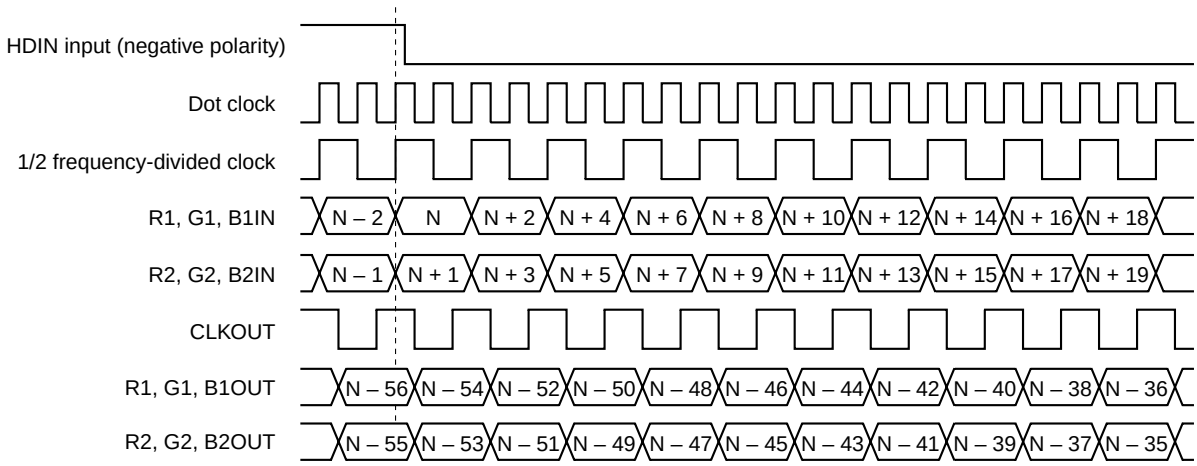
(g) OSD signal input pins (R1OSD, R2OSD, G1OSD, G2OSD, B1OSD, B2OSD, YM1, YM2, YS1 and YS2)

These pins input OSD signals that have been demultiplexed to 1:2. The Red signal is input to R1OSD (Pins 232 and 233) and R2OSD (Pins 2 and 3), the Green signal to G1OSD (Pins 236 and 237) and G2OSD (Pins 4 and 5), and the Blue signal to B1OSD (Pins 238 and 239) and B2OSD (Pins 8 and 9). In addition, the YM signal is input to YM1 (Pin 240) and YM2 (Pin 10), and the YS signal to YS1 (Pin 1) and YS2 (Pin 11).

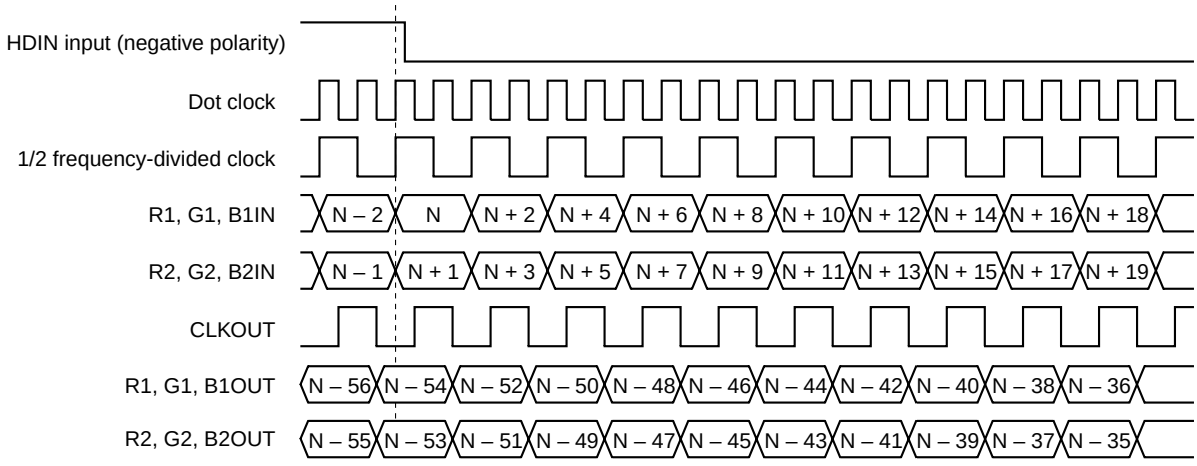
2. RGB Signal and OSD Signal Pipeline Delay

The RGB signal I/O pipeline delay is 54 dot clocks. In addition, the OSD, YM and YS signal pipeline delay is 34 dot clocks. Note that the phase relationship between each clock and the RGB signals is as shown in the figures below. This relationship is the same for the OSD, YM and YS signals.

(1) CLKPOL = L

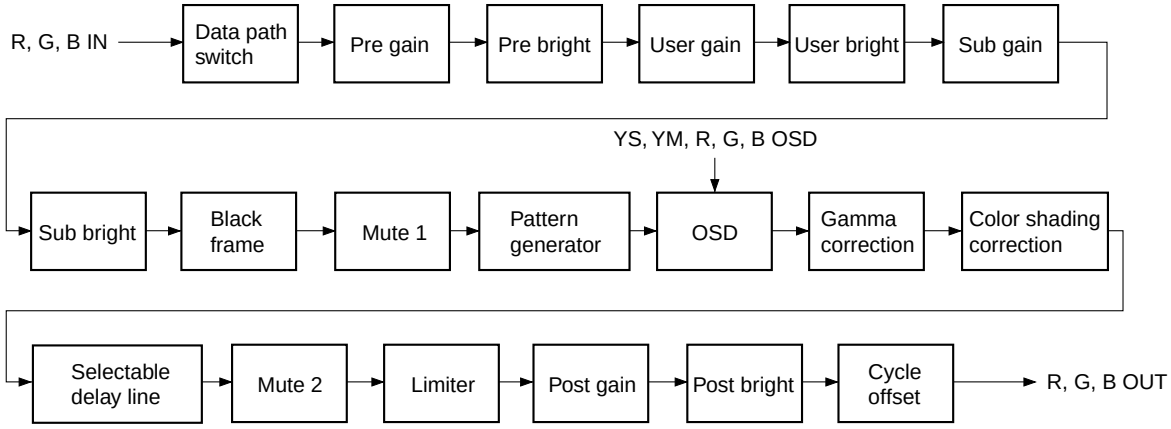


(2) CLKPOL = H



3. Description of DSD Block Signal Processing Functions

The DSD block signal processing flow is shown below.

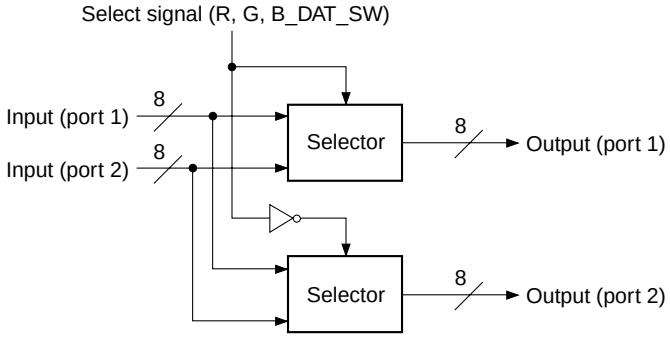


The various signal processing functions are described below. Note that the coefficients used for each arithmetic operation are set through the parallel I/F block. See the individual descriptions of each parallel I/F block item for a detailed description of the parallel I/F block.

(a) Data path switch block

This block can switch the path of the data input to ports 1 and 2. The setting is as follows.

Select signal: 1 = Path switched, 0 = Path not switched (Set independently for R, G and B)

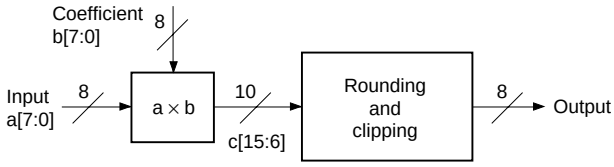


(b) Pre gain block

This block performs multiplication processing independently for ports 1 and 2. The settings are as follows.

Coefficient: 8 bits
Gain setting: 0 to 1.9921875 (= 255/128) times, variable in 256 steps
(Set independently for R, G and B ports 1 and 2)

Multiplication is performed using the 8-bit input and an 8-bit coefficient, and the upper 10 bits c[15:6] of the operation results are output. Next, the c[6] value is checked and rounding is performed to 9 bits. The MSB of the rounded 9 bits is checked, clipping is performed, and the lower 8 bits are output.

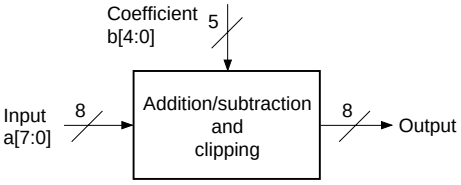


(c) Pre bright block

This block performs addition and subtraction processing independently for ports 1 and 2. The settings are as follows.

Coefficient: 5 bits with code, MSB = code bit
Bright setting: –16 to +15 scales, variable with an accuracy of 1 bit
(Set independently for R, G and B ports 1 and 2)

Multiplication is performed using the 8-bit input and a 5-bit coefficient with code. The coefficient MSB is the code bit. Addition is performed when b[4] = 0, and subtraction when b[4] = 1. However, when performing subtraction, set the two's complement in the lower bits of the coefficient. When the operation results overflow or underflow, clipping is performed.

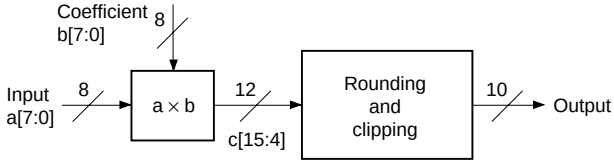


(d) User gain block

This block performs multiplication processing independently for ports 1 and 2. The settings are as follows.

Coefficient: 8 bits
Gain setting: 0 to 7.96875 (= 255/32) times, variable in 256 steps
(Settings shared by R, G and B)

Multiplication is performed using the 8-bit input and an 8-bit coefficient, and the upper 12 bits c[15:4] of the operation results are output. Next, the c[4] value is checked and rounding is performed to 11 bits. The MSB of the rounded 11 bits is checked, clipping is performed, and the lower 10 bits are output.

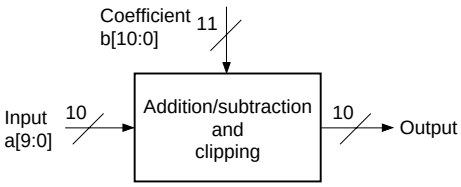


(e) User bright block

This block performs addition and subtraction processing as the user control bright adjustment. The settings are as follows.

Coefficient: 11 bits with code, MSB = code bit
Bright setting: –1024 to +1023 scales, variable with an accuracy of 1 bit
(Settings shared by R, G and B)

Multiplication is performed using the 10-bit input and an 11-bit coefficient with code. The coefficient MSB is the code bit. Addition is performed when b[10] = 0, and subtraction when b[10] = 1. However, when performing subtraction, set the two's complement in the lower bits of the coefficient. When the operation results overflow or underflow, clipping is performed.

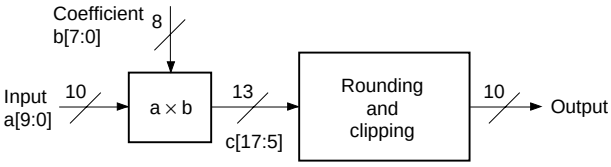


(f) Sub gain block

This block performs multiplication processing as the white balance gain adjustment. The settings are as follows.

Coefficient: 8 bits
Gain setting: 0 to 3.984375 (255/64) times, variable in 256 steps
(Set independently for R, G and B)

Multiplication is performed using the 10-bit input and an 8-bit coefficient, and the upper 13 bits c[17:5] of the operation results are output. Next, the c[5] value is checked and rounding is performed to 12 bits. The upper 2 bits of the rounded 12 bits is checked, clipping is performed, and the lower 10 bits are output.

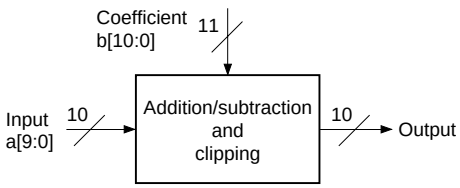


(g) Sub bright block

This block performs addition and subtraction processing as the white balance bright adjustment. The settings are as follows.

Coefficient: 11 bits with code, MSB = code bit
Bright setting: –1024 to +1023 scales, variable with an accuracy of 1 bit
(Set independently for R, G and B)

Multiplication is performed using the 10-bit input and an 11-bit coefficient with code. The coefficient MSB is the code bit. Addition is performed when b[10] = 0, and subtraction when b[10] = 1. However, when performing subtraction, set the two's complement in the lower bits of the coefficient. When the operation results overflow or underflow, clipping is performed.

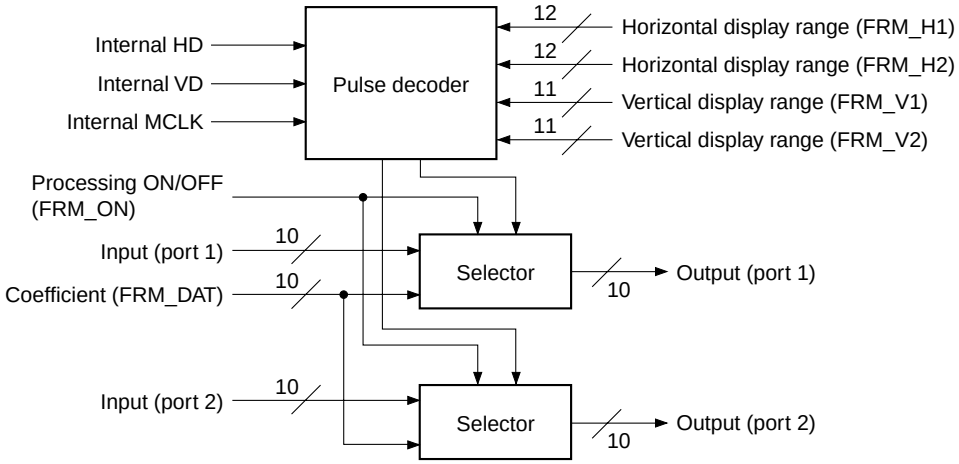


(h) Black frame block

This block performs processing to fix the blanking period of the video signal to the desired level regardless of the front-end signal processing results.
If the number of pixels calculated from the effective period of the video signal to be displayed is less than the number of pixels of the LCD panel on which the signal is to be displayed, the blanking period of the video signal is displayed in the excess pixels. At this time, the displayed blanking period can be fixed to the desired level regardless of the gain and bright adjustment or other picture quality adjustment results by processing with this block. The settings are as follows.

FRM_ON: 1 = Black frame processing ON, 0 = OFF
FRM_DAT: Black frame level setting
FRM_H1, FRM_H2: Set the black frame horizontal display range in 1-dot units
FRM_V1, FRM_V2: Set the black frame vertical display range in 1-line units
(All settings shared by R, G and B)

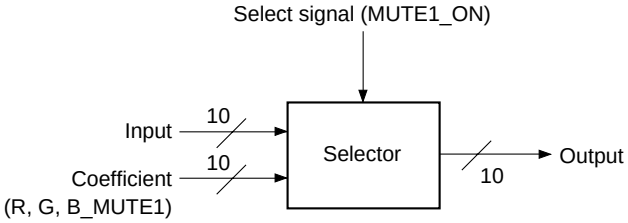
Here, the desired range of the video signal is replaced with 10-bit data (FRM_DAT) by switching the video signal (port 1 and port 2) and the coefficients using the pulse output from the pulse decoder.



(i) Mute 1 block

This block performs mute processing by replacing the video signal with data of the desired level. The settings are as follows.

MUTE1_ON: 1 = Mute processing ON, 0 = OFF (Setting shared by R, G and B)
R, G, B_MUTE1: RGB mute data (Set independently for R, G and B)



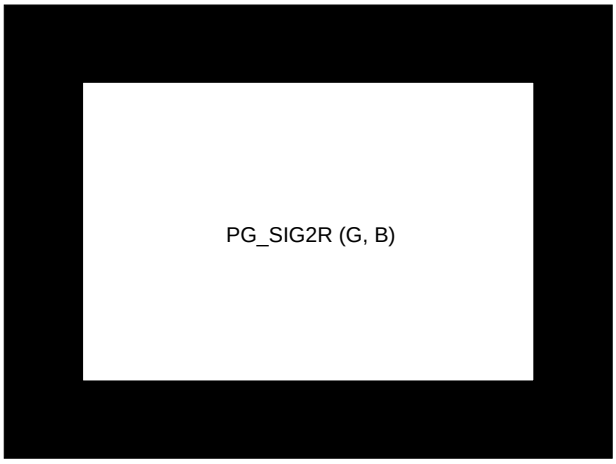
(j) Pattern generator block

This block generates and outputs the set fixed pattern independently of the input signal. This function is valid when PG_ON = 1. When PG_R (G, B)_ON is "0", the signal level goes to 000h respectively for R, G and B.
The raster display pattern is displayed in the effective area, and all other display patterns are displayed in the window area. Here, the effective area is set by PG_HST, PG_HSTP, PG_VST and PG_VSTP, and the window area is set by PG_HWST, PG_HWSTP, PG_VWST and PG_VWSTP.
The display pattern signal level is set independently for R, G and B by PG_SIG1R (G, B)[9:0] and PG_SIG2R (G, B)[9:0]. Within the effective area, the pattern and non-pattern signal levels can be switched by PG_R (G, B)_SEL. At this time, the signal level outside the effective area goes to 000h. During horizontal ramp, horizontal stair, vertical ramp and vertical stair display, the PG_SIG1R (G, B)[9:0] and PG_SIG2R (G, B)[9:0] settings are invalid.

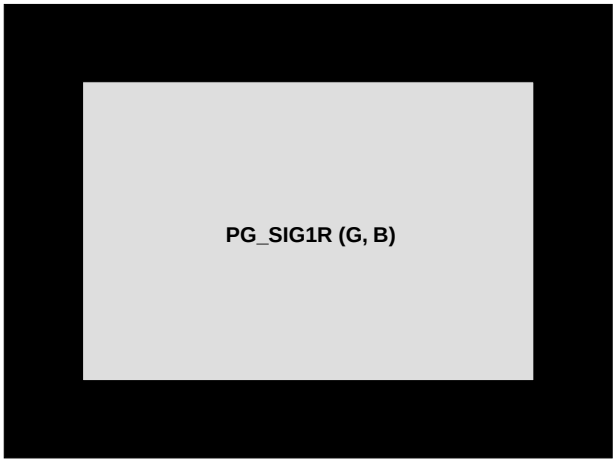
The display patterns and signal levels are as follows.

(1) Raster display

When PG_PAT[2:0] = 0h, a raster is displayed.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	0h
PG_STRP_SW	x
PG_STAIR_SW	x

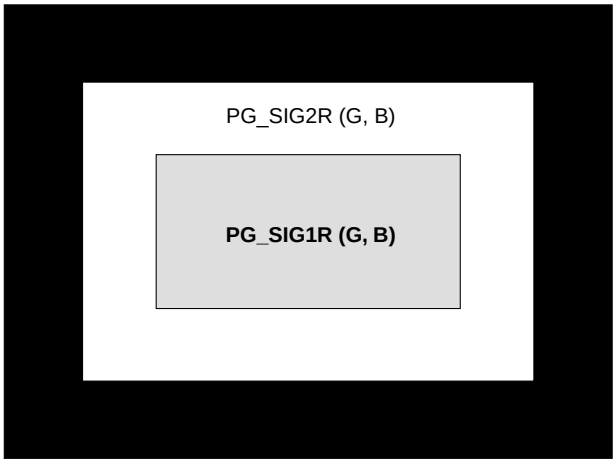


PG_R (G, B)_SEL	1
PG_PAT[2:0]	0h
PG_STRP_SW	x
PG_STAIR_SW	x

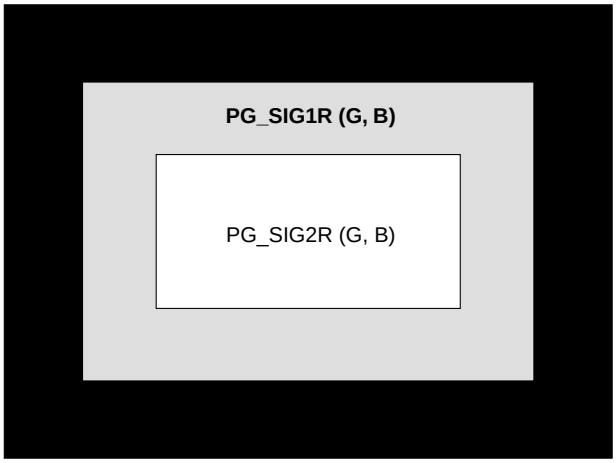
x: Don't care

(2) Window display

When PG_PAT[2:0] = 1h, a window is displayed.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	1h
PG_STRP_SW	x
PG_STAIR_SW	x

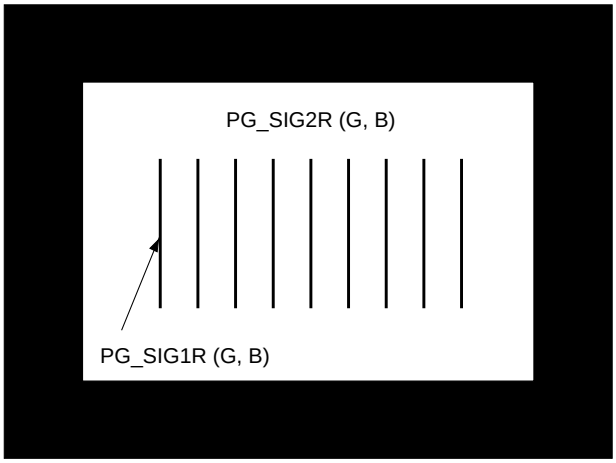


PG_R (G, B)_SEL	1
PG_PAT[2:0]	1h
PG_STRP_SW	x
PG_STAIR_SW	x

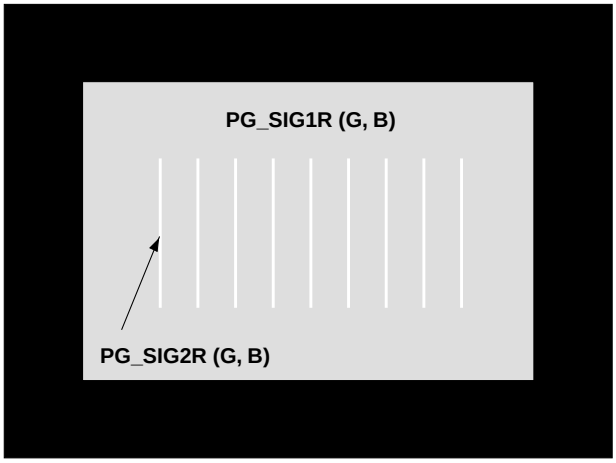
x: Don't care

(3) Vertical stripe display

When PG_PAT[2:0] = 2h and PG_STRP_SW = 0, vertical stripes are displayed.
The stripe period is set by PG_STEP in 2-dot units. The stripe width is set by PG_WIDTH in 1-dot units.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	2h
PG_STRP_SW	0
PG_STAIR_SW	x

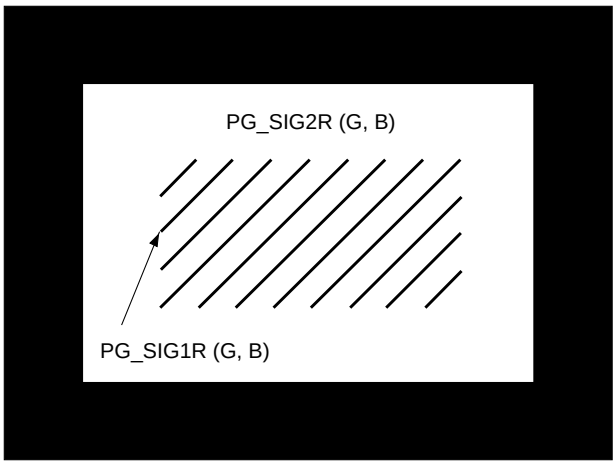


PG_R (G, B)_SEL	1
PG_PAT[2:0]	2h
PG_STRP_SW	0
PG_STAIR_SW	x

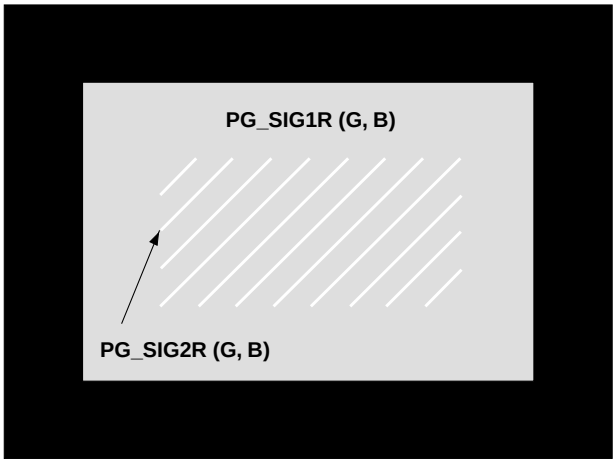
x: Don't care

(4) Diagonal stripes

When PG_PAT[2:0] = 2h and PG_STRP_SW = 1, diagonal stripes are displayed.
The stripe period is set by PG_STEP in 2-dot units. The stripe width is set by PG_WIDTH in 1-dot units.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	2h
PG_STRP_SW	1
PG_STAIR_SW	x

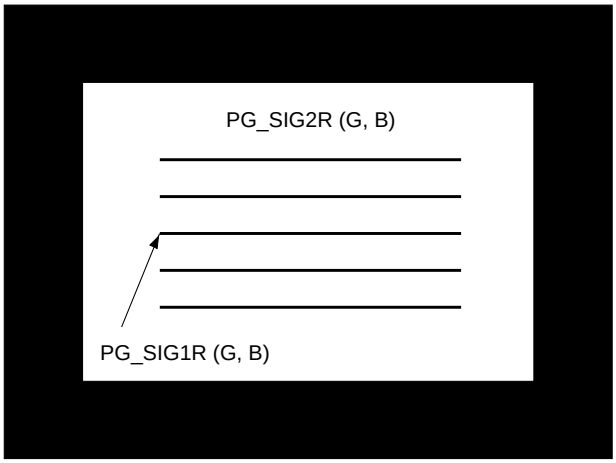


PG_R (G, B)_SEL	1
PG_PAT[2:0]	2h
PG_STRP_SW	1
PG_STAIR_SW	x

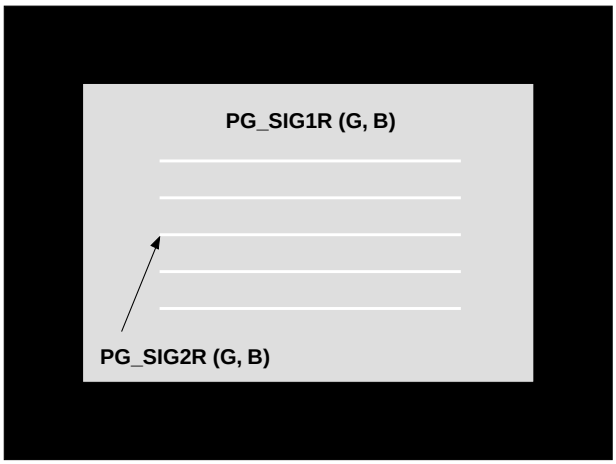
x: Don't care

(5) Horizontal stripes

When PG_PAT[2:0] = 3h, horizontal stripes are displayed.
The stripe period is set by PG_STEP in 2-dot units. The stripe width is set by PG_WIDTH in 1-dot units.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	3h
PG_STRP_SW	x
PG_STAIR_SW	x

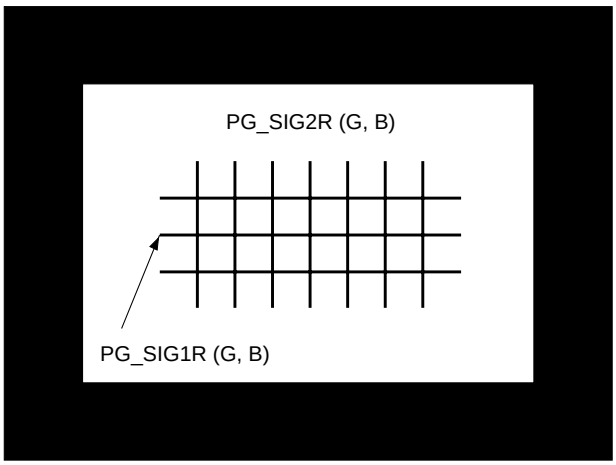


PG_R (G, B)_SEL	1
PG_PAT[2:0]	3h
PG_STRP_SW	x
PG_STAIR_SW	x

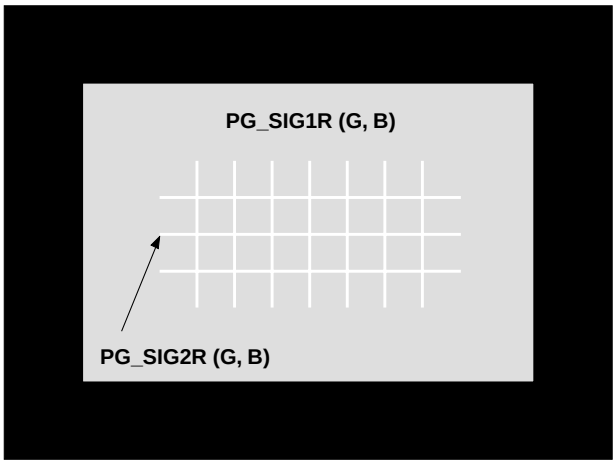
x: Don't care

(6) Cross hatch

When PG_PAT[2:0] = 4h, a cross hatch is displayed.
The stripe period is set by PG_STEP in 2-dot units. The stripe width is set by PG_WIDTH in 1-dot units.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	4h
PG_STRP_SW	x
PG_STAIR_SW	x

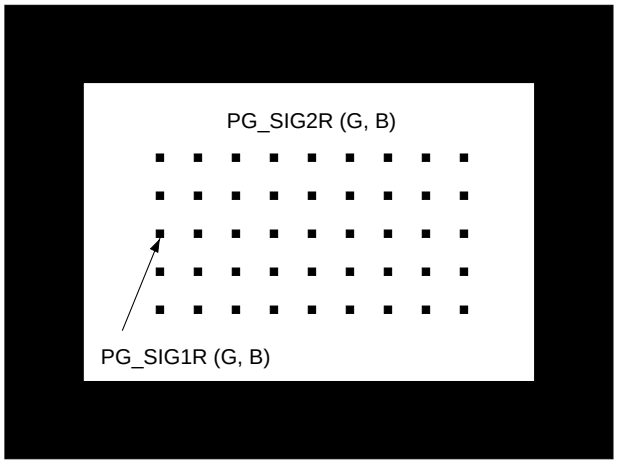


PG_R (G, B)_SEL	1
PG_PAT[2:0]	4h
PG_STRP_SW	x
PG_STAIR_SW	x

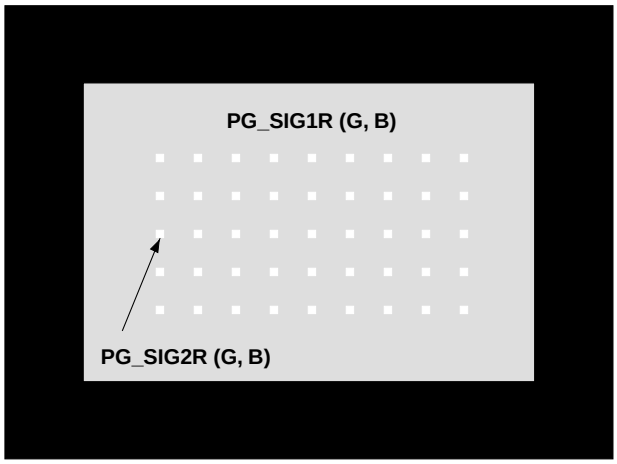
x: Don't care

(7) Dots

When PG_PAT[2:0] = 5h, a dot pattern is displayed.
The dot period is set by PG_STEP in 2-dot units. The dot width is set by PG_WIDTH in 1-dot units.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	5h
PG_STRP_SW	x
PG_STAIR_SW	x

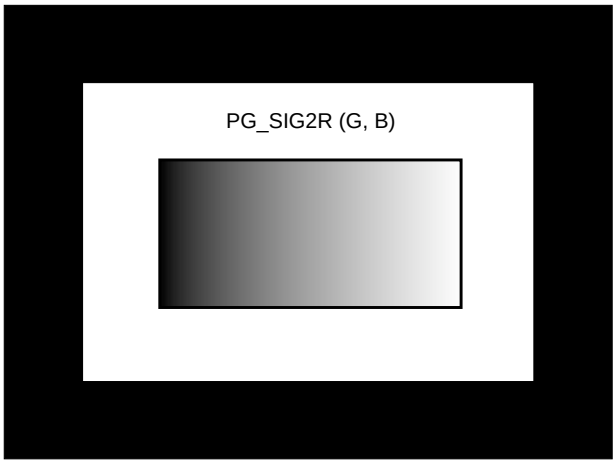


PG_R (G, B)_SEL	1
PG_PAT[2:0]	5h
PG_STRP_SW	x
PG_STAIR_SW	x

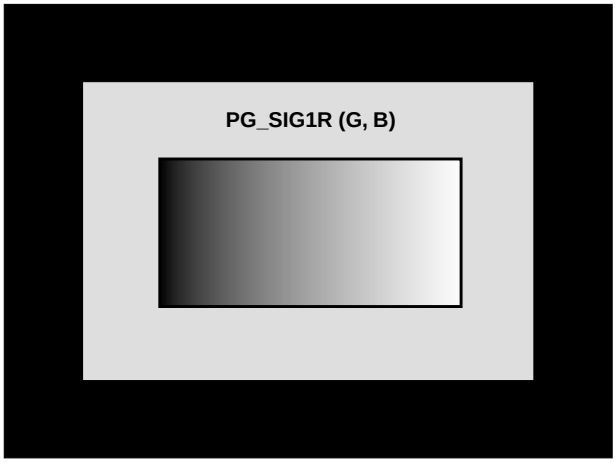
x: Don't care

(8) Horizontal ramp

When PG_PAT[2:0] = 6h and PG_STAIR_SW = 0, a horizontal ramp is displayed.
The signal level is incremented from 000h by one bit for each dot.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	6h
PG_STRP_SW	x
PG_STAIR_SW	0

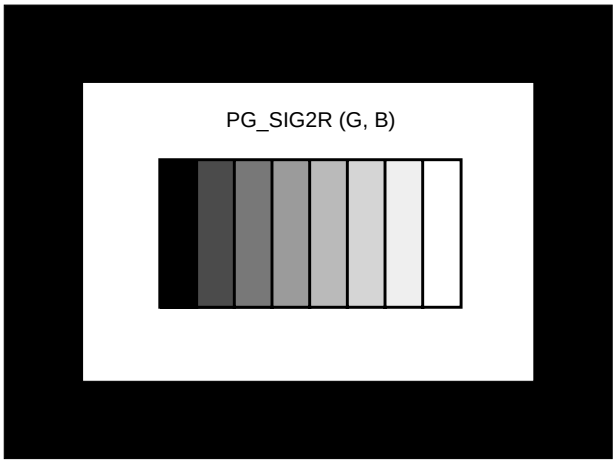


PG_R (G, B)_SEL	1
PG_PAT[2:0]	6h
PG_STRP_SW	x
PG_STAIR_SW	0

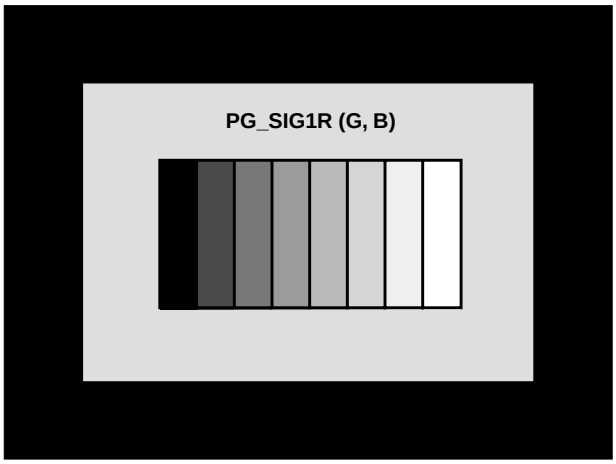
x: Don't care

(9) Horizontal stair

When PG_PAT[2:0] = 6h and PG_STAIR_SW = 1, a horizontal stair is displayed.
The signal level is incremented from 000h by 64 bits for each 64 dots.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	6h
PG_STRP_SW	x
PG_STAIR_SW	1

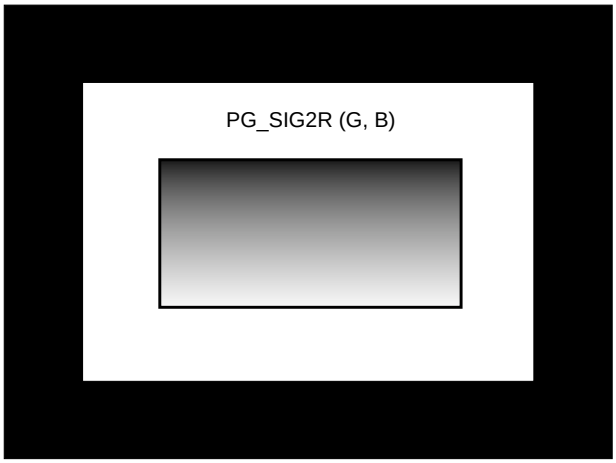


PG_R (G, B)_SEL	1
PG_PAT[2:0]	6h
PG_STRP_SW	x
PG_STAIR_SW	1

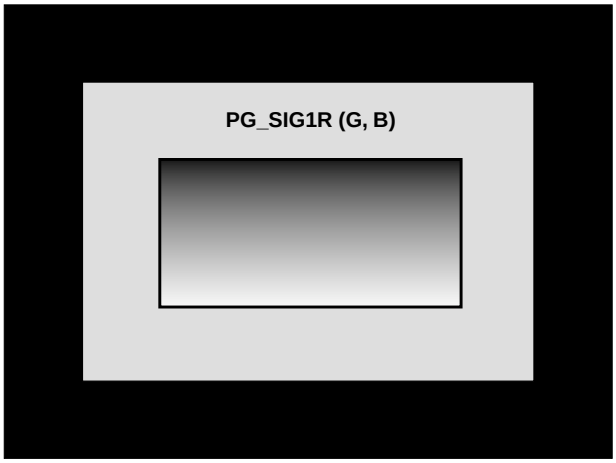
x: Don't care

(10) Vertical ramp

When PG_PAT[2:0] = 7h and PG_STAIR_SW = 0, a vertical ramp is displayed.
The signal level is incremented from 000h by one bit for each line.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	7h
PG_STRP_SW	x
PG_STAIR_SW	0

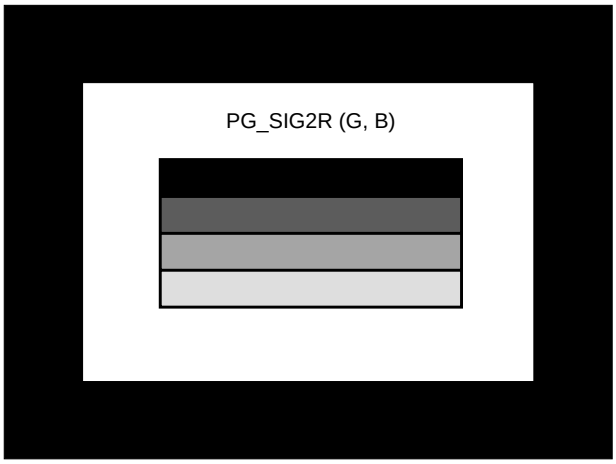


PG_R (G, B)_SEL	1
PG_PAT[2:0]	7h
PG_STRP_SW	x
PG_STAIR_SW	0

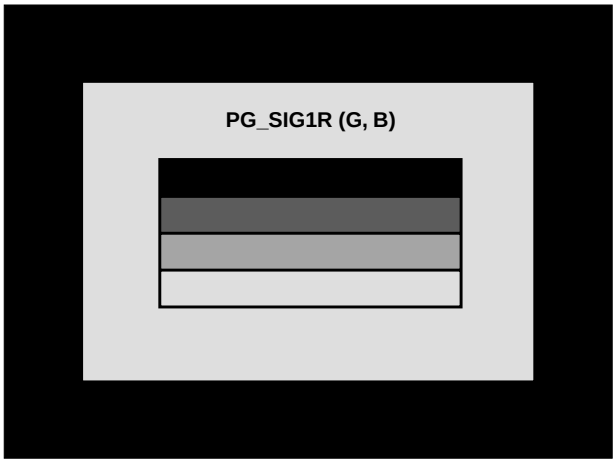
x: Don't care

(11) Vertical stair

When PG_PAT[2:0] = 7h and PG_STAIR_SW = 1, a vertical stair is displayed.
The signal level is incremented from 000h by 64 bits for each 32 lines.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	7h
PG_STRP_SW	x
PG_STAIR_SW	1



PG_R (G, B)_SEL	1
PG_PAT[2:0]	7h
PG_STRP_SW	x
PG_STAIR_SW	1

x: Don't care

(k) OSD block

This block performs video signal half-tone processing and OSD-MIX processing by inputting the 2-bit OSD signal for each color and the YS and YM signals. The half-tone processing setting is as follows.

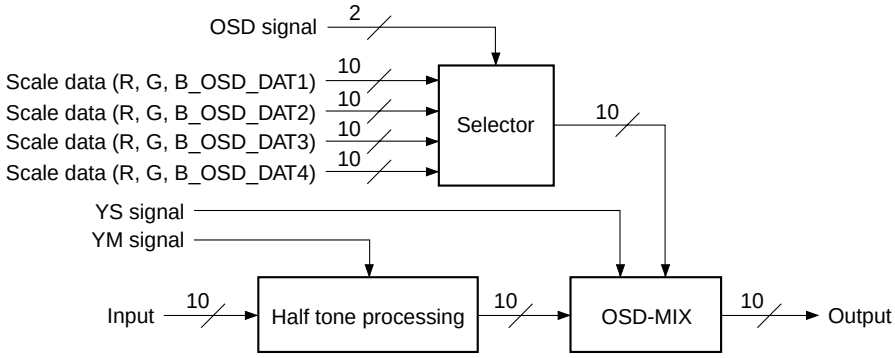
YM signal input: 1 = Half tone processing ON, 0 = OFF

Here, the video signal level is halved by shifting the input data by one bit to the LSB side when YM = 1. For example, when 0F0h is input, 078h is output.
The selector selects one of four types of data with respect to the OSD signal value as shown in the table below. The selected data becomes the OSD signal scale data. The selected scale data can be set independently in 10 bits for R, G and B, so 4 scales can be selected as desired from among 1024 scales for each of R, G and B. Therefore, the desired 64 (= 2^6) colors can be selected from among the total 1.07374 billion (= 2^30) colors for R, G and B.

OSD signal input	Selected scale data
0h	R, G, B_OSD_DAT1
1h	R, G, B_OSD_DAT2
2h	R, G, B_OSD_DAT3
3h	R, G, B_OSD_DAT4

The OSD-MIX processing setting is as follows.

YS signal input: 1 = OSD-MIX processing ON, 0 = OFF

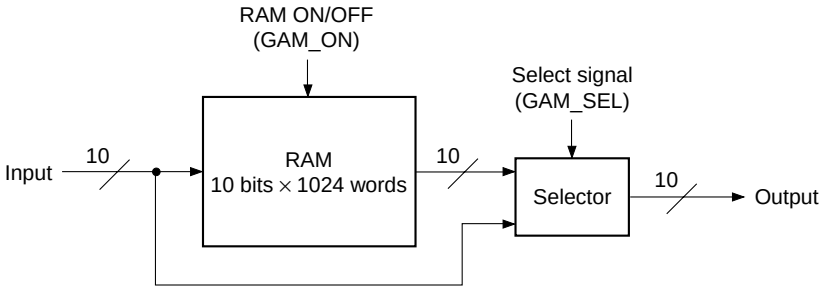


(I) Gamma block

This block performs gamma correction for the user- and white balance-adjusted signal. Gamma correction uses the LUT system, and the RAM size is 10 bits × 1024 words. The settings are as follows.

GAM_ON: 1 = Normal operation, 0 = Standby mode
GAM_SEL: 1 = Path passing through the RAM, 0 = Path not passing through the RAM
(All settings shared by R, G and B)

When operating the RAM, be sure to set GAM_ON = 1. Data cannot be written to or read from the RAM in standby mode. The RAM data is set through the parallel I/F block.
Note that the RAM output is undetermined while data is being set in this RAM, and also during power-on.



(m) Color shading correction block

This block corrects color shading by adding a correction signal to the video signal. Correction points are set at fixed intervals in the horizontal, vertical and scale directions of the video signal. The correction data for these correction points is written in the RAM, and a smooth correction curve is created by reading this data and performing interpolation operations. The settings are as follows.

CSC_ON: 1 = Color shading correction processing ON, 0 = processing OFF
CSC_H_MODE: Sets the horizontal correction interval to 32, 64 or 128 dots
CSC_V_MODE: Sets the vertical correction interval to 32, 64 or 128 lines
CSC_G_MODE: 1 = Scale correction processing ON, 0 = processing OFF
CSC_HNUM: Sets the number of horizontal correction points
CSC_VNUM: Sets the number of vertical correction points
CSC_HP: Sets the horizontal correction start position in 2-dot units
CSC_VP: Sets the vertical correction start position in 1-line units
CSC_R (G, B)_RGT: 1 = Reflects the TG block RGT setting,
0 = Reflects the inverse of the TG block RGT setting
CSC_DWN: 1 = Reflects the TG block DWN setting,
0 = Reflects the inverse of the TG block DWN setting
CSC_XH_ON: 1 = Cross hatch insertion ON, 0 = OFF
(All settings except CSC_R (G, B)_RGT shared by R, G and B)

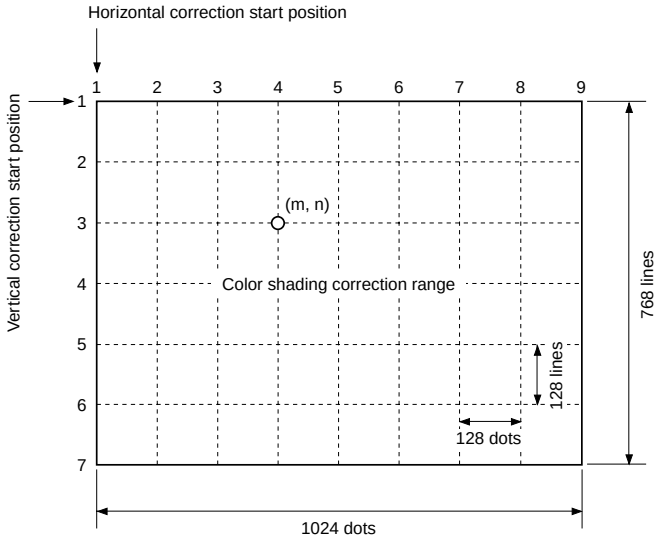
The RAM size is 8 bits × 520 words, so up to 520 correction points can be set. The correction data is set as 8-bit data with code. Correction data can be set in the range of –128 to +127 scale. The example shown in the figure below is for a 1024-dot × 768-line XGA video signal divided into 9 points at 128-dot intervals in the horizontal direction and 7 points at 128-line intervals in the vertical direction. The relationship between the correction point coordinates (m, n) and the RAM address is obtained as follows.

RAM address = (m – 1) + (n – 1) × (Number of horizontal correction points)

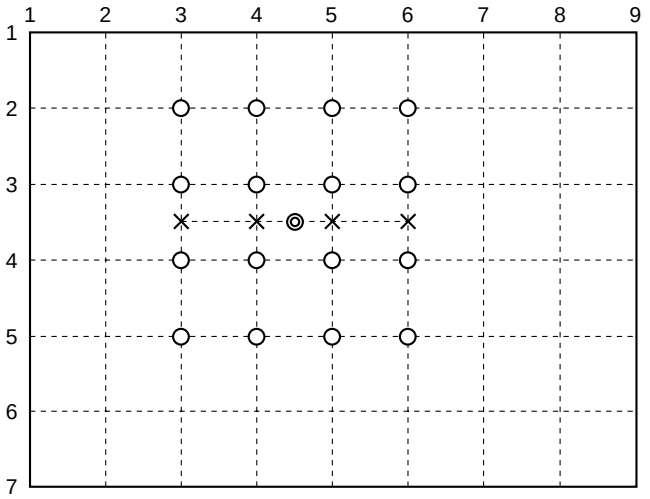
For the example in the figure below, this is as follows.

(9 – 1) + (7 – 1) × 9 = 62

Thus, the correction data must be set in the RAM from address 0 to address 62.
Up/down and/or right/left inversion of the LCD panel is supported by controlling the method of reading the correction data set in the RAM. Up/down and/or right/left inversion are set from DWN and RGT of the TG block. CSC_DWN and CSC_R (G, B)_RGT control the linking with the TG block settings.



Interpolation operations in the horizontal and vertical directions are performed using the 16 points of correction data (○ marks in the figure below) around the pixel to be corrected. First, interpolation operations are performed in the vertical direction using two upper and lower points of correction data at a time to obtain four data (× marks in the figure below). Next, interpolation operations are performed in the horizontal direction using these data to obtain the final correction data (◎ mark in the figure below).



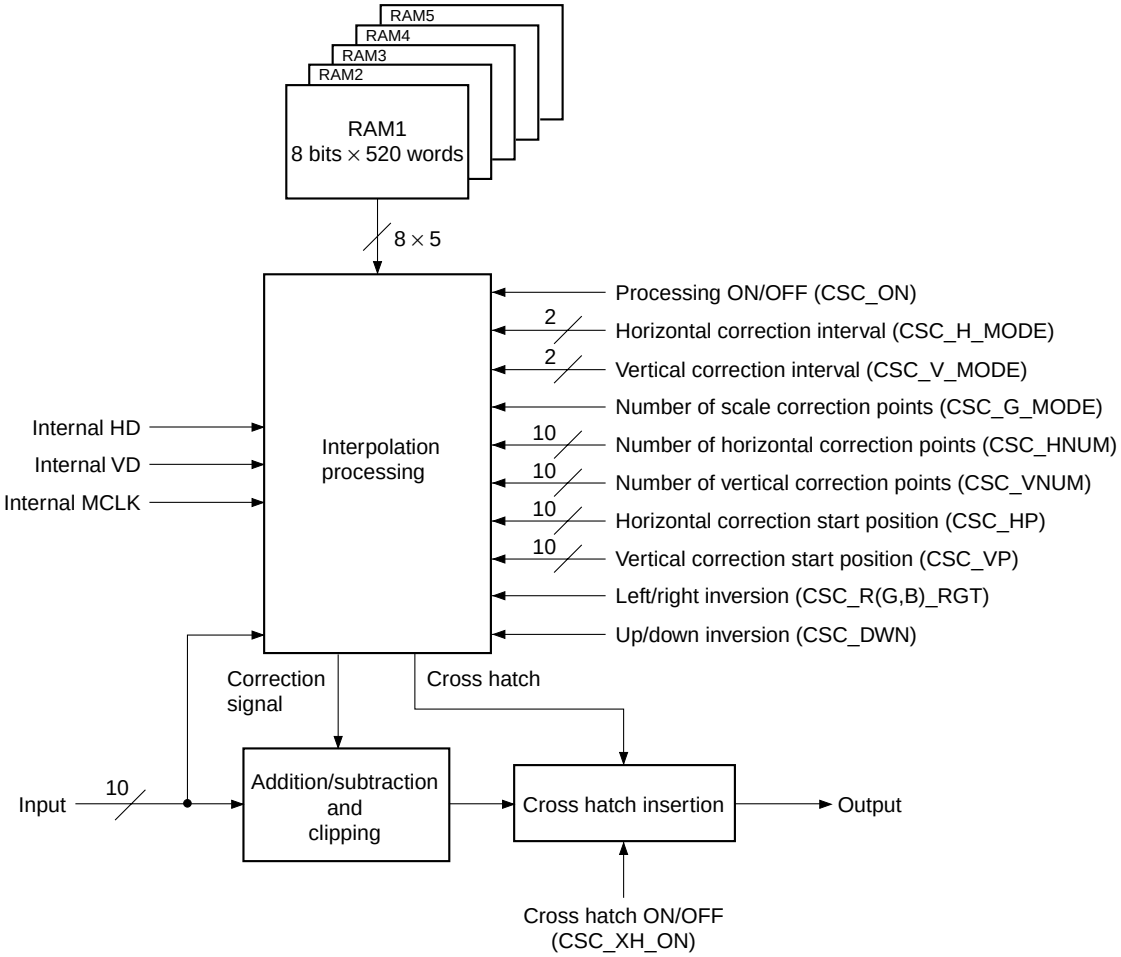
Interpolation operations in the scale direction are performed using the correction data in the five RAMs. When CSC_G_MODE = 1, interpolation operations are performed in the scale direction. There are 5 correction points in the scale direction. The data set in RAM1 to RAM5 is treated as each scale level correction data as shown in the table below, and interpolation operations are performed in the horizontal and vertical directions for each RAM. Then the four operation results (◎ mark in the figure above) for that same pixel (coordinates) are selected according to the scale level of the video signal input to the color shading correction block, and interpolation operations are performed in the scale direction. Thus, when interpolation operations are performed in the scale direction, the correction data for each pixel is obtained from a total 64 points of correction data.

When CSC_G_MODE = 0, correction operations are not performed in the scale direction, and the correction data calculated using the data set in RAM1 is reflected to all scales.

The calculated correction data is added to the video signal. If these operation results overflow or underflow, clipping is performed and 3FFh or 000h is output.

RAM name	Corresponding scale
RAM1	3FFh
RAM2	300h
RAM3	200h
RAM4	100h
RAM5	000h

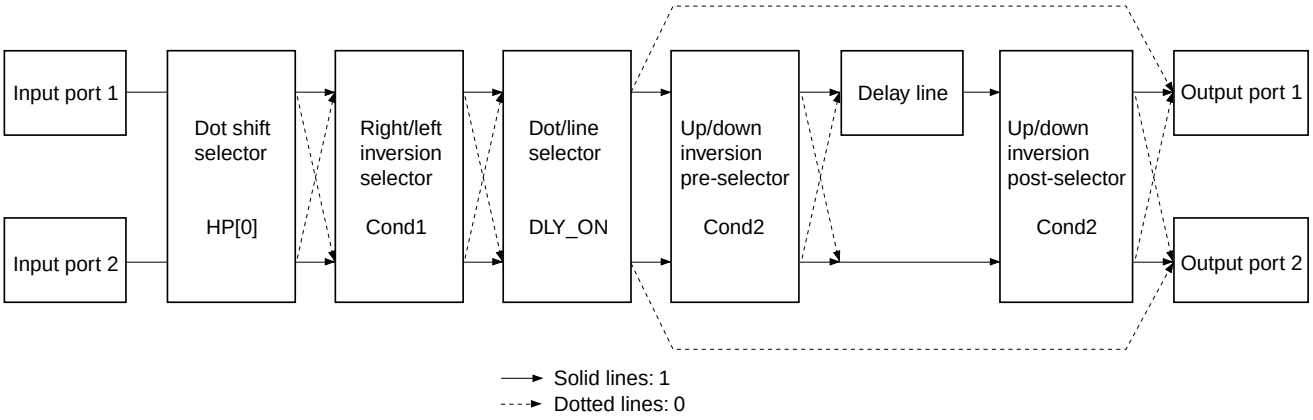
This block has a function for inserting the cross hatch that links the correction points into the video signal.
When CSC_XH_ON = 1, the cross hatch is inserted. The cross hatch level is 3FFh.
When CSC_XH_ON = 0, the cross hatch is not inserted.
The color shading correction block RAM output is undetermined during power-on. When performing color shading correction, be sure to set data in these RAMs. When performing color shading correction in only the horizontal and vertical directions, be sure to set CSC_ON = 1 before setting data in RAM1 of each color. When performing color shading correction in the scale direction in addition to the horizontal and vertical directions, set CSC_ON = 1 and CSC_G_MODE = 1 before setting data in RAM1 to RAM5 of each color. When CSC_ON = 0 and CSC_G_MODE = 0, the RAMs are in standby mode and data cannot be set.



(n) Selectable delay line block

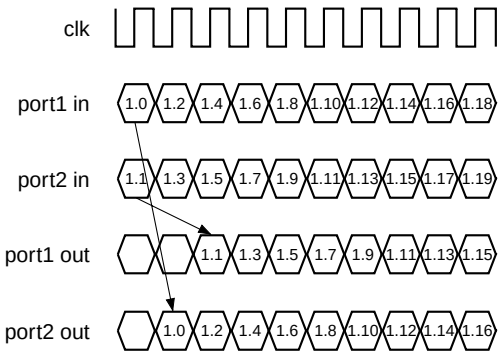
This block supports signal shifting in 1-dot units, performs signal port switching linked with right/left inversion and signal processing that supports dot/line inversion.
This block is comprised of five selectors: dot shift selector, right/left inversion selector, dot/line selector, up/down inversion pre-selector, and up/down inversion post-selector.
The delay line size is 1200 words.
The data paths for this block are shown in the figure below. Port switching during right/left inversion depends on the Cond1 value, and port switching during up/down inversion (when dot/line inversion support is ON) depends on the Cond2 value.

Cond1 = (RGT_SEL_ON) AND [(RGT) Ex-NOR (DLY_R (G, B)_RGT)]
Cond2 = (DWN) Ex-NOR (DLY_DWN)
Note) RGT and DWN are TG block settings.



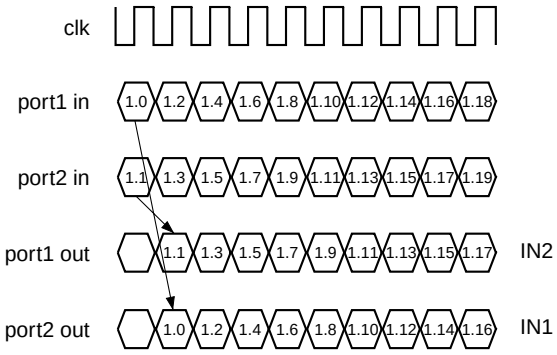
(1) 1-dot shift

When HP[0] = 0, the output data is delayed by one dot compared to when HP[0] = 1.



(2) Right/left inversion

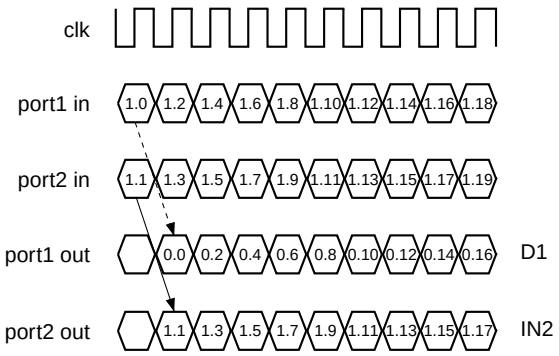
When Cond1 = 0, signal port switching is performed for the output data.



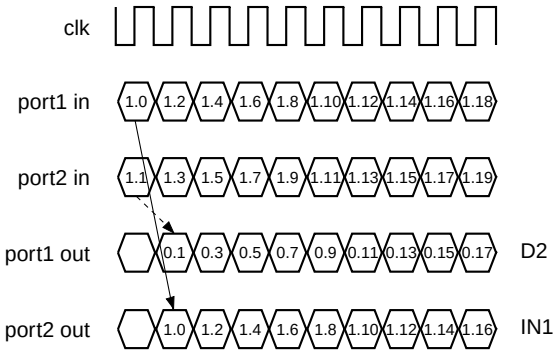
(3) Dot/line inversion support

When DLY_ON = 1, signal processing that supports dot/line inverted drive is performed. The output data is output as shown in the figures below according to the Cond1 and Cond2 values. D and the dotted lines in the figures indicate that the signal is delayed by 1H.

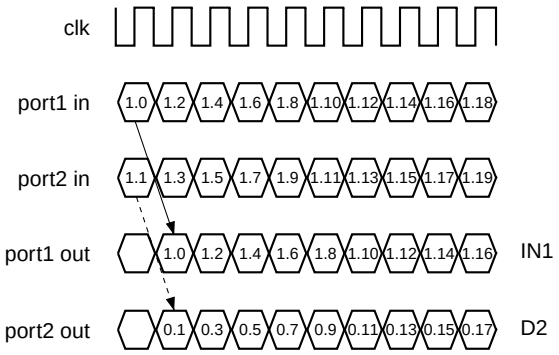
Cond1	Cond2
1	1



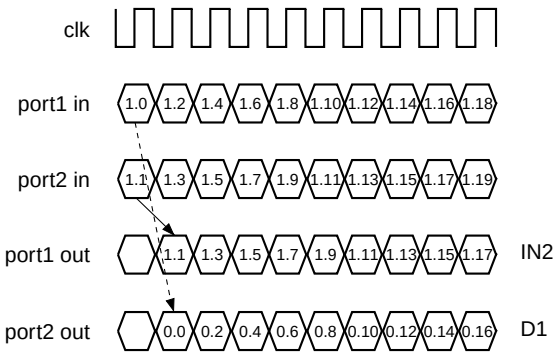
Cond1	Cond2
0	1



Cond1	Cond2
1	0



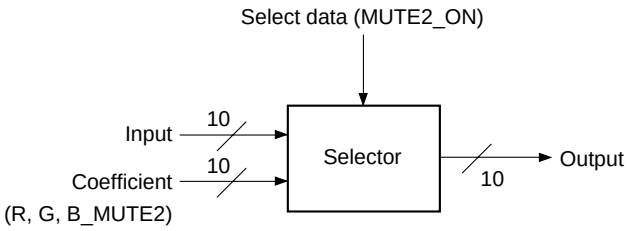
Cond1	Cond2
0	0



(o) Mute 2 block

This block performs mute processing by replacing the video signal with data of the desired level. The settings are as follows.

MUTE2_ON: 1 = Mute processing ON, 0 = OFF (Setting shared by R, G and B)
R, G, B_MUTE2: RGB mute data (Set independently for R, G and B)

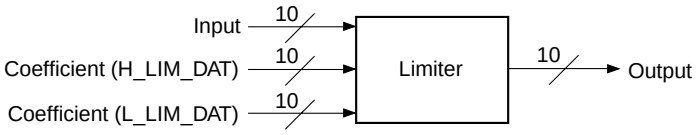


(p) Limiter block

This block performs limiter processing so that the output signal does not exceed a certain range. The settings are as follows.

L_LIM_DAT: Low side limiter level
When input data ≤ L_LIM_DAT, the output is clipped to L_LIM_DAT.
H_LIM_DAT: High side limiter level
When H_LIM_DAT ≤ input data, the output is clipped to H_LIM_DAT.
(Both settings shared by R, G and B)

Set data so that the relationship L_LIM_DAT < H_LIM_DAT is constantly maintained. When both coefficient values are 000h, limiter processing is not performed.

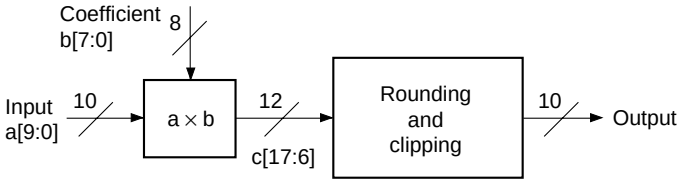


(q) Post gain block

This block performs multiplication processing independently for ports 1 and 2. The settings are as follows.

Coefficient: 8 bits
Gain setting: 0 to 1.9921875 (= 255/128) times, variable in 256 steps
(Set independently for R, G and B ports 1 and 2)

Multiplication is performed using the 10-bit input and an 8-bit coefficient, and the upper 12 bits c[17:6] of the operation results are output. Next, the c[6] value is checked and rounding is performed to 11 bits. The MSB of the rounded 11 bits is checked, clipping is performed, and the lower 10 bits are output.

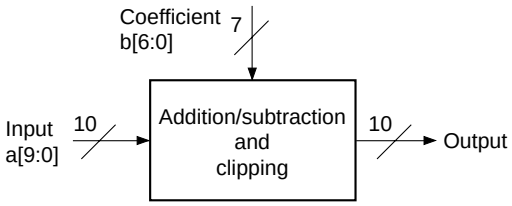


(r) Post bright block

This block performs addition and subtraction processing independently for ports 1 and 2. The settings are as follows.

Coefficient: 7 bits with code, MSB = code bit
Bright setting: –64 to +63 scales, variable with an accuracy of 1 bit
(Set independently for R, G and B ports 1 and 2)

Multiplication is performed using the 10-bit input and a 7-bit coefficient with code. The coefficient MSB is the code bit. Addition is performed when b[6] = 0, and subtraction when b[6] = 1. However, when performing subtraction, set the two's complement in the lower bits of the coefficient. When the operation results overflow or underflow, clipping is performed.



(s) Cycle offset block

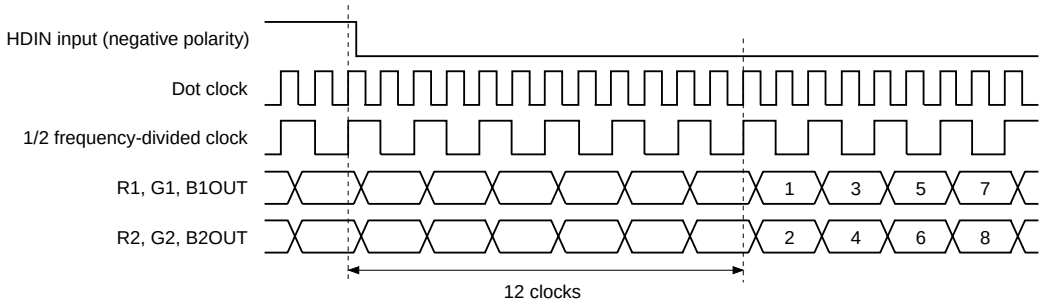
This block performs addition and subtraction processing independently for ports 1 and 2. Arithmetic coefficients are selected sequentially using the counter output value as the select signal. Therefore, a cyclic offset relative to the video signal can be attached. The settings are as follows.

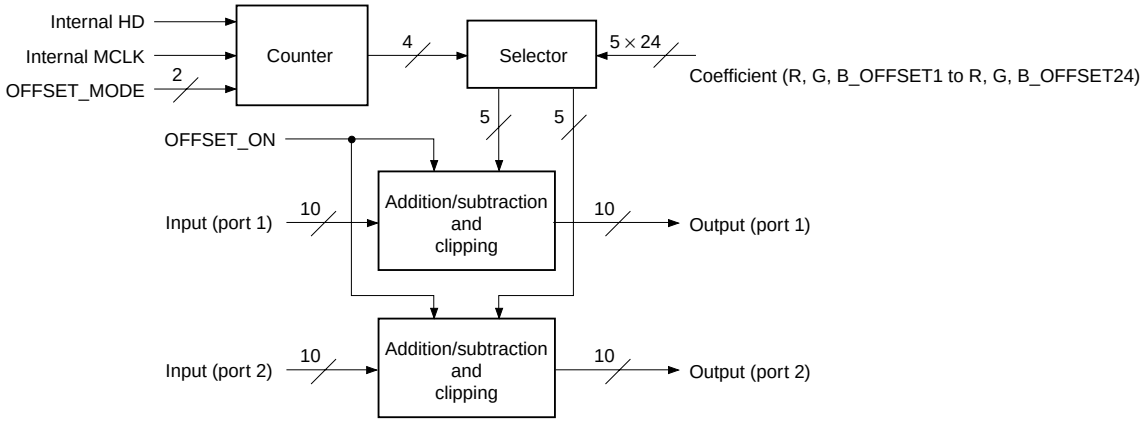
OFFSET_ON: 1 = Offset processing ON, 0 = OFF (Setting shared by R, G and B)
OFFSET_MODE: 0h = 6-dot period, 1h = 12-dot period, 2h = 24-dot period (Setting shared by R, G and B)
R, G, B_OFFSET1 to R, G, B_OFFSET24: 5-bit offset data with code
–16 to +15 scales, variable with an accuracy of 1 bit
(Set independently for R, G and B)

The coefficients selected according to the counter operating period are as shown in the table below. In all cases, the coefficients are assigned in ascending order from the smallest number. The coefficient MSB is the code bit. Addition is performed when MSB = 0, and subtraction when MSB = 1. However, when performing subtraction, set the two's complement in the lower bits of the coefficient. When the operation results overflow or underflow, clipping is performed.

Period	Coefficient number output from selector	
	Port 1 side	Port 2 side
6 dots	1, 3, 5	2, 4, 6
12 dots	1, 3, 5, 7, 9, 11	2, 4, 6, 8, 10, 12
24 dots	1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23	1, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24

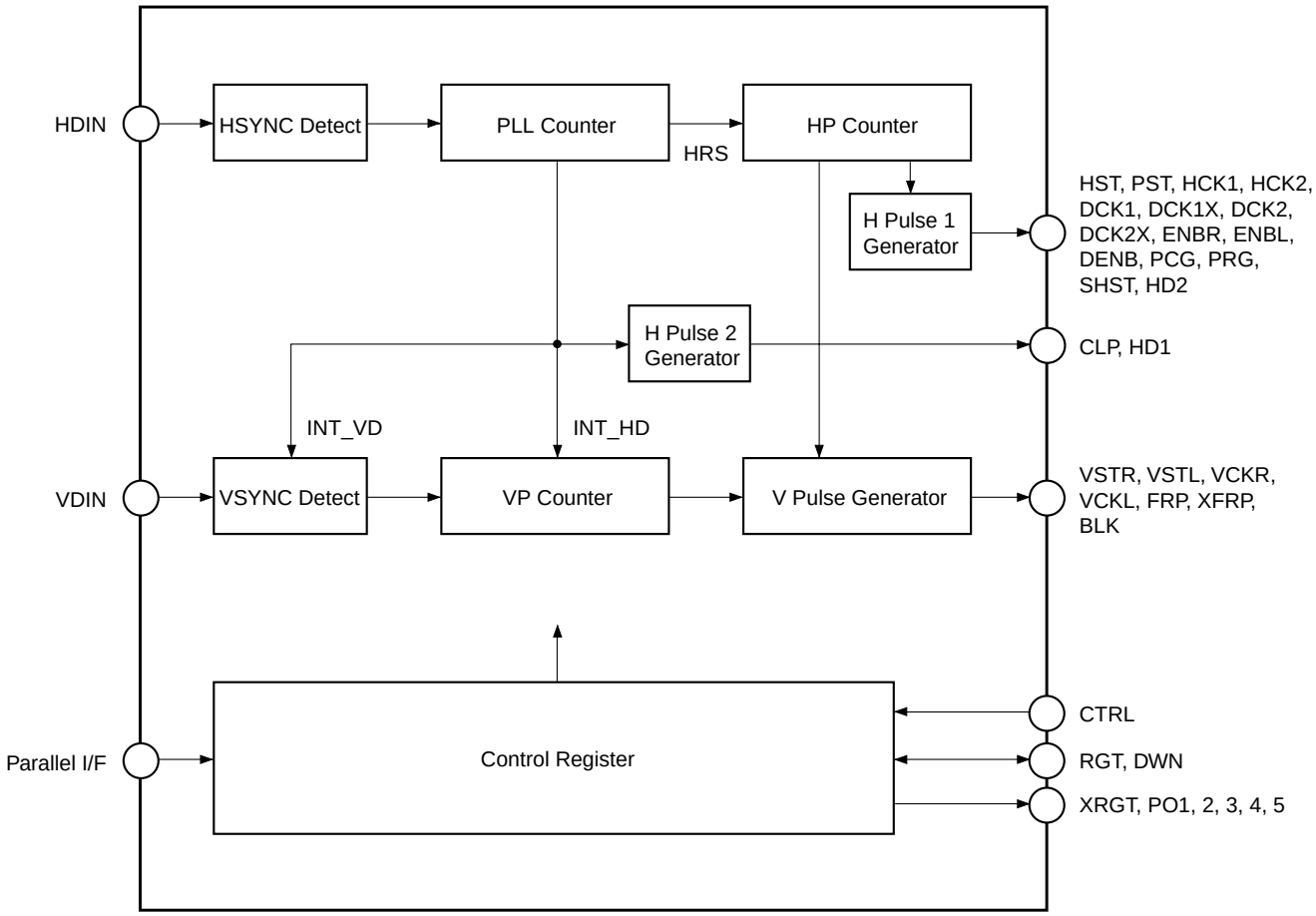
The counter reset timing is delayed by 12 dot clocks from the front edge of the HDIN input.





4. Timing Generator (TG) Block

This block generates the timing pulses required to drive Sony LCD panels. Of the output pulses, the required pulses differ according to the LCD panel type, so be sure to also check the specifications of the panel used. The output timing pulses are all set by the parallel I/F. For a detailed description, see the description of the parallel I/F TG block.
The TG block diagram is shown below.

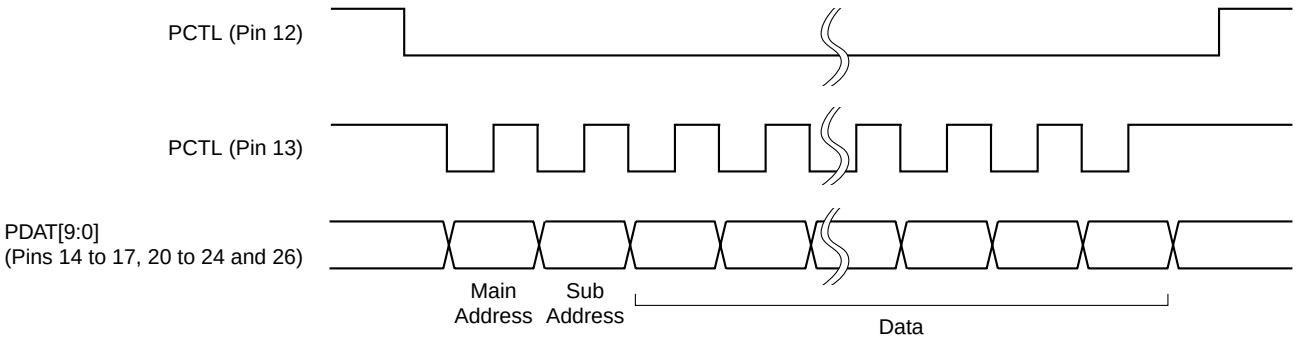


Timing Generator Block Diagram

5. Parallel I/F Block

Register data settings in this IC are performed by parallel data. As shown in the Timing Chart below, the parallel I/F comprises a total 12-bit wide bus consisting of control signal PCTL (Pin 12), clock signal PCLK (Pin 13) and 10-bit wide data signal PDAT[9:0] (Pins 14 to 17, 20 to 24 and 26).
The data signal is input in the order of main address, sub address and data. When setting data in this IC, divide the data into 22 blocks as shown in the table on the next page. Next, the sub address specifies the initial address of the data to be written in the block designated by the main address. The data is set sequentially from the data at the address designated by the sub address. The address of each data set thereafter is automatically incremented by +1 from the address designated by the sub address, so further address setting is unnecessary. This makes it possible to set only the necessary data from the desired address of the desired block.

(1) Timing chart



(2) Main address table

Main address	Set block
000h	TG block
001h	DSD1 block
002h	DSD2 block
003h	Gamma block (Red) RAM
004h	Gamma block (Green) RAM
005h	Gamma block (Blue) RAM
006h	Color shading correction block (Red) RAM1
007h	Color shading correction block (Red) RAM2
008h	Color shading correction block (Red) RAM3
009h	Color shading correction block (Red) RAM4
00Ah	Color shading correction block (Red) RAM5
00Bh	Color shading correction block (Green) RAM1
00Ch	Color shading correction block (Green) RAM2
00Dh	Color shading correction block (Green) RAM3
00Eh	Color shading correction block (Green) RAM4
00Fh	Color shading correction block (Green) RAM5
010h	Color shading correction block (Blue) RAM1
011h	Color shading correction block (Blue) RAM2
012h	Color shading correction block (Blue) RAM3
013h	Color shading correction block (Blue) RAM4
014h	Color shading correction block (Blue) RAM5
015h	Pattern generator block

5-1. TG Block (Main Address: 000h)

The TG block data format is as follows.

Sub address	Data										Initial value
	PDAT9	PDAT8	PDAT7	PDAT6	PDAT5	PDAT4	PDAT3	PDAT2	PDAT1	PDAT0	
000h	POLDET	CLKPOL	HR	RGT	DWN	PO5	PO4	PO3	PO2	PO1	000h
001h	—	HPOL	VPOL	DCKPOL	HSTPOL	HCKPOL	VSTPOL	VCKPOL	BLKPOL	BLKON	1FFh
002h	FRPM[1:0]		DCKFINV	DCKFIX	HSTFIX	HCKFIX	VSTFIX	VCKFIX	HSTM	PSTM	3FFh
003h	—	—	—	—	—	—	—	RGVLNK	FRVC1LNK	SLXBLK	000h
004h	VFRRN[10:2]									PLLP[11]	3FFh
005h	PLLP[10:1]										000h
006h	—	—	—	—	—	—	—	—	HP[11:10]		000h
007h	HP[9:0]										000h
008h	VP[9:0]										000h
009h	CLPU[10:1]										000h
00Ah	CLPD[10:1]										000h
00Bh	PRGU[10:1]										000h
00Ch	PRGD[10:1]										000h
00Dh	HD1U[10:1]										000h
00Eh	HD1D[10:1]										000h
00Fh	FRPP[10:1]										000h
010h	SHSTU[10:1]										000h
011h	SHSTD[10:1]										000h
012h	DENU[10:1]										000h
013h	DEND[10:1]										000h
014h	—	—	—	—	SHP[5:0]						000h
015h	—	—	HSTPC[7:0]								000h
016h	—	—	—	—	HSTPF[5:0]						000h
017h	—	—	PSTPC[7:0]								000h

Sub address	Data										Initial value
	PDAT9	PDAT8	PDAT7	PDAT6	PDAT5	PDAT4	PDAT3	PDAT2	PDAT1	PDAT0	
018h	—	—	—	—	PSTPF[5:0]						000h
019h	—	—	—	—	HCKC[5:0]						000h
01Ah	—	—	—	—	DCK1F[5:0]						000h
01Bh	—	—	—	—	DCK1W[5:0]						000h
01Ch	—	—	—	—	DCK2F[5:0]						000h
01Dh	—	—	—	—	DCK2W[5:0]						000h
01Eh	PCGU[10:1]										000h
01Fh	PDGD[10:1]										000h
020h	ENB1U[10:1]										000h
021h	ENB1D[10:1]										000h
022h	ENB2U[10:1]										000h
023h	ENB2D[10:1]										000h
024h	VCK1P[10:1]										000h
025h	VCK2P[10:1]										000h
026h	VST1P[11:2]										000h
027h	VST2P[11:2]										000h
028h	HD2U[10:1]										000h
029h	HD2D[10:1]										000h
02Ah	BLKU[10:1]										000h
02Bh	BLKD[10:1]										000h
02Ch	—	CLKOUT	HD1OE	HD2OE	CLPOE	PRGOE	SHSTOE	DENOE	FRPOE	XFRPOE	000h
02Dh	HSTOE	PSTOE	HCK1OE	HCK2OE	DCKOE	DCKXOE	V1OE	V2OE	PCGOE	BLKOE	000h

—: Don't care

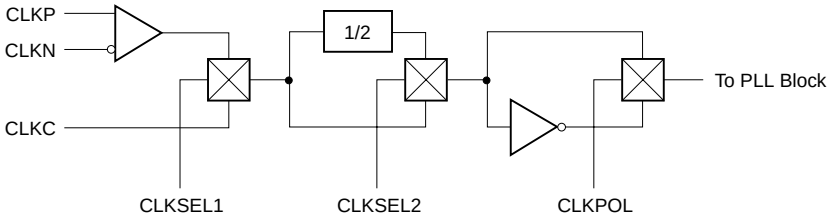
The detailed setting contents are described below.

(a) Clock settings

(1) CLKPOL (sub address: 000h)

This sets the internal clock polarity.
Setting value: 1 = Inverted, 0 = Not inverted

The clock flow from the clock input pins to the PLL block is shown below.



(2) CLKOUT (sub address: 02Ch)

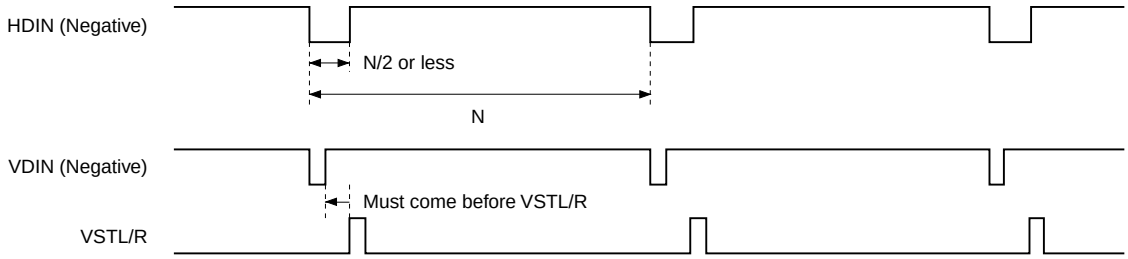
This sets the Pin 47 clock output limit.
Setting value: 1 = Inverted clock is output, 0 = Low is output

(b) SYNC polarity settings

(1) POLDET (sub address: 000h)

This sets the sync polarity auto discrimination function ON/OFF.
Setting value: 1 = Auto discrimination function ON, 0 = Auto discrimination function OFF

When POLDET = 1, the HPOL and VPOL settings below are invalid. When using this function, the HDIN sync portion must be 1/2 or less of 1H, and the VDIN sync portion must come before the rise position of the VSTL/R pulse.



(2) HPOL and VPOL (sub address: 001h)

These set the sync signal polarity when POLDET = 0.
Setting value: 1 = Positive polarity, 0 = Negative polarity

The internal operation of this IC is with the input sync signal fixed to positive polarity. Therefore, these HPOL and VPOL must be set in accordance with the polarity of the sync signal input from HDIN and VDIN.
Set HPOL and VPOL to "1" when the input sync signal is positive polarity, or to "0" when negative polarity.

(c) Dots per 1H and lines per 1F settings

(1) HR (sub address: 000h)

This sets the PLL counter reset ON/OFF.
Setting value: 1 = Reset enabled, 0 = Reset disabled

When HR = 0, the internal frequency divider is used, and the HD1 pulse output should be used as the return pulse. The number of dot clocks per 1H is set by PLLP[11:1] below.

(2) PLLP[11:1] (sub addresses: 004h and 005h)

This sets the internal PLL counter reset period in 11 bits. Setting is possible in 2-dot units. When the number of dot clocks per 1H is N, set the "(N – 2)/2" value.
When HR = 0, free-running occurs at the above N. When HR = 1, if the next HDIN is not input before the internal PLL counter counts up to 2047, free-running mode is established and free-running occurs at N.
When HDIN is input, free-running is canceled and normal operation is established.

(3) VFRRN[10:2] (sub address: 004h)

This sets the number of lines in 9 bits during vertical free running. Setting is possible in 4-line units. To have operation run freely at M lines, set the "(M – 4)/4" value. If the next VDIN is not input before the internal vertical line counter counts up to 2047, free-running mode is established. When VDIN is input, free-running is canceled and normal operation is established.

(d) Scan direction settings

RGT and DWN (sub address: 000h)

These settings switch the scan directions of the LCD panel.
Setting value: 1 = Forward scan, 0 = Reverse scan

When CTRL (Pin 148) is low, RGT (Pin 136) and DWN (Pin 147) function as output pins, and the data set in the respective registers is reflected. When CTRL is high, this setting is ignored, RGT and DWN function as input pins, and are reflected to internal operation.

(e) Register parallel output settings

PO1, PO2, PO3, PO4 and PO5 (sub address: 000h)

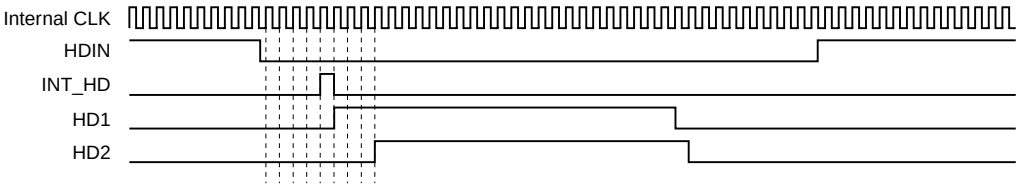
These set the register setting parallel output.
Setting value: 1 = High is output, 0 = Low is output

The set data is reflected to the output pins PO1 (Pin 154), PO2 (Pin 153), PO3 (Pin 152), PO4 (Pin 164) and PO5 (Pin 166) of the same name.

(f) Horizontal display position and horizontal direction pulse settings

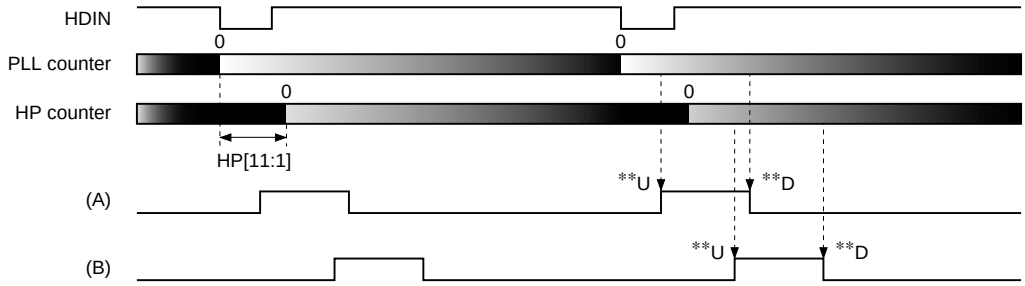
(1) HP[11:0] (sub addresses: 006h and 007h)

HP[11:1] sets the horizontal pulse position for the LCD panel in 11 bits. The position can be set in 2-dot units using the internal pulse INT_HD generated from the front edge of HDIN as the reference. The HP setting range is from "0 to (N – 2)".
If the HP value is set to the number of frequency divisions N or higher, the HP setting is ignored and "(N – 2)" is used as the setting value.
The HST, PST, HCK1, HCK2, DCK1, DCK1X, DCK2, DCK2X, ENBL, ENBR, VSTL, VSTR, VCKL, VCKR, FRP, XFRP, PCG, PRG, BLK and HD2 horizontal timing pulses are linked according to the HP setting.
The internal reference pulse INT_HD rises at the 5th clock from the front edge of the HDIN input, and all the pulses are synchronized using this as the reference. Increasing HP shifts the output positions of the linked pulses toward the rear of the time series. The example below shows the shortest output position from HDIN when HP is set to 000h. (Note that the output position changes according to the settings in (2) below.)
HP[0] can shift the video in 1-dot units. See 3. Description of DSD Block Signal Processing Functions, (n) Selectable delay line block, (1) 1-dot shift for a detailed description.



(2) CLPU[10:1], CLPD[10:1], PRGU[10:1], PRGD[10:1], HD1U[10:1], HD1D[10:1], SHSTU[10:1], SHSTD[10:1], DENU[10:1], DEND[10:1], PCGU[10:1], PCGD[10:1], ENB1U[10:1], ENB1D[10:1], ENB2U[10:1], ENB2D[10:1], HD2U[10:1], HD2D[10:1]
(sub addresses: 009h to 013h, 01Eh to 023h and 028h to 029h)

These set the horizontal timing pulse output positions in 10 bits. The respective rise and fall positions can be set in 2-dot units. Settings ending in "U" set the rise position, and settings ending in "D" set the fall position. Horizontal pulses are divided into the following two types.
(A) CLP and HD1 → Pulses synchronized to the PLL counter
Set the "(rise position/fall position – 10)/2" value.
(B) PRG, SHST, DEN, PCG, ENBL, ENBR and HD2 → Pulses synchronized to the HP counter
Set the "(rise position/fall position – HP setting value – 16)/2" value.
An outline of each type is shown below. When **U and **D are set to the same value, "1" is output.



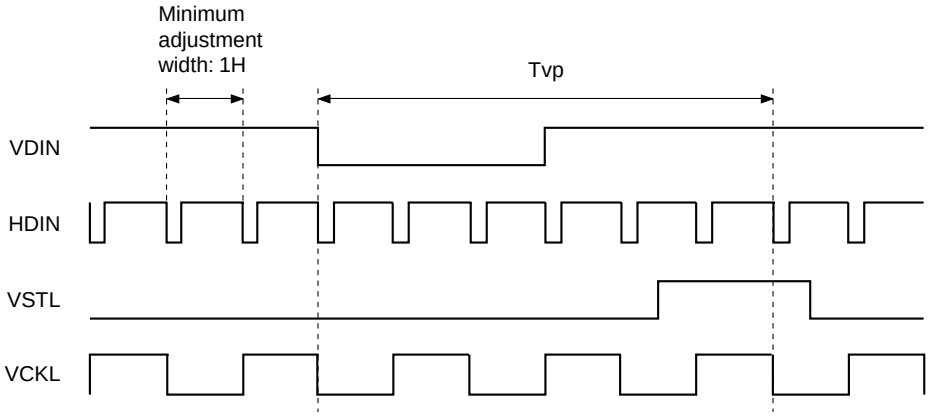
(3) HD1OE, HD2OE, CLPOE, PRGOE, SHSTOE, DENOE and PCGOE (sub addresses: 02Ch and 02Dh)

These set the HD1, HD2, CLP, PRG, SHST, DEN and PCG pulse output limits, respectively.
Setting value: 1 = Pulse is output, 0 = Output is fixed to "0"

(g) Vertical display position setting

VP[9:0] (sub address: 008h)

This sets the vertical display start position in 10 bits. The position can be set in 1-line units using the front edge of VDIN as the reference. The VSTL/VSTR, VCKL/VCKR, FRP and XFRP pulse phases change by linking with this setting.



Tvp minimum and maximum setting values

	Min.	Max.
VP[9:0]	000h	3FFh
Tvp	6H	1029H

(h) HST and PST pulse settings

(1) HSTM (sub address: 002h)

This sets the pulse width for horizontal display start timing pulse HST.

Setting value: 1 = Twice the HCK period width, 0 = HCK period width

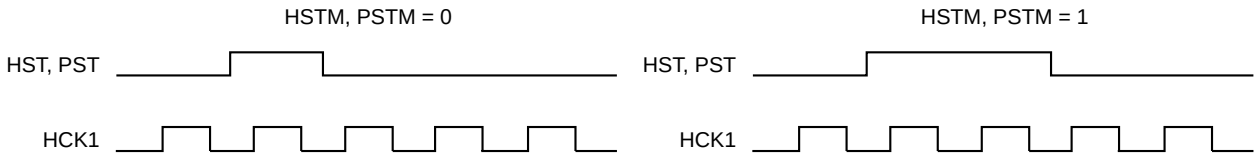
Set the width according to the LCD panel specifications.

(2) PSTM (sub address: 002h)

This sets the pulse width for dot sequential precharge start timing pulse PST.

Setting value: 1 = Twice the HCK period width, 0 = HCK period width

Set the width according to the LCD panel specifications.



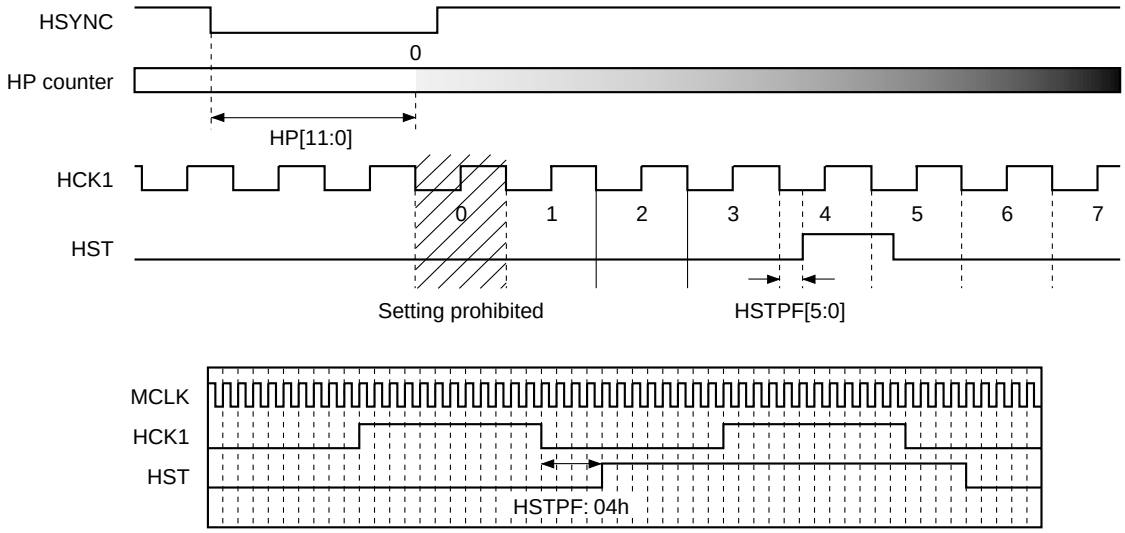
(3) HSTFIX and HSTPOL (sub addresses: 001h and 002h)

These set the HST and PST pulse output polarities. The polarity changes as follows according to the combination of linked/not linked with control signal RGT. This setting is shared by HST and PST.

HSTFIX	HSTPOL	RGT	Output polarity
0	0	0	Positive
0	0	1	Negative
0	1	0	Negative
0	1	1	Positive
1	0	0	Negative
1	0	1	Negative
1	1	0	Positive
1	1	1	Positive

(4) HSTPC[7:0], HSTPF[5:0], PSTPC[7:0] and PSTPF[5:0] (sub addresses: 015h to 018h)

These set the HST and PST pulse phases. Reset is applied when the internal HP counter reaches "0", and the HST and PST pulse phases within 1H can be set at the HCK1 and HCK2 period, respectively, by HSTPC and PSTPC.
HSTPF and PSTPF can set the HST and PST pulse phase relative to HCK1 and HCK2 in 1-dot units.
Do not set HSTPC and PSTPC to 00h, as the pulses may not be output correctly in this case.
The HSTPF and PSTPF values can be set up to "(HCKC × 2 – 2)". If higher values are set, the pulses are not output. Set the "(phase difference from HCK pulse)" value.
The figures below show the timings for HSTPC: 04h and HSTPF: 04h, respectively. These timings are the same for the PST pulse.



(5) HSTOE and PSTOE (sub address: 02Dh)

These set the HST and PST pulse output limits, respectively.

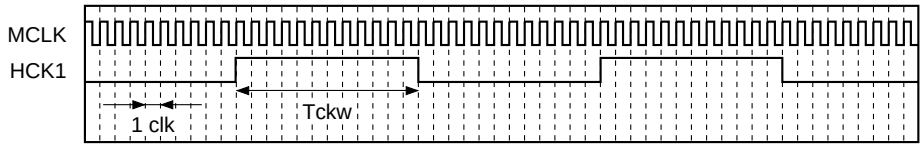
Setting value: 1 = Pulse is output, 0 = Output is fixed to "0"

(i) HCK1 and HCK2 pulse settings

(1) HCKC[5:0] (sub address: 019h)

This sets the HCK1 and HCK2 period (LCD panel sampling period). Settings which result in an odd number for Tckw in the figure below are prohibited, so be sure to set a value that results in an even number. Set the "(Tckw – 1)" value according to the LCD panel specifications. When this setting is changed, the HST and PST pulse phases also change, so first set HCKC to the correct value and then make the HST and PST settings. Example setting values are shown in the table below.

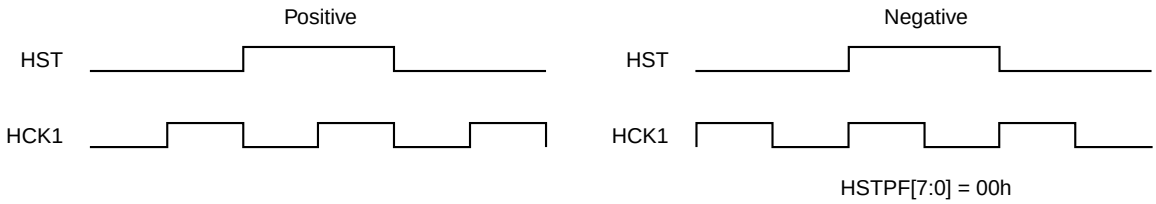
LCD panel	Tckw	HCKC setting
SVGA, WXGA	6 clk	05h
XGA, SXGA	12 clk	0Bh
UXGA	24 clk	17h



(2) HCKFIX and HCKPOL (sub addresses: 001h and 002h)

These set the HCK pulse output polarity. The polarity relative to the HST pulse changes as follows according to the combination of linked/not linked with control signal RGT.

HCKFIX	HCKPOL	RGT	Output polarity
L	L	L	Positive
L	L	H	Negative
L	H	L	Negative
L	H	H	Positive
H	L	L	Negative
H	L	H	Negative
H	H	L	Positive
H	H	H	Positive



(3) HCK1OE and HCK2OE (sub address: 02Dh)

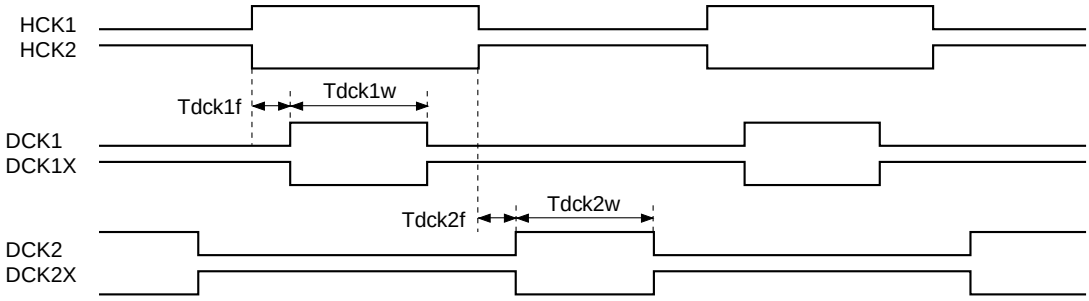
These set the HCK1 and HCK2 pulse output limits, respectively.

Setting value: 1 = Pulse is output, 0 = Output is fixed to "0"

(j) DCK1, DCK1X, DCK2 and DCK2X pulse settings

(1) DCK1F[5:0], DCK1W[5:0], DCK2F[5:0] and DCK2W[5:0] (sub addresses: 01Ah to 01Dh)

These set the DCK1, DCK1X, DCK2 and DCK2X pulse phases and widths. DCK1F sets the DCK1 and DCK1X pulse phases relative to HCK1 and HCK2 in 1-dot units, and DCK2F sets the DCK2 and DCK2X pulse phases relative to HCK1 and HCK2 in 1-dot units. Set the "Tdck1 (2) f" value.
The DCKFINV, DCKFIX and RGT settings differ according to whether the phase is synchronized with the rising edge of HCK1 or HCK2.
The DCK1 and DCK1X pulse width and the DCK2 and DCK2X pulse width can be set in 2-dot units by DCK1W and DCK2W, respectively. Set the "(Tdck1 (2) W – 2)/2" value.



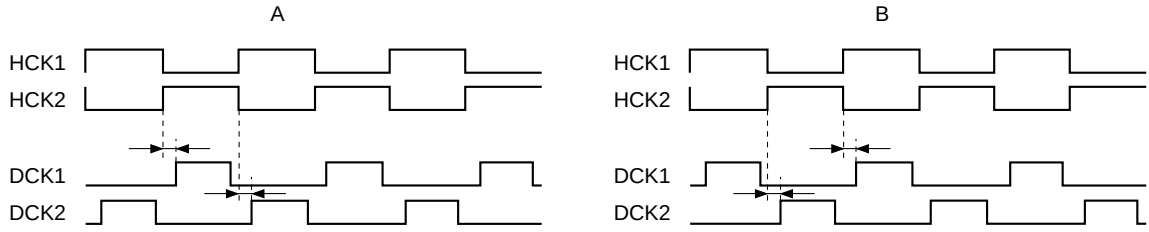
(2) DCKPOL (sub address: 001h)

This setting switches the DCK1 and DCK1X, DCK2 and DCK2X output polarities. Switching this setting, inverts the polarities each pair of DCK1 and DCK1X, DCK2 and DCK2X at once.

(3) DCKFINV and DCKFIX (sub address: 002h)

This setting switches the DCK1, DCK1X, DCK2 and DCK2X output phases relative to HCK1 and HCK2. The phase changes as follows according to the combination of linked/not linked with right/left inversion control signal RGT.

DCKFIX	DCKFINV	RGT	Output phase
0	0	0	A
0	0	1	B
0	1	0	B
0	1	1	A
1	0	0	B
1	0	1	B
1	1	0	A
1	1	1	A



(4) DCKOE (sub address: 02Dh)

This sets the output limit of DCK1 and DCK2 pulses.

Setting value: 1 = DCK1 and DCK2 pulses are output, 0 = Output is fixed to "0"

(5) DCKXOE (sub address: 02Dh)

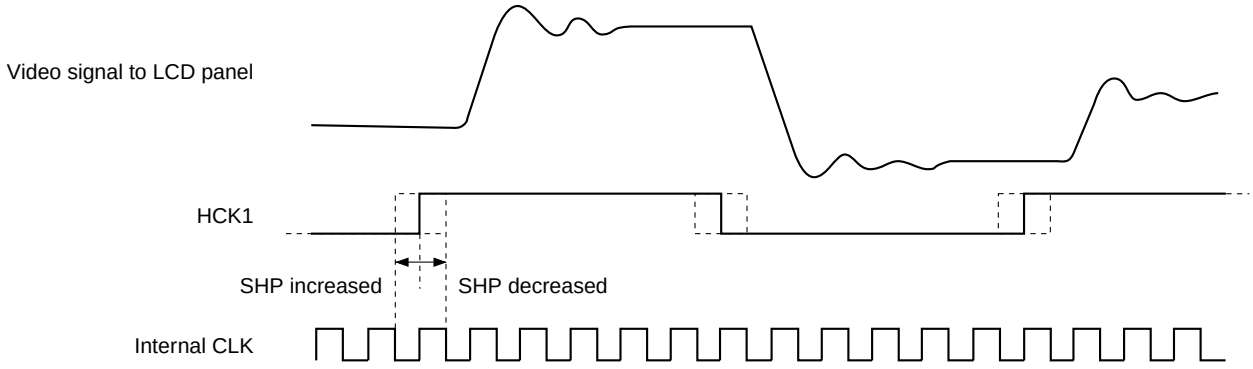
This sets the output limit of DCK1X and DCK2X pulses.

Setting value: 1 = DCK1X and DCK2X pulses are output, 0 = Output is fixed to "0"

(k) LCD panel sample-and-hold position setting

SHP[5:0] (sub address: 014h)

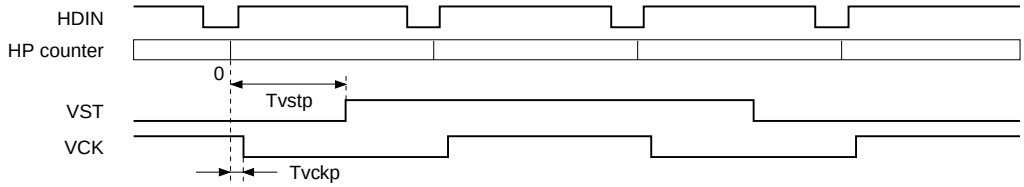
This sets the horizontal transfer start pulse and clock pulse phases relative to the video signal to the LCD panel. The phase can be set in 64 positions with 6 bits. Incrementing SHP by +1 shifts the HST, PST, HCK1, HCK2, DCK1, DCK1X, DCK2 and DCK2X pulses forward by 1 dot (half the internal clock period). The LCD panel sample-and-hold position can be set by shifting the above pulse phases forward or backward relative to the video signal. At this time, the phases between the HST, PST, HCK1, HCK2, DCK1, DCK1X, DCK2 and DCK2X pulses does not change. The figure below shows an example of HCK1 during 12-dot simultaneous sampling.
This setting eliminates the need to set the sample-and-hold position with a Sony sample-and-hold driver IC (CXA3512R, CXA3562R), and makes it possible to adjust the phases of the video signal to the LCD panel and the horizontal transfer clock without changing the position of the video signal on the screen.



(l) VST and VCK pulse settings

(1) VST1P[11:2] and VST2P[11:2] (sub addresses: 026h to 027h)

These set the VSTL and VSTR pulse rise and fall positions within 1H in 10 bits. The position can be set in 4-dot units using the internal HP counter "0" position as the reference. Set the "(Tvstp – 4)/4" value.
See the FRVC1LNK, RGVLNK and RGT settings hereafter to determine which of the VST1P or VST2P settings is reflected to VSTL or VSTR.



(2) VCK1P[10:1] and VCK2P[10:1] (sub addresses: 024h to 025h)

These set the VCKL, VCKR, FRP and XFRP inversion positions within 1H in 10 bits. The inversion positions can be set in 2-dot units using the internal HP counter "0" position as the reference. Set the "(Tvckp – 2)/2" value.
See the FRVC1LNK, RGVLNK and RGT settings hereafter to determine which of the VCK1P, VCK2P or FRPP settings is reflected to VCKL or VCKR.

(3) VSTFIX and VCKFIX (sub address: 002h), VSTPOL and VCKPOL (sub address: 001h)

These set the VST and VCK pulse output polarities. The VSTL and VSTR pulse polarities and the VCKL and VCKR pulse polarities relative to the VSTL and VSTR pulses change as follows according to the combination of linked/not linked with control signal DWN.

***FIX	***POL	DWN	Output polarity
0	0	0	Positive
0	0	1	Negative
0	1	0	Negative
0	1	1	Positive
1	0	0	Negative
1	0	1	Negative
1	1	0	Positive
1	1	1	Positive

***: VST or VCK

(4) V1OE (sub address: 02Dh)

This sets the output limit of VSTL, VCKL and ENBL pulses.
Setting value: 1 = VSTL, VCKL and ENBL pulses are output, 0 = Output is fixed to "0"

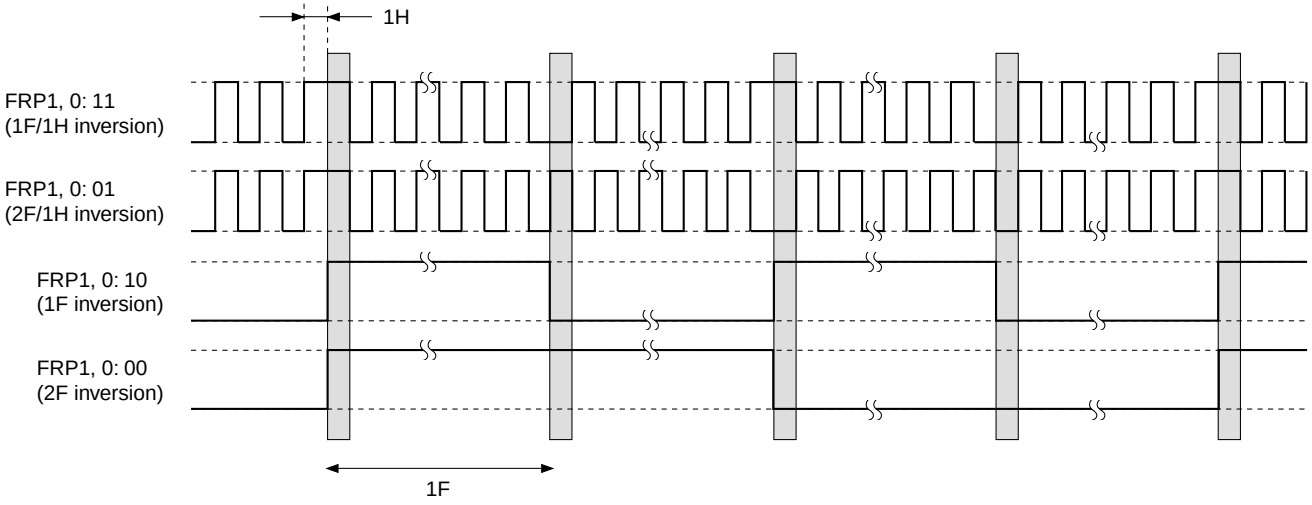
(5) V2OE (sub address: 02Dh)

This sets the output limit of VSTR, VCKR and ENBR pulses.
Setting value: 1 = VSTR, VCKR and ENBR pulses are output, 0 = Output is fixed to "0"

(m) FRP and XFRP pulse settings

(1) FRPM[1:0] (sub address: 002h)

This sets the period for switching the LCD AC conversion signal FRP pulse. 1F/1H, 2F/1H, 1F and 2F inversion can be set as shown in the figure below. Normally use FRP1, 0: 11.



(2) FRPP[10:1] (sub address: 00Fh)

This sets the FRP and XFRP inversion positions within 1H in 10 bits. The inversion positions can be set in 2-dot units using the internal HP counter "0" position as the reference. Set the "(FRP inversion position – HP counter "0" position – 2)/2" value.
XFRP is output as the polarity inverted FRP pulse.

(3) FRPOE and XFRPOE (sub address: 02Ch)

These set the FRP and XFRP pulse output limits, respectively.
Setting value: 1 = Pulse is output, 0 = Output is fixed to "0"

(n) VCK and FRP transition point shared setting and V block pulse right/left inversion link setting

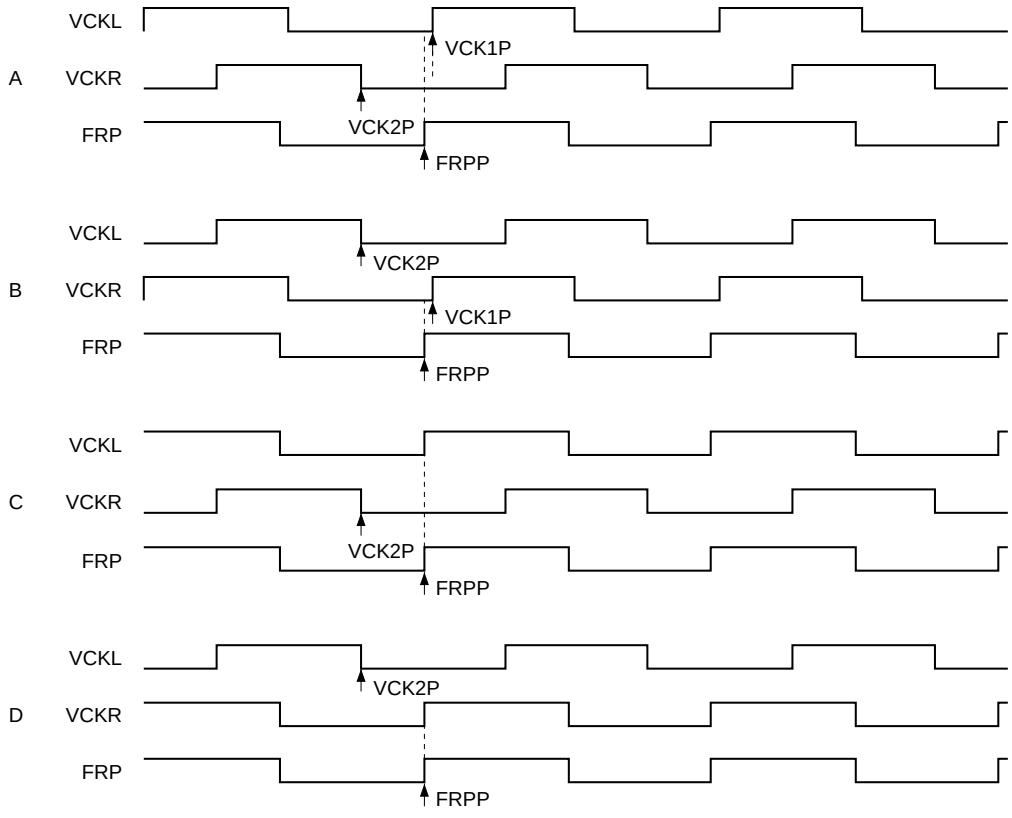
FRVC1LNK and RGVLNK (sub address: 003h)

These set the VCKL and VCKR transition points

Setting value: 1 = FRP and VCK transition points are shared,
0 = FRP and VCK transition points are independent

When FRVC1LNK = 1, the VCK inversion timing is forcibly synchronized with the FRP inversion timing. At this time, which of VCKL or VCKR is linked with the FRP transition point is as follows.
When FRVC1LNK = 0, the VCKL and VCKR transition points are determined by VCK1P[10:1] or VCK2P[10:1] according to the RGT setting. When RGVLNK = 1, the V block pulses, VSTL, VCKL and ENBL are switched with VSTR, VCKR and ENBR, respectively, linked with right/left inversion control signal RGT. When RGVLNK = 0, the V block pulses are fixed regardless of the RGT setting. See the following page for a detailed description.

FRVC1LNK	RGVLNK	RGT	Output waveform
0	0	0	A
0	0	1	A
0	1	0	B
0	1	1	A
1	0	0	C
1	0	1	C
1	1	0	D
1	1	1	C



(o) V scanner pulse scan direction link setting

RGVLNK (sub address: 003h)

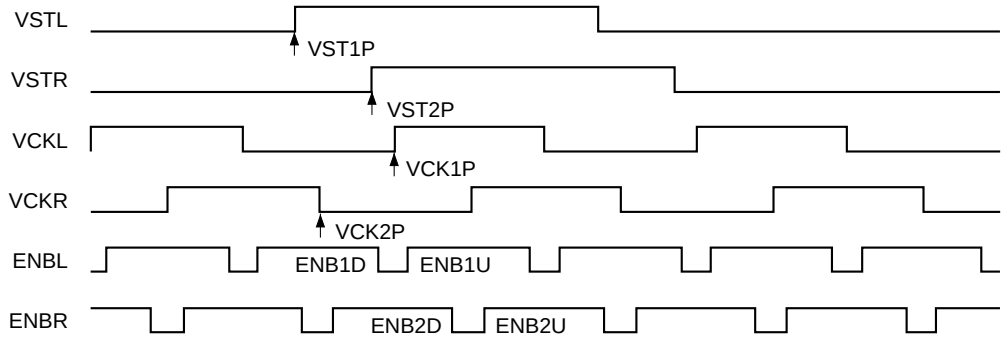
This sets whether to link the V block pulses, VSTL, VSTR, VCKL, VCKR, ENBL and ENBR with the right/left inversion control signal RGT.

Setting value: 1 = Linked with RGT, 0 = Independent of RGT

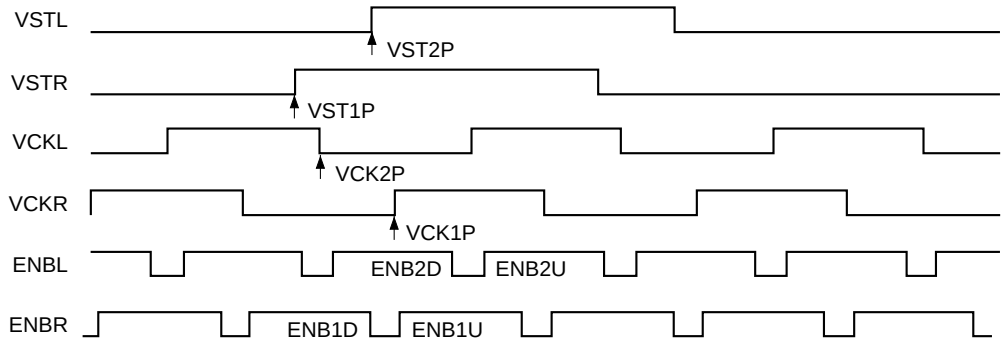
When RGVLNK = 1, rise and fall positions of VSTL and VSTR, ENBL and ENBR pulses and inversion position of VCKL and VCKR pulses are changed respectively by linking with RGT. When RGVLNK = 0, VSTL, VCKL and ENBL are set by VST1P, VCK1P, ENB1U and ENB1D, respectively, and VSTR, VCKR and ENBR are set by VST2P, VCK2P, ENB2U and ENB2D, respectively, independent of the RGT setting.

RGVLNK	RGT	Output waveform
0	0	A
0	1	A
1	0	B
1	1	A

A



B



(p) BLK pulse settings

(1) BLKON (sub address: 001h)

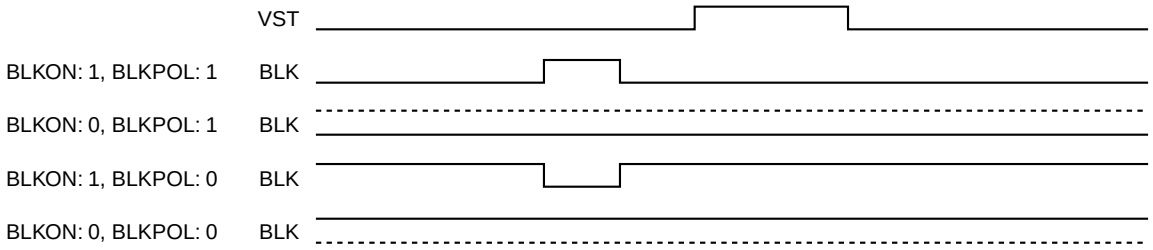
This sets the black frame write pulse BLK ON/OFF.
Setting value: 1 = Pulse is output, 0 = DC is output

When BLKON = 1, BLK is output as a single pulse in 1V.

(2) BLKPOL (sub address: 001h)

This sets the black frame write pulse BLK polarity.
Setting value: 1 = Positive polarity, 0 = Negative polarity

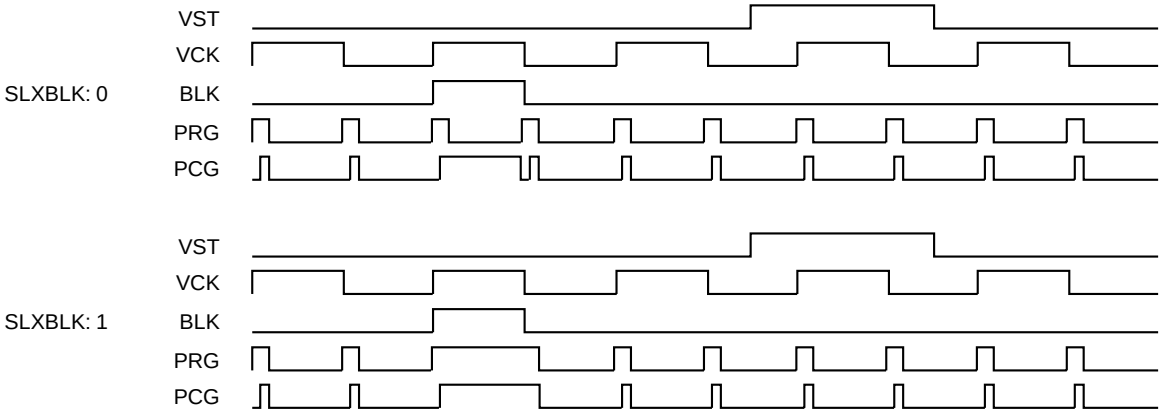
Set BLKPOL = 1 for a Sony SVGA panel, and BLKPOL = 0 for an XGA panel.



(3) SLXBLK (sub address: 003h)

This sets the precharge waveform top/bottom black frame display mode.
Setting value: 1 = XGA type, 0 = Other than XGA type

Set SLXBLK = 1 only when using top/bottom black frame display mode on a Sony XGA type LCD panel. Set SLXBLK = 0 in all other cases.



(4) BLKU[10:1] and BLKD[10:1] (sub addresses: 02Ah to 02Bh)

These set the BLK pulse rise and fall positions within 1H in 10 bits. The positions can be set in 2-dot units using the internal HP counter "0" position as the reference. Set the "(BLK rise/fall position – HP counter "0" position – 2)/2" value.

(5) BLKOE (sub address: 02Dh)

This is the BLK pulse output limit setting.

Setting value: 1 = Pulse is output, 0 = Output is fixed to "0"

5-2. DSD1 Block (Main Address: 001h)

The DSD1 block data format is as follows.

Sub address	Data										Initial value
	PDAT9	PDAT8	PDAT7	PDAT6	PDAT5	PDAT4	PDAT3	PDAT2	PDAT1	PDAT0	
000h	—	R_DAT_SW	R1_PRE_GAIN[7:0]								000h
001h	—	—	—	—	—	R1_PRE_BRT[4:0]					000h
002h	—	—	R2_PRE_GAIN[7:0]								000h
003h	—	—	—	—	—	R2_PRE_BRT[4:0]					000h
004h	—	G_DAT_SW	G1_PRE_GAIN[7:0]								000h
005h	—	—	—	—	—	G1_PRE_BRT[4:0]					000h
006h	—	—	G2_PRE_GAIN[7:0]								000h
007h	—	—	—	—	—	G2_PRE_BRT[4:0]					000h
008h	—	B_DAT_SW	B1_PRE_GAIN[7:0]								000h
009h	—	—	—	—	—	B1_PRE_BRT[4:0]					000h
00Ah	—	—	B2_PRE_GAIN[7:0]								000h
00Bh	—	—	MUTE1_ON	GAM_SEL	GAM_ON	B2_PRE_BRT[4:0]					000h
00Ch	—	USER_BRT[10]	USER_GAIN[7:0]								000h
00Dh	USER_BRT[9:0]										000h
00Eh	—	R_SUB_BRT[10]	R_SUB_GAIN[7:0]								000h
00Fh	R_SUB_BRT[9:0]										000h
010h	—	G_SUB_BRT[10]	G_SUB_GAIN[7:0]								000h
011h	G_SUB_BRT[9:0]										000h
012h	—	B_SUB_BRT[10]	B_SUB_GAIN[7:0]								000h
013h	B_SUB_BRT[9:0]										000h
014h	R_MUTE1[9:0]										000h
015h	G_MUTE1[9:0]										000h
016h	B_MUTE1[9:0]										000h
017h	R_OSD_DAT1[9:0]										000h
018h	R_OSD_DAT2[9:0]										000h

Sub address	Data										Initial value
	PDAT9	PDAT8	PDAT7	PDAT6	PDAT5	PDAT4	PDAT3	PDAT2	PDAT1	PDAT0	
019h	R_OSD_DAT3[9:0]										000h
01Ah	R_OSD_DAT4[9:0]										000h
01Bh	G_OSD_DAT1[9:0]										000h
01Ch	G_OSD_DAT2[9:0]										000h
01Dh	G_OSD_DAT3[9:0]										000h
01Eh	G_OSD_DAT4[9:0]										000h
01Fh	B_OSD_DAT1[9:0]										000h
020h	B_OSD_DAT2[9:0]										000h
021h	B_OSD_DAT3[9:0]										000h
022h	B_OSD_DAT4[9:0]										000h
023h	R_MUTE2[9:0]										000h
024h	G_MUTE2[9:0]										000h
025h	B_MUTE2[9:0]										000h
026h	L_LIM_DAT[9:0]										000h
027h	H_LIM_DAT[9:0]										000h
028h	—	MUTE2_ON	R1_POST_GAIN[7:0]								000h
029h	—	—	—	R1_POST_BRT[6:0]							000h
02Ah	—	—	R2_POST_GAIN[7:0]								000h
02Bh	—	—	—	R2_POST_BRT[6:0]							000h
02Ch	—	—	G1_POST_GAIN[7:0]								000h
02Dh	—	—	—	G1_POST_BRT[6:0]							000h
02Eh	—	—	G2_POST_GAIN[7:0]								000h
02Fh	—	—	—	G2_POST_BRT[6:0]							000h
030h	—	—	B1_POST_GAIN[7:0]								000h
031h	—	—	—	B1_POST_BRT[6:0]							000h
032h	—	—	B2_POST_GAIN[7:0]								000h
033h	—	—	—	B2_POST_BRT[6:0]							000h

—: Don't care

The detailed setting contents are described below.

(a) R_DAT_SW, G_DAT_SW and B_DAT_SW (sub addresses: 000h, 004h and 008h)

These select the data path switch block data path.
Setting value: 1 = Data path is switched, 0 = Data path is not switched

(b) R1_PRE_GAIN[7:0], R2_PRE_GAIN[7:0], G1_PRE_GAIN[7:0], G2_PRE_GAIN[7:0], B1_PRE_GAIN[7:0] and B2_PRE_GAIN[7:0] (sub addresses: 000h, 002h, 004h, 006h, 008h and 00Ah)

These set the pre gain block arithmetic coefficients in 8 bits.

(c) R1_PRE_BRT[4:0], R2_PRE_BRT[4:0], G1_PRE_BRT[4:0], G2_PRE_BRT[4:0], B1_PRE_BRT[4:0] and B2_PRE_BRT[4:0] (sub addresses: 001h, 003h, 005h, 007h, 009h and 00Bh)

These set the pre bright block arithmetic coefficients in 5 bits with code.

(d) USER_GAIN[7:0] (sub address: 00Ch)

This sets the user gain block arithmetic coefficients in 8 bits.

(e) USER_BRT[10:0] (sub addresses: 00Ch and 00Dh)

This sets the user bright block arithmetic coefficients in 11 bits with code.

(f) R_SUB_GAIN[7:0], G_SUB_GAIN[7:0] and B_SUB_GAIN[7:0] (sub addresses: 00Eh, 010h and 012h)

These set the R, G and B sub gain block arithmetic coefficients in 8 bits.

(g) R_SUB_BRT[10:0], G_SUB_BRT[10:0] and B_SUB_BRT[10:0] (sub addresses: 00Eh to 013h)

These set the R, G and B sub bright block arithmetic coefficients in 11 bits with code.

(h) MUTE1_ON (sub address: 00Bh)

This selects mute 1 block processing ON/OFF.
Setting value: 1 = Mute processing ON, 0 = OFF

(i) R_MUTE1[9:0], G_MUTE1[9:0] and B_MUTE1[9:0] (sub addresses: 014h to 016h)

These set the mute 1 block data in 10 bits.

(j) R_OSD_DAT1 to 4[9:0], G_OSD_DAT1 to 4[9:0] and B_OSD_DAT1 to 4[9:0] (sub addresses: 014h to 022h)

These set the OSD block decode data in 10 bits.

(k) GAM_SEL (sub address: 00Bh)

This selects the gamma block data path.
Setting value: 1 = Path passing through the RAM, 0 = Path not passing through the RAM

(l) GAM_ON (sub address: 00Bh)

This sets the gamma block RAM operating mode.
Setting value: 1 = Normal operation, 0 = Standby mode

Note that in standby mode, data cannot be written to or read from the RAM. Also, previously set data is held even when the RAM is set to standby mode.

(m) L_LIM_DAT[9:0] and H_LIM_DAT[9:0] (sub addresses: 026h and 027h)

This sets the limiter block limit value data in 10 bits.
Be sure to maintain the relationship L_LIM_DAT < H_LIM_DAT. Note that when both coefficients are set to 000h, limiter processing is not performed.

(n) MUTE2_ON (sub address: 028h)

This selects mute 2 block processing ON/OFF.
Setting value: 1 = Mute processing ON, 0 = OFF

(o) R_MUTE2[9:0], G_MUTE2[9:0] and B_MUTE2[9:0] (sub addresses: 023h to 025h)

These set the mute 2 block data in 10 bits.

(p) R1_POST_GAIN[7:0], R2_POST_GAIN[7:0], G1_POST_GAIN[7:0], G2_POST_GAIN[7:0], B1_POST_GAIN[7:0] and B2_POST_GAIN[7:0] (sub addresses: 028h, 02Ah, 02Ch, 02Eh, 030h and 032h)

These set the post gain block arithmetic coefficients in 8 bits.

(q) R1_POST_BRT[6:0], R2_POST_BRT[6:0], G1_POST_BRT[6:0], G2_POST_BRT[6:0], B1_POST_BRT[6:0] and B2_POST_BRT[6:0] (sub addresses: 029h, 02Bh, 02Dh, 02Fh, 031h and 033h)

These set the post bright block arithmetic coefficients in 7 bits with code.

5-3. DSD2 Block (Main Address: 002h)

The DSD2 block data format is as follows.

Sub address	Data										Initial value
	PDAT9	PDAT8	PDAT7	PDAT6	PDAT5	PDAT4	PDAT3	PDAT2	PDAT1	PDAT0	
000h	FRM_DAT[9:0]										000h
001h	FRM_H1[9:0]										000h
002h	FRM_H2[9:0]										000h
003h	FRM_V1[9:0]										000h
004h	FRM_V2[9:0]										000h
005h	—	—	CSC_XH_ON	FRM_ON	FRM_V1[10]	FRM_V2[10]	FRM_H1[11:10]		FRM_H2[11:10]		000h
006h	CSC_ON	CSC_G_MODE	CSC_V_MODE[1:0]		CCS_H_MODE[1:0]		CSC_DWN	CSC_B_RGT	CSC_G_RGT	CSC_R_RGT	000h
007h	CSC_HP[10:1]										000h
008h	CSC_VP[9:0]										000h
009h	CSC_HNUM[9:0]										000h
00Ah	CSC_VNUM[9:0]										000h
00Bh	—	OFFSET_ON	OFFSET_MODE[1:0]		RGT_SEL_ON	DLY_ON	DLY_DWN	DLY_B_RGT	DLY_G_RGT	DLY_R_RGT	000h
00Ch	R_OFFSET2[4:0]					R_OFFSET1[4:0]					000h
00Dh	R_OFFSET4[4:0]					R_OFFSET3[4:0]					000h
00Eh	R_OFFSET6[4:0]					R_OFFSET5[4:0]					000h
00Fh	R_OFFSET8[4:0]					R_OFFSET7[4:0]					000h
010h	R_OFFSET10[4:0]					R_OFFSET9[4:0]					000h
011h	R_OFFSET12[4:0]					R_OFFSET11[4:0]					000h
012h	R_OFFSET14[4:0]					R_OFFSET13[4:0]					000h
013h	R_OFFSET16[4:0]					R_OFFSET15[4:0]					000h
014h	R_OFFSET18[4:0]					R_OFFSET17[4:0]					000h
015h	R_OFFSET20[4:0]					R_OFFSET19[4:0]					000h
016h	R_OFFSET22[4:0]					R_OFFSET21[4:0]					000h
017h	R_OFFSET24[4:0]					R_OFFSET23[4:0]					000h

Sub address	Data										Initial value
	PDAT9	PDAT8	PDAT7	PDAT6	PDAT5	PDAT4	PDAT3	PDAT2	PDAT1	PDAT0	
018h	G_OFFSET2[4:0]					G_OFFSET1[4:0]					000h
019h	G_OFFSET4[4:0]					G_OFFSET3[4:0]					000h
01Ah	G_OFFSET6[4:0]					G_OFFSET5[4:0]					000h
01Bh	G_OFFSET8[4:0]					G_OFFSET7[4:0]					000h
01Ch	G_OFFSET10[4:0]					G_OFFSET9[4:0]					000h
01Dh	G_OFFSET12[4:0]					G_OFFSET11[4:0]					000h
01Eh	G_OFFSET14[4:0]					G_OFFSET13[4:0]					000h
01Fh	G_OFFSET16[4:0]					G_OFFSET15[4:0]					000h
020h	G_OFFSET18[4:0]					G_OFFSET17[4:0]					000h
021h	G_OFFSET20[4:0]					G_OFFSET19[4:0]					000h
022h	G_OFFSET22[4:0]					G_OFFSET21[4:0]					000h
023h	G_OFFSET24[4:0]					G_OFFSET23[4:0]					000h
024h	B_OFFSET2[4:0]					B_OFFSET1[4:0]					000h
025h	B_OFFSET4[4:0]					B_OFFSET3[4:0]					000h
026h	B_OFFSET6[4:0]					B_OFFSET5[4:0]					000h
027h	B_OFFSET8[4:0]					B_OFFSET7[4:0]					000h
028h	B_OFFSET10[4:0]					B_OFFSET9[4:0]					000h
029h	B_OFFSET12[4:0]					B_OFFSET11[4:0]					000h
02Ah	B_OFFSET14[4:0]					B_OFFSET13[4:0]					000h
02Bh	B_OFFSET16[4:0]					B_OFFSET15[4:0]					000h
02Ch	B_OFFSET18[4:0]					B_OFFSET17[4:0]					000h
02Dh	B_OFFSET20[4:0]					B_OFFSET19[4:0]					000h
02Eh	B_OFFSET22[4:0]					B_OFFSET21[4:0]					000h
02Fh	B_OFFSET24[4:0]					B_OFFSET23[4:0]					000h

—: Don't care

The detailed setting contents are described below.

(a) FRM_DAT[9:0] (sub address: 000h)

This sets the black frame level for the black frame block in 10 bits.

(b) FRM_ON (sub address: 005h)

This sets black frame display ON/OFF for the black frame block.

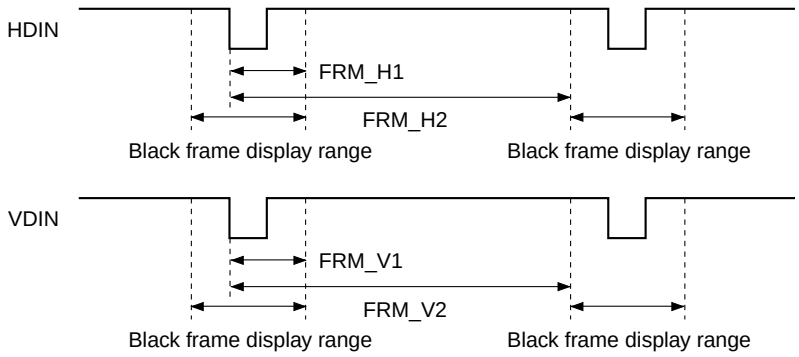
Setting value: 1 = ON, 0 = OFF

(c) FRM_H1[11:0] and FRM_H2[11:0] (sub addresses: 001h, 002h and 005h)

These set the horizontal black frame display range for the black frame block in 12 bits. The range can be set in 1-dot units using the front edge of the HDIN input as the reference. Set the "display range" value.

(d) FRM_V1[10:0] and FRM_V2[10:0] (sub addresses: 003h to 005h)

These set the vertical black frame display range for the black frame block in 11 bits. The range can be set in 1-line units using the front edge of the VDIN input as the reference. Set the "display range – 3" value.



(e) CSC_ON (sub address: 006h)

This sets color shading correction processing ON/OFF for the color shading correction block.

Setting value: 1 = ON, 0 = OFF

(f) CSC_H_MODE[1:0] (sub address: 006h)

This sets the horizontal correction point interval for the color shading correction of the color shading correction block.

Setting value: 0h = 32-dot interval, 1h = 64-dot interval, 2h = 128-dot interval

(g) CSC_V_MODE[1:0] (sub address: 006h)

This sets the vertical correction point interval for the color shading correction of the color shading correction block.

Setting value: 0h = 32-line interval, 1h = 64-line interval, 2h = 128-line interval

(h) CSC_G_MODE (sub address: 006h)

This sets the scale correction ON/OFF for the color shading correction of the color shading correction block.

Setting value: 1 = Scale correction ON, 0 = OFF

(i) CSC_R_RGT, CSC_G_RGT and CSC_B_RGT (sub address: 006h)

These set the right/left inversion for the color shading correction block.

Setting value: 1 = Reflects the TG block RGT setting, 0 = Reflects the inverse of TG block RGT setting

(j) CSC_DWN (sub address: 006h)

This sets the up/down inversion for the color shading correction block.

Setting value: 1 = Reflects the TG block DWN setting, 0 = Reflects the inverse of TG block DWN setting

(k) CSC_HP[10:1] (sub address: 007h)

This sets the horizontal correction start position for the color shading correction block in 10 bits. The position can be set in 2-dot units using the front edge of the HDIN input as the reference. Set the "(correction start position – 4)/2" value.

(l) CSC_VP[9:0] (sub address: 008h)

This sets the vertical correction start position for the color shading correction block in 10 bits. The position can be set in 1-line units using the front edge of the VDIN input as the reference. Set the "correction start position – 3" value.

(m) CSC_HNUM[9:0] and CSC_VNUM[9:0] (sub addresses: 009h and 00Ah)

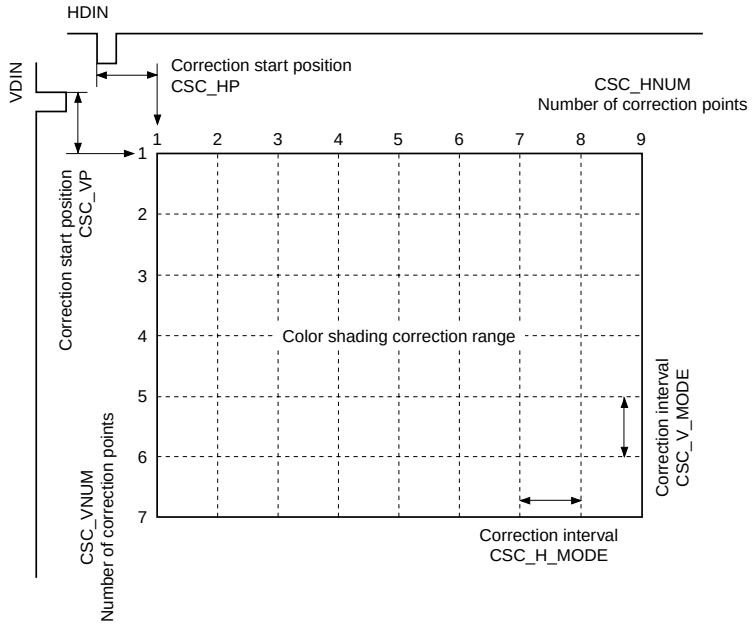
These set the number of horizontal and vertical correction points for the color shading correction block in 10 bits. Set the "(number of correction points – 1)" value. The size of the RAM for setting the correction data is 520 words, so set the number of correction points as follows.

Number of horizontal correction points × Number of vertical correction points ≤ 520

(n) CSC_XH_ON (sub address: 005h)

This sets the cross hatch display ON/OFF for the color shading correction block.

Setting value: 1 = Displayed, 0 = Not displayed



(o) RGT_SEL_ON, DLY_ON, DLY_DWN, DLY_R_RGT, DLY_G_RGT and DLY_B_RGT (sub address: 00Bh)

These are the selectable delay line block settings.

RGT_SEL_ON: This sets ON/OFF for port switching linked with left/right inversion.
Setting value: 1 = ON, 0 = OFF

DLY_ON: This sets the dot/line inverted drive support ON/OFF.
Setting value: 1 = ON, 0 = OFF

DLY_DWN: This sets the up/down inversion for the selectable delay line block.
Setting value: 1 = Reflects the TG block DWN setting,
0 = Reflects the inverse of the TG block DWN setting

DLY_R_RGT, DLY_G_RGT and DLY_B_RGT: These set the right/left inversion for the selectable delay line block.
Setting value: 1 = Reflects the TG block RGT setting,
0 = Reflects the inverse of the TG block RGT setting

The initial value is 0h for all settings.

(p) OFFSET_ON (sub address: 00Bh)

This sets the offset processing ON/OFF for the cycle offset block.
Setting value: 1 = ON, 0 = OFF

(q) OFFSET_MODE[1:0] (sub address: 00Bh)

This sets the offset cycle for the cycle offset block.
Setting value: 0h = 6-dot cycle, 1h = 12-dot cycle, 2h = 24-dot cycle

(r) R_OFFSET1 to 24, G_OFFSET1 to 24 and B_OFFSET1 to 24 (sub addresses: 00Ch to 02Fh)

These set the offset data for the cycle offset block in 5 bits with code.

5-4. Gamma Block RAM (Main Address: 003h to 005h)

In the gamma block, the gamma correction data is set in a 10-bit × 1024-word RAM. Here, the set sub address directly becomes the RAM write address. Thereafter, the RAM write address is automatically incremented by +1. Following the main address, designate the RAM write start address in the sub address with 10 bits, then set the gamma correction data in PDAT[9:0] with 10 bits. Note that GAM_ON of the DSD1 block should be set to "1" before setting data in the RAM.

5-5. Color Shading Correction Block RAM (Main Address: 006h to 014h)

In the color shading correction block, the color shading correction data is set in an 8-bit × 520-word RAM. Here, the set sub address directly becomes the RAM write address. Thereafter, the RAM write address is automatically incremented by +1. Following the main address, designate the RAM write start address in the sub address with 10 bits, then set the color shading correction data in PDAT[7:0] with 8 bits. Note that CSC_ON and CSC_G_MODE of the DSD2 block should be set to "1" before setting data in the RAM.

5-6. Pattern Generator Block (Main Address: 015h)

The pattern generator block data format is as follows.

Sub address	Data										Initial value
	PDAT9	PDAT8	PDAT7	PDAT6	PDAT5	PDAT4	PDAT3	PDAT2	PDAT1	PDAT0	
000h	PG_ON	PG_R_ON	PG_G_ON	PG_B_ON	PG_R_SEL	PG_G_SEL	PG_B_SEL	PG_PAT[2:0]			000h
001h	PG_STRP_SW	PG_STAIR_SW	PG_HST[11]	PG_HSTP[11]	PG_HWST[11]	PG_HWSTP[11]	PG_VST[10]	PG_VSTP[10]	PG_VWST[11]	PG_VWSTP[11]	000h
002h	PG_HST[10:1]										000h
003h	PG_HSTP[10:1]										000h
004h	PG_HWST[10:1]										000h
005h	PG_HWSTP[10:1]										000h
006h	PG_VST[9:0]										000h
007h	PG_VSTP[9:0]										000h
008h	PG_VWST[9:0]										000h
009h	PG_VWSTP[9:0]										000h
00Ah	—	PG_STEP[9:1]									000h
00Bh	PG_WIDTH[9:0]										000h
00Ch	PG_SIG1R[9:0]										000h
00Dh	PG_SIG2R[9:0]										000h
00Eh	PG_SIG1G[9:0]										000h
00Fh	PG_SIG2G[9:0]										000h
010h	PG_SIG1B[9:0]										000h
011h	PG_SIG2B[9:0]										000h

—: Don't care

The detailed setting contents are described below.

(a) PG_ON (sub address: 000h)

This sets the test signal output ON/OFF.
Setting value: 1 = Test pattern output mode enabled, 0 = Normal signal output

(b) PG_R (G, B)_ON (sub address: 000h)

These set the test signal level setting ON/OFF.
Setting value: 1 = Various settings enabled, 0 = Output fixed to "0"

(c) PG_R (G, B)_SEL (sub address: 000h)

These switch the pattern and non-pattern signal levels within the effective area.
Setting value: 1 = Pattern signal level is PG_SIG1R (G, B), 0 = Pattern signal level is PG_SIG2R (G, B)

(d) PG_PAT[2:0] (sub address: 000h)

This switches the display pattern within the window area.
Setting value: See the table below.

0	Raster
1	Window
2	Vertical stripe/diagonal stripe
3	Horizontal stripe
4	Cross hatch
5	Dot
6	Horizontal ramp/horizontal stair
7	Vertical ramp/vertical stair

(e) PG_STRP_SW (sub address: 001h)
(Valid only when PG_PAT[2:0] = 2h)

This switches between vertical stripe and diagonal stripe.
Setting value: 1 = Diagonal stripe, 0 = Vertical stripe

(f) PG_STAIR_SW (sub address: 001h)
(Valid only when PG_PAT[2:0] = 6h or 7h)

This switches between ramp and stair.
Setting value: 1 = Stair, 0 = Ramp

(g) PG_HST[11:1] (sub addresses: 001h and 002h)
PG_HSTP[11:1] (sub addresses: 001h and 003h)

These set the horizontal effective area in 11 bits. The area can be set in 2-dot units using the front edge of the HDIN input as the reference. Set the "(set point – 50)/2" value.

(h) PG_HWST[11:1] (sub addresses: 001h and 004h)
PG_HWSTP[11:1] (sub addresses: 001h and 005h)

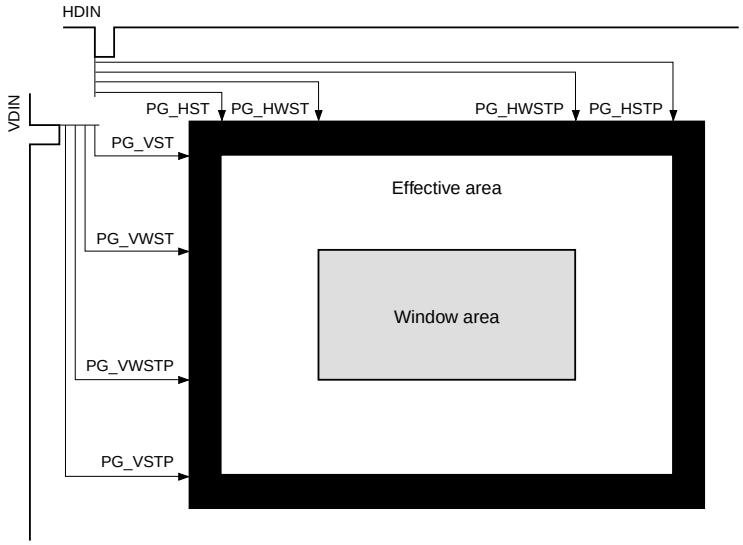
These set the horizontal window area in 11 bits. The area can be set in 2-dot units using the front edge of the HDIN input as the reference. Set the "(set point – 52)/2" value.

(i) PG_VST[10:0] (sub addresses: 001h and 006h)
PG_VSTP[10:0] (sub addresses: 001h and 007h)

These set the vertical effective area in 11 bits. The area can be set in 1-line units using the front edge of the VDIN input as the reference. Set the "set point – 3" value.

(j) PG_VWST[10:0] (sub addresses: 001h and 008h)
PG_VWSTP[10:0] (sub addresses: 001h and 009h)

These set the vertical window area in 11 bits. The area can be set in 1-line units using the front edge of the VDIN input as the reference. Set the "set point – 4" value.



(k) PG_STEP[9:1] (sub address: 00Ah)
(Valid for PG_PAT[2:0] = 2h, 3h, 4h, and 5h)

This sets the vertical stripe, diagonal stripe, horizontal stripe, cross hatch and dot period in 9 bits. The period can be set in 2-dot units. Set the "(period – 2)/2" value.

(l) PG_WIDTH[9:0] (sub address: 00Bh)
(Valid for PG_PAT[2:0] = 2h, 3h, 4h, and 5h)

This sets the vertical stripe, diagonal stripe, horizontal stripe, cross hatch and dot line width in 10 bits. The width can be set in 1-dot units. Set the "width" value.

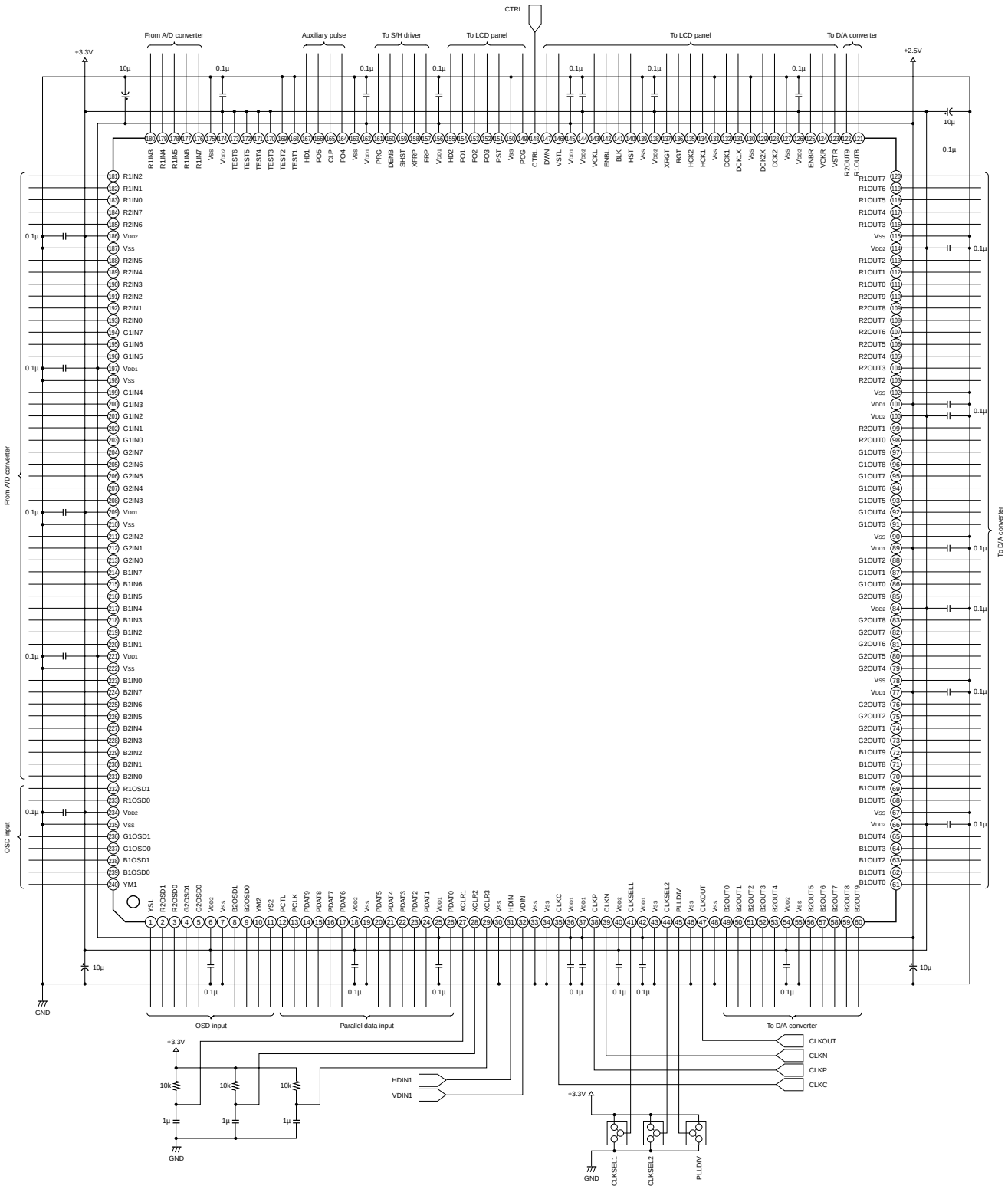
(m) PG_SIG1R (G, B)[9:0] and PG_SIG2R (G, B)[9:0] (sub addresses: 00Ch to 011h)

These set the output signal level inside and outside the pattern area within the effective area in 10 bits. The level can be set with an accuracy of 1 bit.

Notes on Handling

- The power supply and GND patterns have a large effect on undesired radiation on the substrate and interference to analog circuits, etc. General precautions are as follows.
    - Make the GND pattern as wide as possible. Using a multi-layer substrate and a solid ground is recommended.
    - Connect each power supply pin to GND via a ceramic chip capacitor of 0.1µF or more located as close to each pin as possible.
- Do not use this IC under conditions other than the recommended operating conditions.
- Absolute maximum rating values should not be exceeded even momentarily. Exceeding ratings may damage the device, leading to eventual breakdown.
- This IC has a MOS structure which is easily damaged by static electricity, so thorough measures should be taken to prevent electrostatic discharge.
- Since this IC utilizes a MOS structure, it may latch up due to excessive noise or power surge greater than the maximum rating of the I/O pins, interface with two power supplies of another circuit, or the order in which power is supplied to circuits. Make a thorough study of measures against the possibility of latch up before use.
- When the initialization of this IC is performed at power-on, system clear cancellation is performed after the supply voltage is set in the range of the recommended operating conditions and stabilized. Keep in mind that the internal circuit may not be initialized correctly if system clear cancellation is performed before the supply voltage is set in the range of the recommended operating conditions.
- When designing the substrate, take sufficient care for the surrounding temperature and heat radiation, and make sure the IC junction temperature does not exceed the maximum value.
- Be sure to make the number of dot clocks input to the CXD3511Q in 1H an even number. Note that if there is an odd number of dot clocks, the internal phase compensation PLL will not operate properly.
- Be sure to make a thorough evaluation of any items not listed in this data sheet.

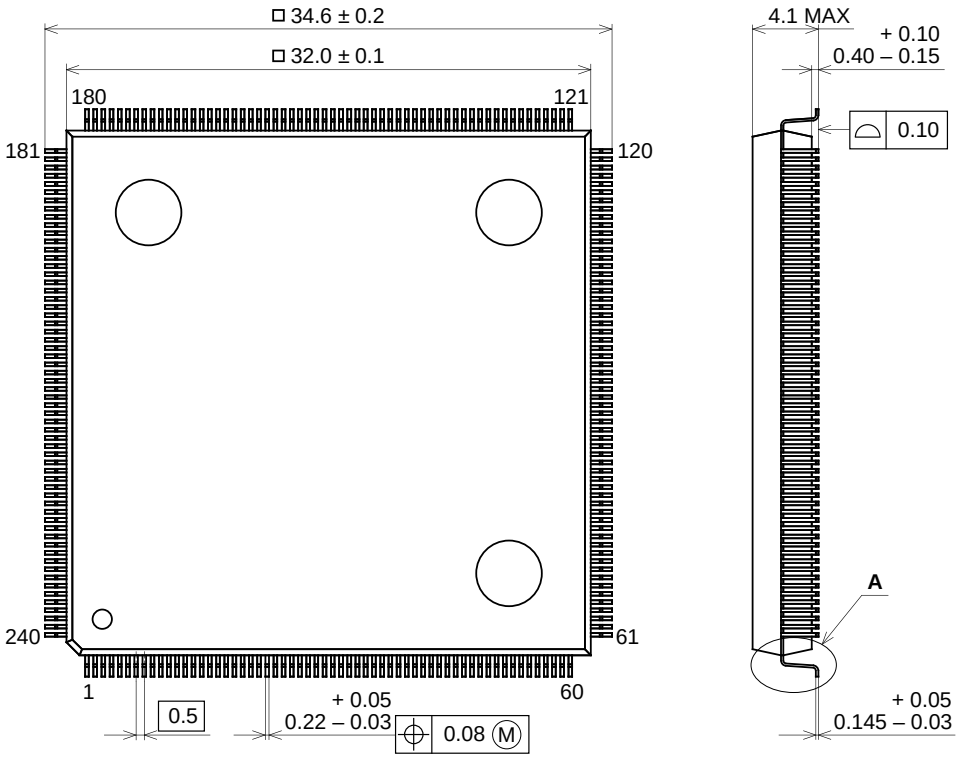
Application Circuit

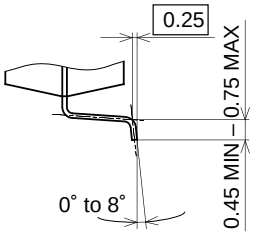


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

240PIN QFP (PLASTIC)





DETAIL **A**

SONY CODE	QFP-240P-L022
EIAJ CODE	QFP240-P-3232
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	7.6g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
LEAD TREATMENT	Sn-Bi