19-1524; Rev 2; 11/99

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

2.7V, Single-Supply, Cellular-Band Linear Power Amplifiers

MAX2264/MAX2265/MAX2266

General Description

The MAX2264/MAX2265/MAX2266 power amplifiers are designed for operation in IS-98-based CDMA, IS-136-based TDMA, and PDC cellular telephones operating in the 900MHz range. When matched for CDMA operation and biased with margin over the adjacent and alternate channel specification (-45dBc/-56dBc), the amplifiers achieve 28dBm output power with 37% efficiency (MAX2265). At +16dBm output—a very common power level for CDMA phones—the MAX2265 still has 7% efficiency, yielding excellent overall talk time. At the same power level, the MAX2264/MAX2266 have an unprecedented 12%/17% efficiency, while still obtaining 32%/32% efficiency at maximum output power.

The MAX2264/MAX2265/MAX2266 have internally referenced bias ports that are normally terminated with simple resistors. The bias ports allow customization of ACPR margin and gain. They can also be used to "throttle back" bias current when generating low power levels. The MAX2264/MAX2265/MAX2266 have excellent gain stability over temperature (±0.8dB), so overdesign of driver stages and excess driver current are dramatically reduced, further increasing the phone's talk time. The devices can be operated from +2.7V to +5V while meeting all ACPR specifications over the entire temperature range. Nonlinear efficiency is 48% when matched for linear operation, or 55% when matched for non-linear-only operation (MAX2265).

The devices are packaged in a 16-pin TSSOP with exposed pad (EP). For module or direct chip attach applications, the MAX2264 is also available in die form.

Applications

Cellular-Band CDMA Dual-Mode Phones
Cellular-Band PDC Phones
Cellular-Band TDMA Dual-Mode Phones
Dual-Mode Phones
2-Way Pagers
Power-Amplifier Modules

Selector Guide

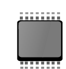
DEVICE	POWER-ADDED EFFICIENCY (%)		
	CDMA AT +28dBm	CDMA AT +16dBm	TDMA AT +30dBm
MAX2264	32	12	—
MAX2265	37	7	42
MAX2266	32	17	—

Features

- ♦ **Low Average CDMA Current Consumption in Typical Urban Scenario**
  55mA (MAX2264)
  90mA (MAX2265)
  40mA (MAX2266)
- ♦ **0.5µA Shutdown Mode Eliminates External Supply Switch**
- ♦ **±0.8dB Gain Variation Over Temperature**
- ♦ **No External Reference or Logic Interface Circuitry Needed**
- ♦ **Supply Current and ACPR Margin Dynamically Adjustable**
- ♦ **+2.7V to +5V Single-Supply Operation**
- ♦ **37% Efficiency at +2.7V Operation**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2264EUE	-40°C to +85°C	16 TSSOP-EP
MAX2264E/D	-40°C to +85°C	Dice*
MAX2265EUE	-40°C to +85°C	16 TSSOP-EP
MAX2266EUE	-40°C to +85°C	16 TSSOP-EP

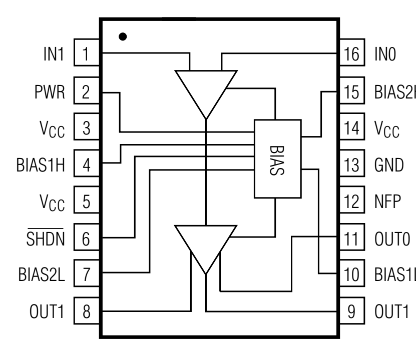

TSSOP-EP
5mm x 6.4mm

**Contact factory for dice specifications.*

Pin Configurations

TOP VIEW

MAX2264/MAX2266



TSSOP-EP

Pin Configurations continued at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND (no RF input) ....-0.3V to +6.5V
Logic Inputs to GND....................................-0.3V to (V_{CC} + 0.3V)
BIAS_ _ to GND..-0.3V to (V_{CC} + 0.3V)
RF Input Power ....+13dBm (20mW)
Logic Input Current..±10mA
Output VSWR with +13dBm Input.......................................2.5:1

Total DC Power Dissipation (T_{PADDLE} = +100°C)
16-Pin TSSOP-EP (derate 60mW/°C above T_{PADDLE} = +100°C) 4W
θ_{JA} ....8°C/W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5V, T_A = T_{MIN} to T_{MAX}, no input signal applied, $V_{\overline{SHDN}}$ = 2.0V. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}			2.7		5.0	V
Idle Current	I_{CC}	MAX2264/MAX2266	PWR = V_{CC}		95		mA
			PWR = GND		34		
		MAX2265			83		
Shutdown Supply Current	I_{CC}	$\overline{SHDN}$ = PWR = GND			0.5	10	µA
Logic Input Current High		Logic = V_{CC}		-1		5	µA
Logic Input Current Low		Logic = GND		-1		1	µA
Logic Threshold High				2.0			V
Logic Threshold Low						0.8	V

AC ELECTRICAL CHARACTERISTICS—MAX2264

(MAX2264 EV kit, V_{CC} = V_{PWR} = $V_{\overline{SHDN}}$ = +3.3V, T_A = +25°C, f_{IN} = 836MHz, CDMA modulation, $\overline{SHDN}$ = V_{CC}, matching networks tuned for 824MHz to 849MHz operation, 50Ω system, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency Range (Notes 1, 2)	f_{IN}	PWR = V_{CC} or GND		824		849	MHz
Power Gain (Note 1)	G_P	PWR = V_{CC}	T_A = +25°C	23	24.5		dB
			T_A = T_{MIN} to T_{MAX}	22			
		PWR = GND		18	21		
Gain Variation vs. Temperature (Note 1)		T_A = T_{MIN} to T_{MAX}, relative to T_A = +25°C			±0.8		dB
Output Power (High-Power Mode) (Note 1)	P_{OUT}	PWR = V_{CC}, P_{IN} adjusted to meet ACPR specification, f_{IN} = 824MHz to 849MHz		27	28		dBm
		PWR = V_{CC} = 2.8V, P_{IN} adjusted to meet ACPR specification, f_{IN} = 824MHz to 849MHz		26	27		
Output Power (Low-Power Mode) (Note 1)	P_{OUT}	PWR = GND, P_{IN} adjusted to meet ACPR specification, f_{IN} = 824MHz to 849MHz		15	16.5		dBm
		PWR = GND, V_{CC} = 2.8V, P_{IN} adjusted to meet ACPR specification, f_{IN} = 824MHz to 849MHz		14	15.5		

AC ELECTRICAL CHARACTERISTICS—MAX2264 (continued)

(MAX2264 EV kit, V_{CC} = V_{PWR} = $V_{\overline{SHDN}}$ = +3.3V, T_A = +25°C, f_{IN} = 836MHz, CDMA modulation, $\overline{SHDN}$ = V_{CC}, matching networks tuned for 824MHz to 849MHz operation, 50Ω system, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AMPS Output Power (Note 1)	P_{OUT}	P_{IN} = 8dBm	30.5	31		dBm
Adjacent-Channel Power Ratio Limit (Notes 1, 2)	ACPR	V_{CC} = 2.8V to 5.0V, offset = 885kHz, 30kHz BW, f_{IN} = 824MHz to 849MHz	-44			dBc
Alternate-Channel Power Ratio Limit (Notes 1, 2)	ACPR	V_{CC} = 2.8V to 5.0V, offset = 1980kHz, 30kHz BW, f_{IN} = 824MHz to 849MHz	-56			dBc
Power-Added Efficiency (Note 3)	PAE	PWR = V_{CC}, P_{IN} adjusted to meet ACPR specification		32		%
		PWR = GND, P_{IN} adjusted to meet ACPR specification		12		
AMPS Power-Added Efficiency	PAE	P_{IN} = 8dBm		44		%
Power-Mode Switching Time		(Note 4)		550		ns
Turn-On Time (Notes 1, 4)		PWR = V_{CC} or GND		1	5	µs
Maximum Input VSWR	VSWR	f_{IN} = 824MHz to 849MHz, PWR = GND or V_{CC}		2.4:1		
Nonharmonic Spurious due to Load Mismatch (Notes 1, 5)		P_{IN} = 10dBm			-60	dBc
Noise Power (Note 6)		Measured at 881MHz		-139		dBm/Hz
		PWR = GND, measured at 881MHz		-136		
AMPS Noise Power (Note 6)		Measured at 881MHz, P_{IN} = 8dBm		-138		dBm/Hz
Harmonic Suppression		(Note 7)		32		dBc

AC ELECTRICAL CHARACTERISTICS—MAX2265

(MAX2265 EV kit, V_{CC} = $V_{\overline{SHDN}}$ = +3.3V, T_A = +25°C, f_{IN} = 836MHz, CDMA modulation, matching networks tuned for 824MHz to 849MHz operation, 50Ω system, unless otherwise indicated.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range (Notes 1, 2)	f_{IN}		824		849	MHz
Power Gain (Note 1)	G_P	T_A = +25°C	24	25.5		dB
		T_A = T_{MIN} to T_{MAX}	23			
Gain Variation vs. Temperature (Note 1)		T_A = T_{MIN} to T_{MAX}, relative to T_A = +25°C		±0.7		dB
Output Power (Note 1)	P_{OUT}	P_{IN} adjusted to meet ACPR specification, f_{IN} = 824MHz to 849MHz	27	28		dBm
		V_{CC} = 2.8V, P_{IN} adjusted to meet ACPR specification, f_{IN} = 824MHz to 849MHz	26	26.5		
AMPS Output Power (Note 1)	P_{OUT}	P_{IN} = 8dBm	30	31		dBm
Adjacent-Channel Power Ratio (Notes 1, 2)	ACPR	V_{CC} = 2.8V to 5.0V, offset = 885kHz, 30kHz BW, f_{IN} = 824MHz to 849MHz	-44	-45		dBc
Alternate-Channel Power Ratio (Notes 1, 2)	ACPR	V_{CC} = 2.8V to 5.0V, offset = 1980kHz, 30kHz BW, f_{IN} = 824MHz to 849MHz	-56	-57		dBc

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AC ELECTRICAL CHARACTERISTICS—MAX2265 (continued)

(MAX2265 EV kit, V_{CC} = $V_{\overline{SHDN}}$ = +3.3V, T_A = +25°C, f_{IN} = 836MHz, CDMA modulation, matching networks tuned for 824MHz to 849MHz operation, 50Ω system, unless otherwise indicated.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Added Efficiency (Note 3)	PAE	P_{IN} adjusted to give P_{OUT} = 28dBm		37		%
		P_{IN} adjusted for P_{OUT} = 16dBm		7		
AMPS Power-Added Efficiency	PAE	P_{IN} = 8dBm		48		%
Turn-On Time (Notes 1, 4)				1	5	µs
Maximum Input VSWR	VSWR	f_{IN} = 824MHz to 849MHz		1.3:1		
Nonharmonic Spurious Due to Load Mismatch (Notes 1, 5)		P_{IN} = 10dBm			-60	dBc
Noise Power (Note 6)		Measured at 881MHz		-140		dBm/Hz
AMPS Noise Power (Note 6)		Measured at 881MHz, P_{IN} = 8dBm		-139		dBm/Hz
Harmonic Suppression		(Note 7)		47		dBc

AC ELECTRICAL CHARACTERISTICS—MAX2266

(MAX2266 EV kit, V_{CC} = $V_{\overline{SHDN}}$ = +3.3V, T_A = +25°C, f_{IN} = 836MHz, CDMA modulation, matching networks tuned for 824MHz to 849MHz operation, 50Ω system, unless otherwise indicated.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency Range (Notes 1, 2)	f_{IN}	PWR = V_{CC} or GND		824		849	MHz
Power Gain (Note 1)	G_P	PWR = V_{CC}	T_A = +25°C	24.5	26		dB
			T_A = T_{MIN} to T_{MAX}	23			
		PWR = GND		25	27.5		
Gain Variation vs. Temperature (Note 1)		T_A = T_{MIN} to T_{MAX}, relative to T_A = +25°C			±0.8		dB
Output Power (High-Power Mode) (Note 1)	P_{OUT}	PWR = V_{CC}, P_{IN} adjusted to meet ACPR specification, f_{IN} = 824MHz to 849MHz		27	28		dBm
		PWR = V_{CC} = 2.8V, P_{IN} adjusted to meet ACPR specification, f_{IN} = 824MHz to 849MHz		26	27		
Output Power (Low-Power Mode) (Note 1)	P_{OUT}	PWR = GND, P_{IN} adjusted to meet ACPR specification, f_{IN} = 824MHz to 849MHz		14	15.5		dBm
		PWR = GND, V_{CC} = 2.8V, P_{IN} adjusted to meet ACPR specification, f_{IN} = 824MHz to 849MHz		13	14		
AMPS Output Power (Note 1)	P_{OUT}	P_{IN} = 8dBm		31	32		dBm
Adjacent-Channel Power Ratio Limit (Notes 1, 2)	ACPR	V_{CC} = 2.8V to 5.0V, offset = 885kHz, 30kHz BW, f_{IN} = 824MHz to 849MHz		-44			dBc
Alternate-Channel Power Ratio Limit (Notes 1, 2)	ACPR	V_{CC} = 2.8V to 5.0V, offset = 1980kHz, 30kHz BW, f_{IN} = 824MHz to 849MHz		-56			dBc
Power-Added Efficiency (Note 3)	PAE	PWR = V_{CC}, P_{IN} adjusted to meet ACPR specification			32		%
		PWR = GND, P_{IN} adjusted to meet ACPR specification			17		

AC ELECTRICAL CHARACTERISTICS—MAX2266 (continued)

(MAX2266 EV kit, $V_{CC} = V_{PWR} = V_{\overline{SHDN}} = +3.3V$, $T_A = +25°C$, $f_{IN} = 836MHz$, CDMA modulation, $\overline{SHDN} = V_{CC}$, matching networks tuned for 824MHz to 849MHz operation, 50Ω system, unless otherwise noted.)

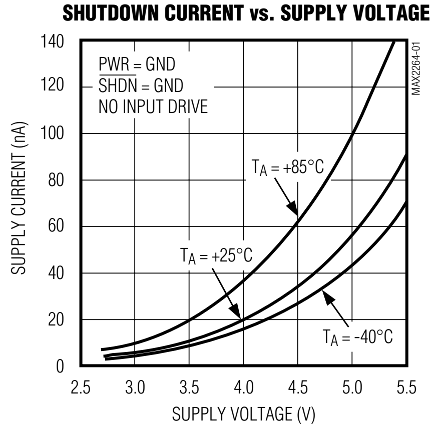
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AMPS Power-Added Efficiency	PAE	P_{IN} = 8dBm		48		%
Power-Mode Switching Time		(Note 4)		550		ns
Turn-On Time (Notes 1, 4)		PWR = V_{CC} or GND		1	5	µs
Maximum Input VSWR	VSWR	f_{IN} = 824MHz to 849MHz, PWR = GND or V_{CC}		2.4:1		
Nonharmonic Spurious due to Load Mismatch (Notes 1, 5)		P_{IN} = 10dBm			-60	dBc
Noise Power (Note 6)		Measured at 881MHz		-137		dBm/Hz
		PWR = GND, measured at 881MHz		-130		
AMPS Noise Power (Note 6)		Measured at 881MHz, P_{IN} = 8dBm		-136		dBm/Hz
Harmonic Suppression		(Note 7)		32		dBc

Note 1: Minimum and maximum values are guaranteed by design and characterization, not production tested.
Note 2: P_{MAX} is met over this frequency range at the ACPR limit with a single matching network. For optimum performance at other frequencies, the output matching network must be properly designed. See the *Applications Information* section. Operation between 750MHz and 1000MHz is possible but has not been characterized.
Note 3: PAE is specified into a 50Ω load, while meeting ACPR requirements.
Note 4: Time from logic transition until P_{OUT} is within 1dB of its final mean power.
Note 5: Murata isolator as load with 20:1 VSWR any phase angle after isolator.
Note 6: Noise power can be improved by using the circuit in Figures 1, 2, and 3.
Note 7: Harmonics measured on evaluation kit, which provides some harmonic attenuation in addition to the rejection provided by the IC. The combined suppression is specified.

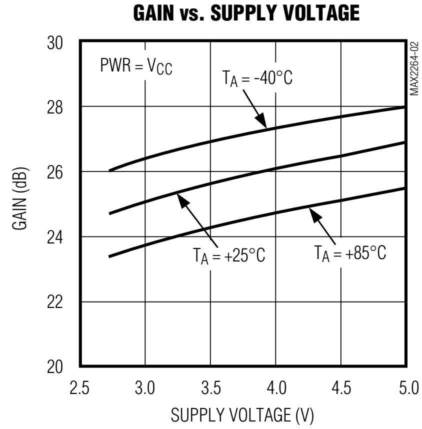
Typical Operating Characteristics

(MAX2264/MAX2265/MAX2266 EV kits, V_{CC} = +3.3V, $\overline{SHDN} = V_{CC}$, CDMA modulation, T_A = +25°C, unless otherwise noted.)

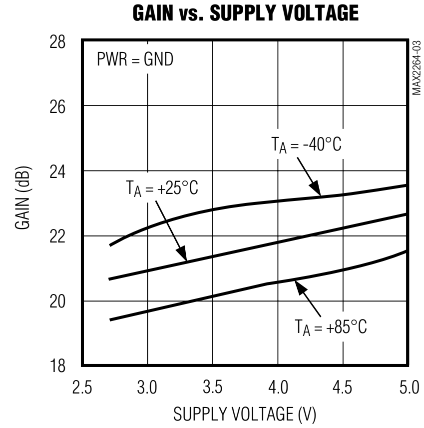
MAX2264
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



MAX2264
GAIN vs. SUPPLY VOLTAGE



MAX2264
GAIN vs. SUPPLY VOLTAGE



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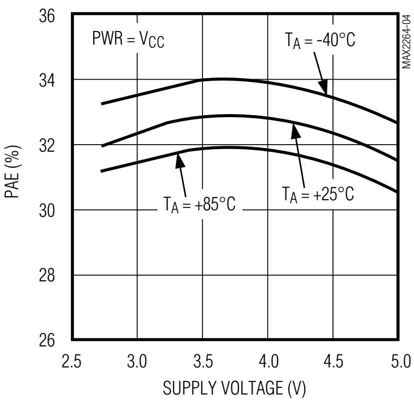
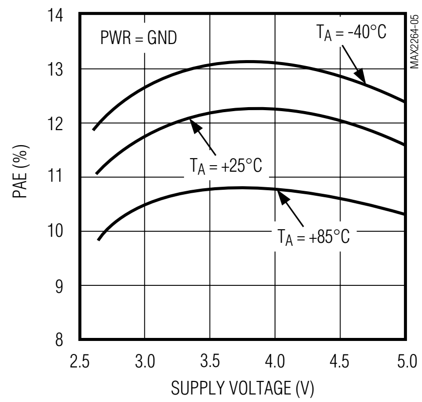
Typical Operating Characteristics (continued)

(MAX2264/MAX2265/MAX2266 EV kits, V_{CC} = +3.3V, $\overline{SHDN}$ = V_{CC}, CDMA modulation, T_A = +25°C, unless otherwise noted.)

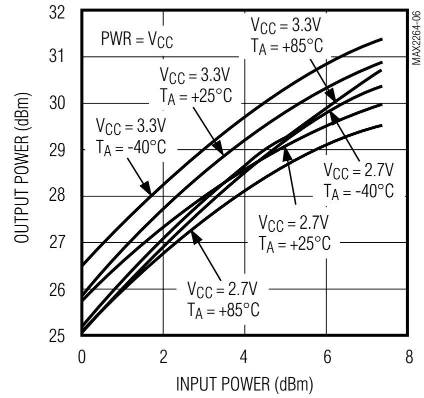
MAX2264
POWER-ADDED EFFICIENCY vs. SUPPLY VOLTAGE



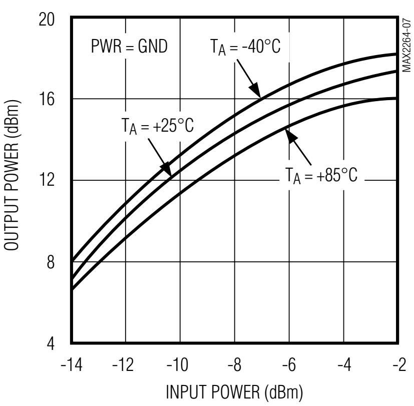
MAX2264
POWER-ADDED EFFICIENCY vs. SUPPLY VOLTAGE



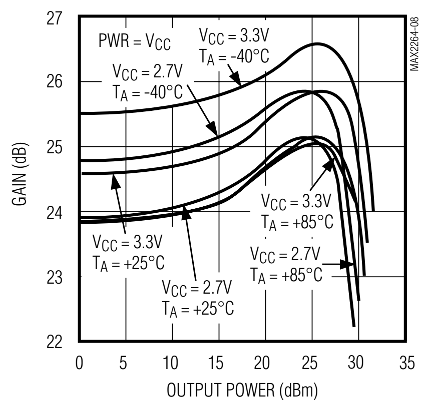
MAX2264
OUTPUT POWER vs. INPUT POWER



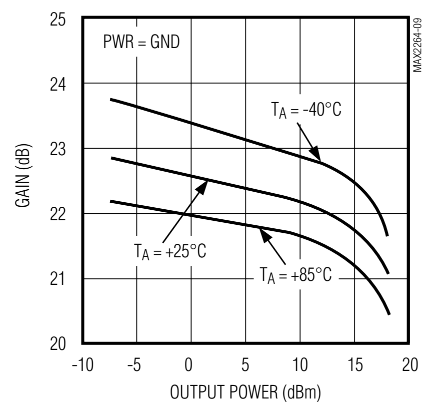
MAX2264
OUTPUT POWER vs. INPUT POWER



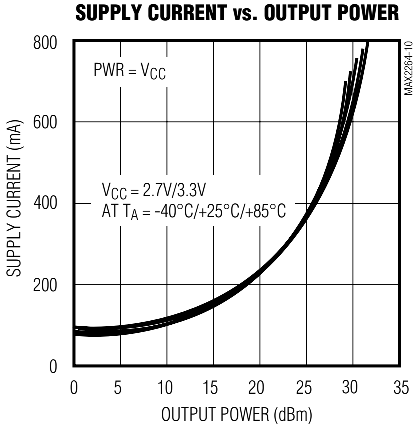
MAX2264
GAIN vs. OUTPUT POWER



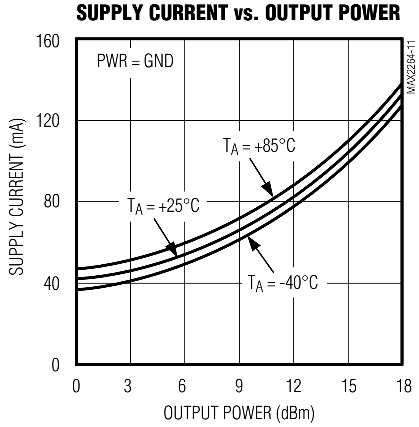
MAX2264
GAIN vs. OUTPUT POWER



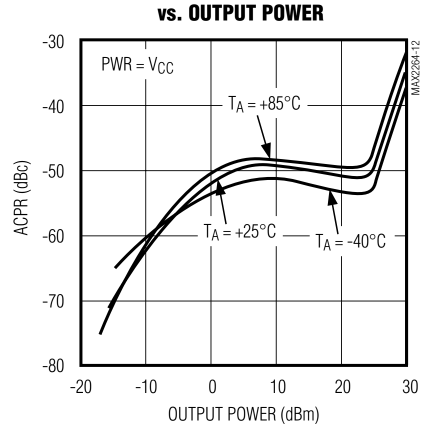
MAX2264
SUPPLY CURRENT vs. OUTPUT POWER



MAX2264
SUPPLY CURRENT vs. OUTPUT POWER



MAX2264
ADJACENT-CHANNEL POWER RATIO vs. OUTPUT POWER

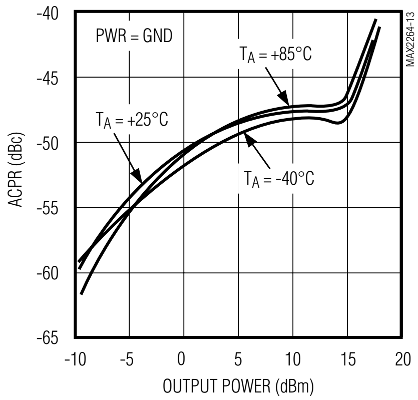


2.7V, Single-Supply, Cellular-Band Linear Power Amplifiers

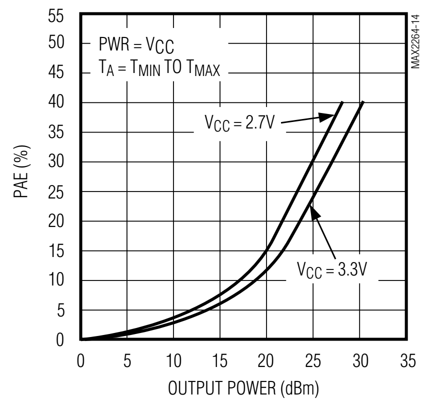
Typical Operating Characteristics (continued)

(MAX2264/MAX2265/MAX2266 EV kits, V_{CC} = +3.3V, $\overline{SHDN}$ = V_{CC}, CDMA modulation, T_A = +25°C, unless otherwise noted.)

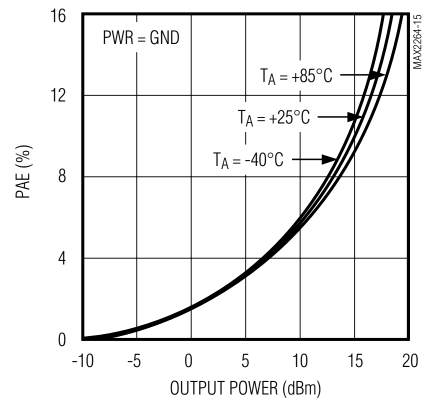
MAX2264 ADJACENT-CHANNEL POWER RATIO vs. OUTPUT POWER



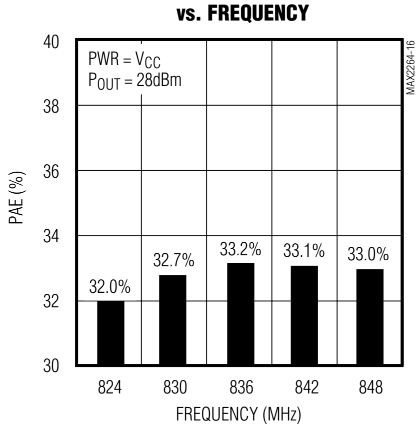
MAX2264 POWER-ADDED EFFICIENCY vs. OUTPUT POWER



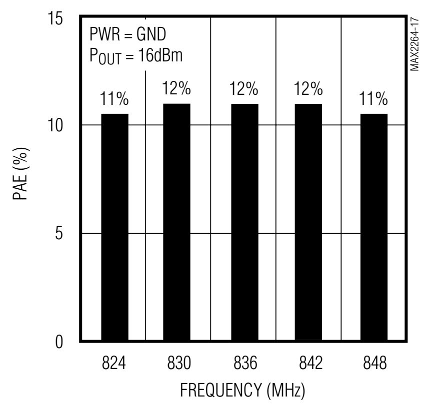
MAX2264 POWER-ADDED EFFICIENCY vs. OUTPUT POWER



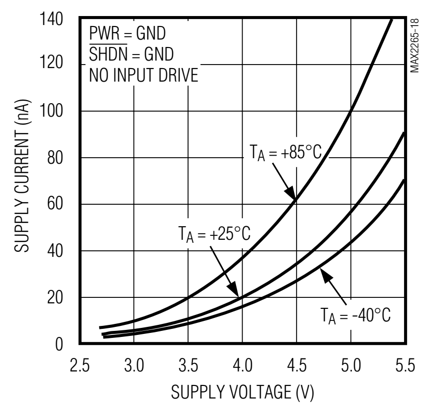
MAX2264 POWER-ADDED EFFICIENCY vs. FREQUENCY



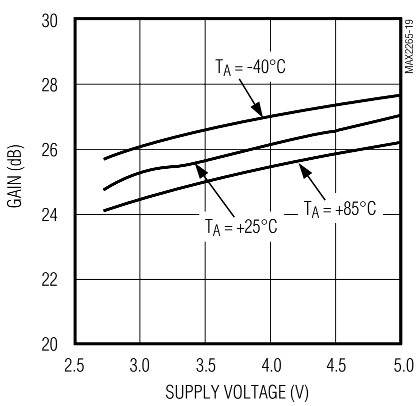
MAX2264 POWER-ADDED EFFICIENCY vs. FREQUENCY



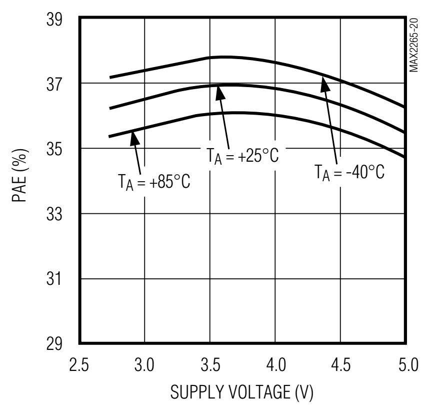
MAX2265 SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



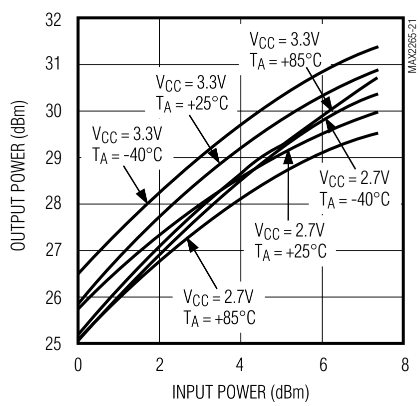
MAX2265 GAIN vs. SUPPLY VOLTAGE



MAX2265 POWER-ADDED EFFICIENCY vs. SUPPLY VOLTAGE



MAX2265 OUTPUT POWER vs. INPUT POWER

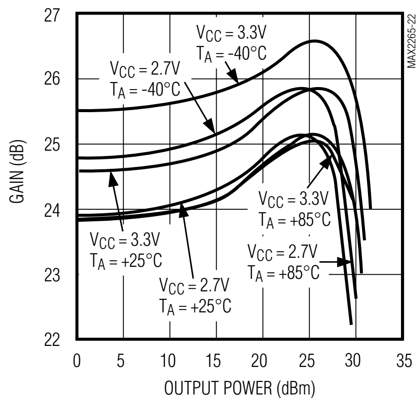


2.7V, Single-Supply, Cellular-Band Linear Power Amplifiers

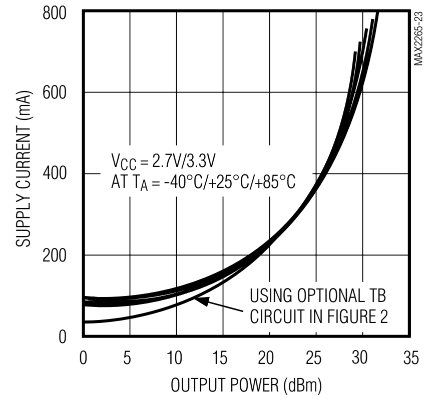
Typical Operating Characteristics (continued)

(MAX2264/MAX2265/MAX2266 EV kits, V_{CC} = +3.3V, $\overline{SHDN}$ = V_{CC}, CDMA modulation, T_A = +25°C, unless otherwise noted.)

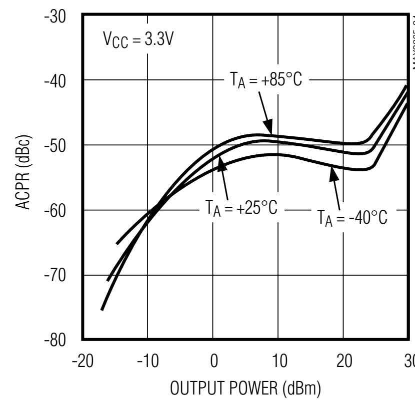
MAX2265
GAIN vs. OUTPUT POWER



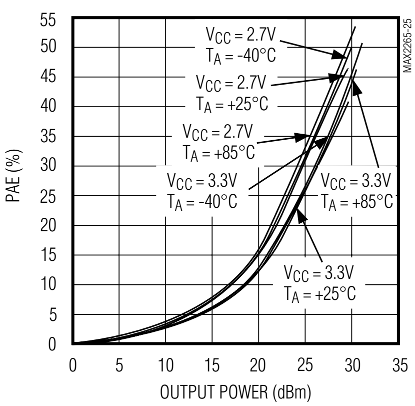
MAX2265
SUPPLY CURRENT vs. OUTPUT POWER



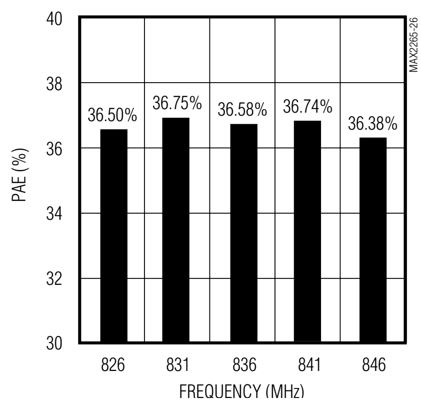
MAX2265
ADJACENT-CHANNEL POWER RATIO vs. OUTPUT POWER



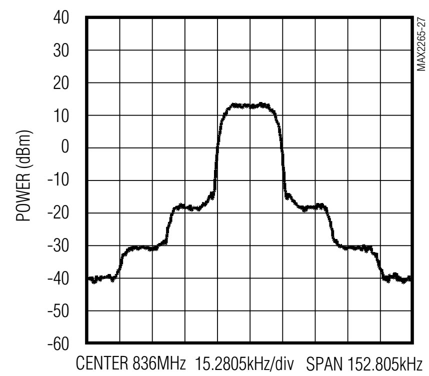
MAX2265
POWER-ADDED EFFICIENCY vs. OUTPUT POWER



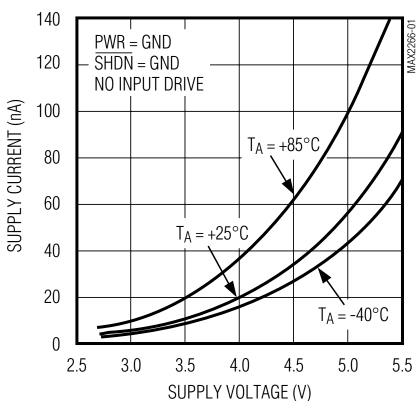
MAX2265
POWER-ADDED EFFICIENCY vs. FREQUENCY



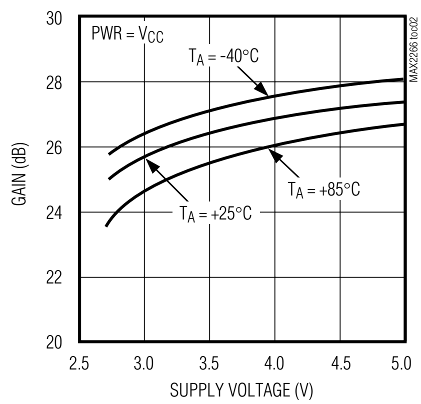
MAX2265
TDMA POWER SPECTRUM



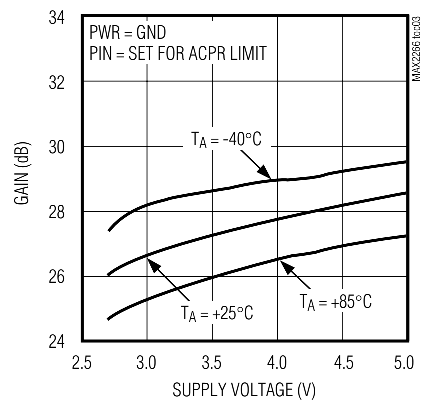
MAX2266
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



MAX2266
GAIN vs. SUPPLY VOLTAGE



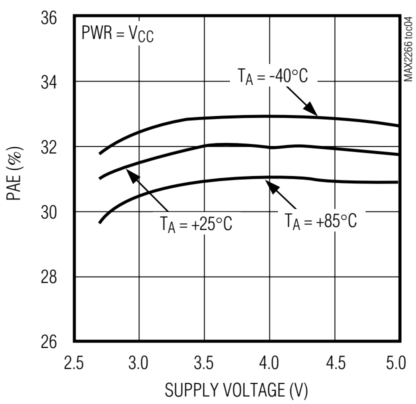
MAX2266
GAIN vs. SUPPLY VOLTAGE



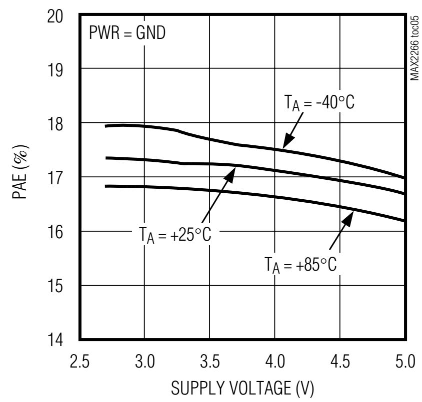
Typical Operating Characteristics (continued)

(MAX2264/MAX2265/MAX2266 EV kits, V_{CC} = +3.3V, $\overline{SHDN}$ = V_{CC}, CDMA modulation, T_A = +25°C, unless otherwise noted.)

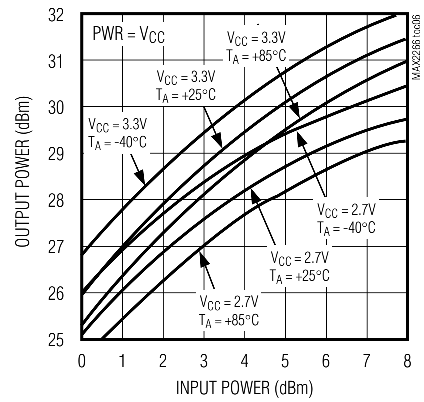
**MAX2266
POWER-ADDED EFFICIENCY
vs. SUPPLY VOLTAGE**



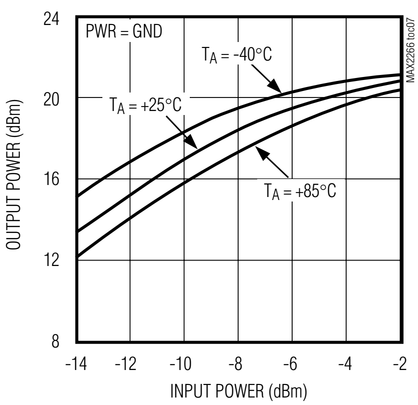
**MAX2266
POWER-ADDED EFFICIENCY
vs. SUPPLY VOLTAGE**



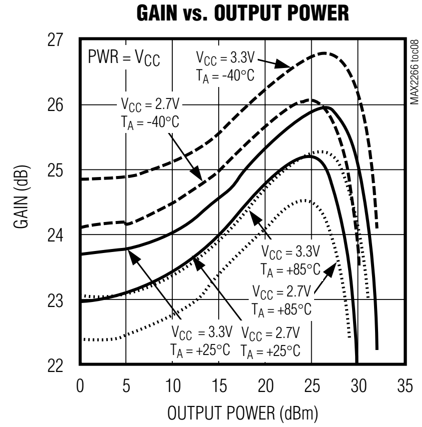
**MAX2266
OUTPUT POWER vs. INPUT POWER**



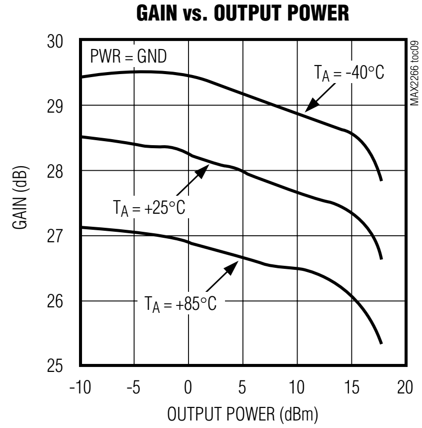
**MAX2266
OUTPUT POWER vs. INPUT POWER**



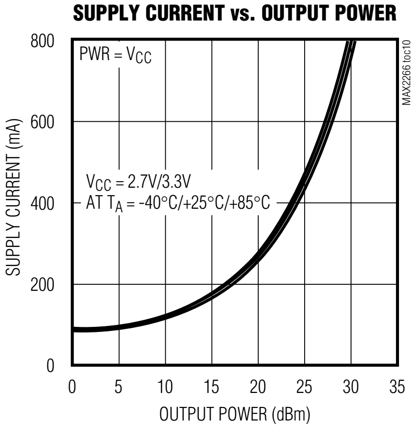
**MAX2266
GAIN vs. OUTPUT POWER**



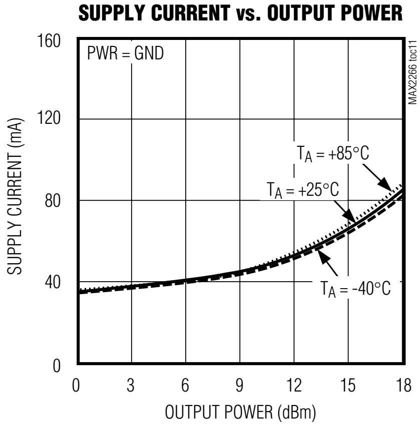
**MAX2266
GAIN vs. OUTPUT POWER**



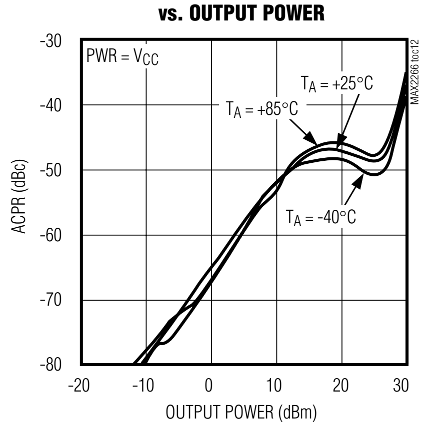
**MAX2266
SUPPLY CURRENT vs. OUTPUT POWER**



**MAX2266
SUPPLY CURRENT vs. OUTPUT POWER**



**MAX2266
ADJACENT-CHANNEL POWER RATIO
vs. OUTPUT POWER**

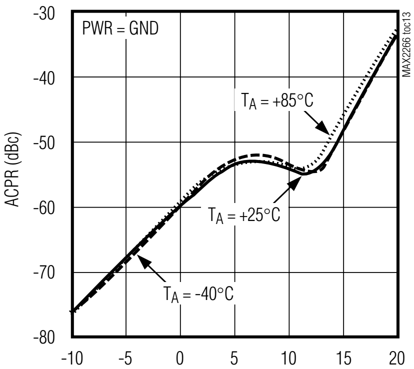


2.7V, Single-Supply, Cellular-Band Linear Power Amplifiers

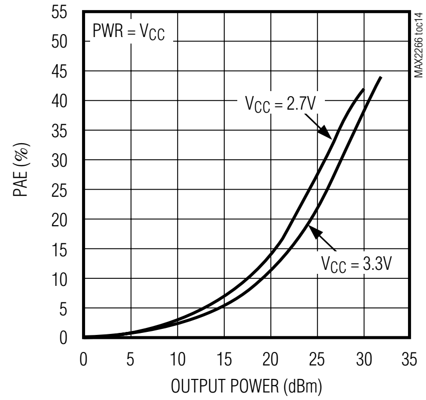
Typical Operating Characteristics (continued)

(MAX2264/MAX2265/MAX2266 EV kits, V_{CC} = +3.3V, $\overline{SHDN}$ = V_{CC}, CDMA modulation, T_A = +25°C, unless otherwise noted.)

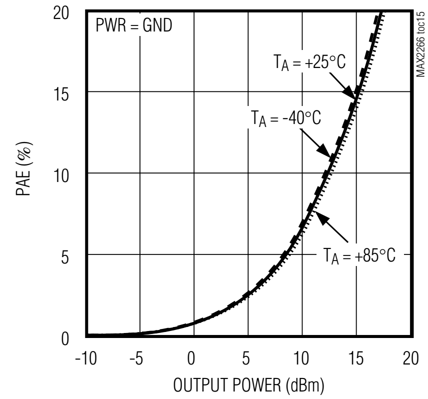
MAX2266 ADJACENT-CHANNEL POWER RATIO vs. OUTPUT POWER



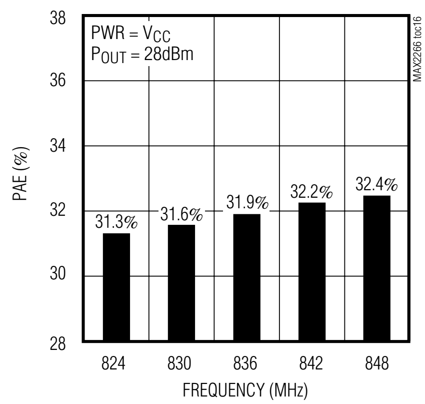
MAX2266 POWER-ADDED EFFICIENCY vs. OUTPUT POWER



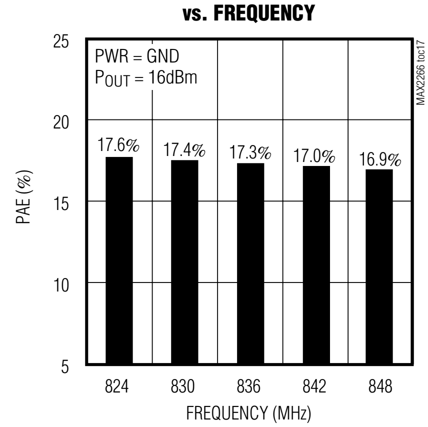
MAX2266 POWER-ADDED EFFICIENCY vs. OUTPUT POWER



MAX2266 POWER-ADDED EFFICIENCY vs. FREQUENCY



MAX2266 POWER-ADDED EFFICIENCY vs. FREQUENCY



Pin Description

PIN		NAME	FUNCTION
MAX2264 MAX2266	MAX2265		
1	1	IN1	RF Input Port. Requires external matching network.
2	—	PWR	Mode-Select Input. Drive low to select the low-power mode (BIAS1L and BIAS2L). Drive high to select high-power mode (BIAS1H and BIAS2H).
3, 5, 14	3, 5	V_{CC}	Voltage Supply. Bypass with capacitors connected between this pin and GND.
4	4	BIAS1H	High-Power Mode First Stage Bias Control. See *General Description*.
6	2, 6	$\overline{SHDN}$	Shutdown Control Input. Drive $\overline{SHDN}$ low to enable shutdown. Drive high for normal operation. On the MAX2265, make sure that both pins get driven simultaneously. To place the MAX2264/MAX2266 into shutdown mode, also pull the PWR pin low.
7	—	BIAS2L	Low-Power Mode Second Stage Bias Control. See *General Description*.
8, 9	8, 9	OUT1	RF Output Ports. Require an appropriate output matching network and collector bias.
10	—	BIAS1L	Low-Power Mode First Stage Bias Control. See *General Description*.
11	—	OUT0	RF Output Port. Requires an appropriate output matching network and collector bias.
12	12	NFP	Noise Filtering Pin. Connect noise filtering network as described in *Noise Filtering* section. If unused, leave open.
—	7, 10, 11, 14, 16	N.C.	Not Internally Connected. Do not make any connections to these pins.
13, Slug	13, Slug	GND	Ground. Solder the package slug to high-thermal-conductivity circuit board ground plane.
15	15	BIAS2H	High-Power Mode Second Stage Bias Control. See *General Description*.
16	—	IN0	RF Input Port. Requires external matching network.

Detailed Description

The MAX2264/MAX2265/MAX2266 are linear power amplifiers (PAs) intended for CDMA and TDMA applications. The devices have been fully characterized in the 824MHz to 849MHz U.S. cellular band and can be used from 750MHz to 1000MHz by adjusting the input and output match. In CDMA applications, they provide typically 28dBm of output power and up to 37% power-added efficiency (PAE) from a single +2.7V to +5V supply. In TDMA applications, efficiency is 42% at 30dBm of output power.

An inherent drawback of traditional PAs is that their efficiency drops rapidly with reduced output power. For example, in a PA designed for maximum efficiency at +28dBm, the efficiency at +15dBm falls well below 4.5% (over 210mA from a +3.3V supply). This behavior significantly reduces talk time in CDMA phones because over 90% of the time they are at output powers below +16dBm. The MAX2264/MAX2265/MAX2266 are optimized for lowest current draw at output powers that are most likely to occur in real-life situations. This provides up to 50% reduced average PA current.

High-Power and Low-Power Modes

The MAX2264/MAX2266 are designed to provide optimum PAE in both high- and low-power modes. For a +3.3V supply, maximum output power is +28dBm in high-power mode and +16dBm in low-power mode. Use the system's microcontroller to determine required output power, and switch between the two modes as appropriate with the PWR logic pin.

Bias Control

The bias current of the first stage in low-power mode is proportional to the current flowing out of BIAS1L. The voltage at BIAS1L is fixed by an internal bandgap reference, so the current out of this pin is inversely proportional to the value of the resistor between this pin and ground. Similarly, the bias current of the first stage in high-power mode is proportional to the current flowing out of BIAS1H. The current in the second stage is proportional to the currents out of BIAS2L and BIAS2H for low- and high-power modes, respectively.

Additionally, these resistors allow for customization of gain and alternate- and adjacent-channel power ratios. Increasing the bias current in the first stage increases the gain and improves alternate-channel power ratio at the expense of efficiency. Increasing the bias current in the second stage increases gain at the expense of efficiency as well as adjacent- and alternate-channel power ratios.

The PA bias current can be dynamically adjusted by summing a current into the bias pin of interest with an external source such as a DAC. See the MAX2265 *Typical Application Circuit* for using a voltage DAC and current setting resistors RTB1 and RTB2. Choosing RTB1 = R1 and RTB2 = R2 allows current adjustment between 0mA to double the nominal idle current with DAC voltages between 0V and 2.4V. The DAC must be able to source approximately 100µA.

Shutdown Mode

Pull pins 2 and 6 low to place the MAX2264/MAX2265/MAX2266 into shutdown mode. In this mode, all gain stages are disabled and supply current drops to 0.5µA.

Increasing Efficiency Further

The MAX2266 incorporates an additional external switch to increase efficiency to 17% at +16dBm and to 32% at +28dBm. This efficiency increase is mainly due to the additional isolation between the high- and low-power outputs provided by the external switch.

Applications Information

External Components

The MAX2264/MAX2265/MAX2266 require matching circuits at their inputs and outputs for operation in a 50Ω system. The application circuits in Figures 1, 2, and 3 describe the topology of the matching circuits for

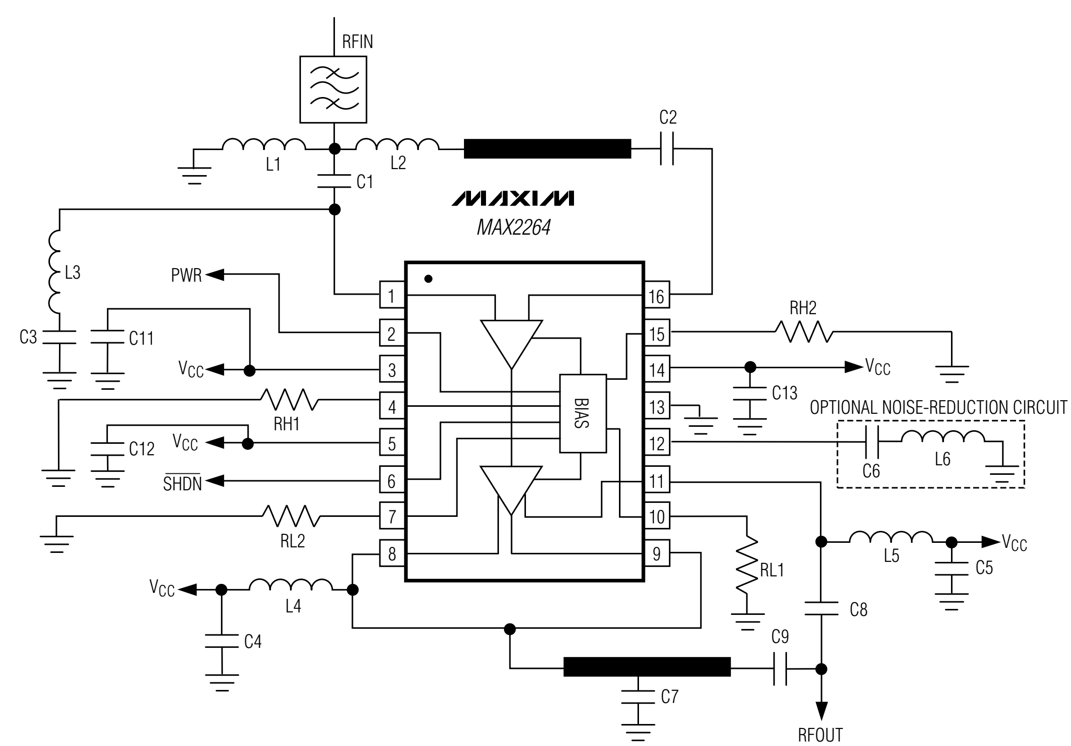


Figure 1. MAX2264 Typical Application Circuit

each device; suggested component values, suppliers, and part numbers are listed in Table 1. These values are optimized for best simultaneous efficiency and return loss performance. Use high-quality components in these matching circuits for greatest efficiency.

Layout and Power-Supply Bypassing

A properly designed PC board is essential to any RF/microwave circuit. Be sure to use controlled impedance lines on all high-frequency inputs and outputs. Proper grounding of the GND pins is fundamental; if the PC board uses a topside RF ground, connect all GND pins (especially the TSSOP package exposed GND pad) directly to it. On boards where the ground plane is not on the component side, it's best to connect all GND pins to the ground plane with plated through-holes close to the package.

To minimize coupling between different sections of the system, the ideal power-supply layout is a star configuration with a large decoupling capacitor at a central V_{CC} node. The V_{CC} traces branch out from this central node, each leading to a separate V_{CC} node on the PC board. A second bypass capacitor with low ESR at the RF frequency of operation is located at the end of each trace. This arrangement provides local decoupling at the V_{CC} pin.

Input and output impedance-matching networks are very sensitive to layout-related parasitics. It is important to keep all matching components as close to the IC as possible to minimize the effects of stray inductance and stray capacitance of PC board traces.

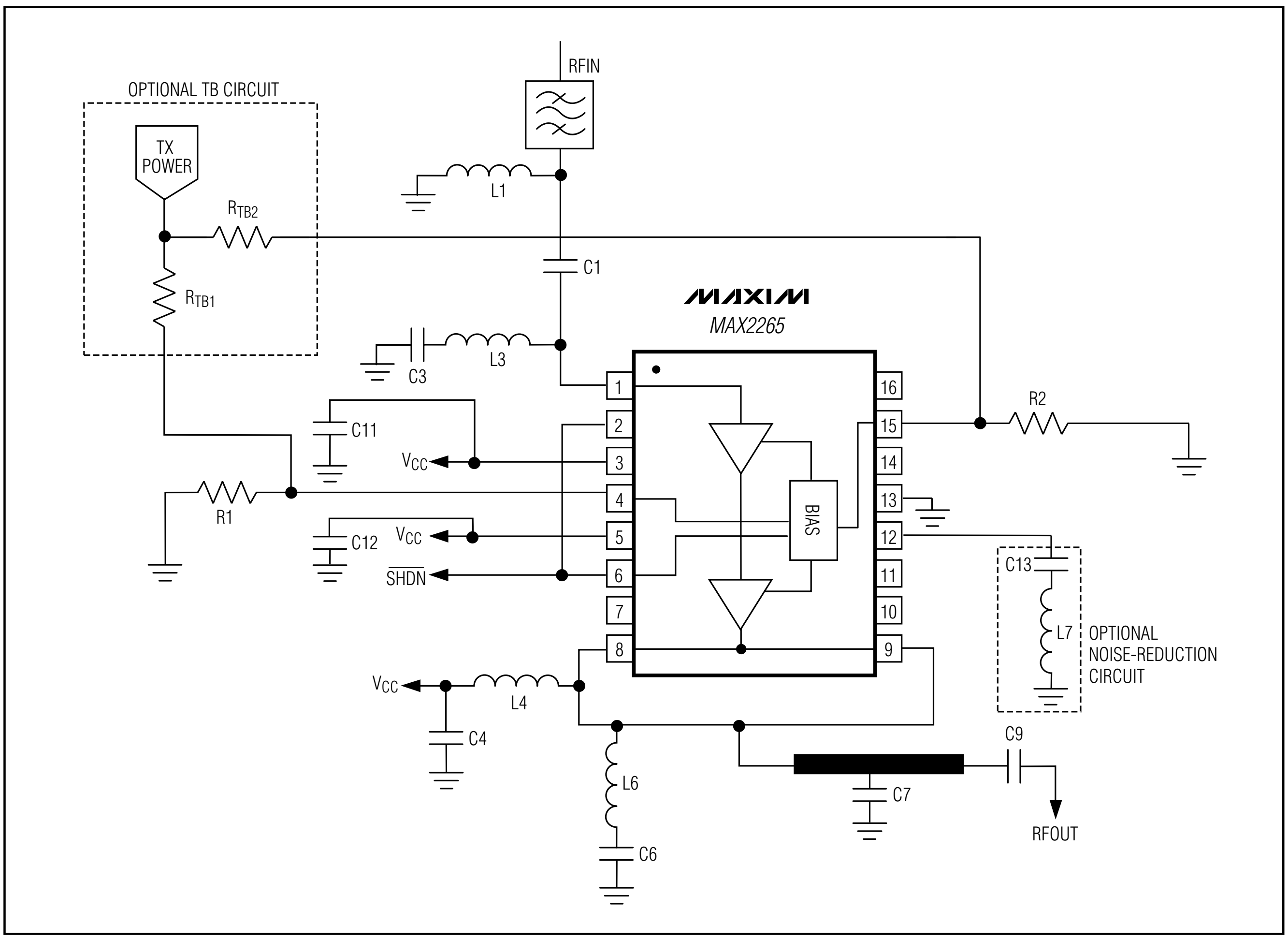


Figure 2. MAX2265 Typical Application Circuit

2.7V, Single-Supply, Cellular-Band Linear Power Amplifiers

Noise Filtering

For improved noise performance, the MAX2264/MAX2265/MAX2266 allow for additional noise filtering for further suppression of transmit noise. This is achieved by using C6 and L6 on the MAX2264, C13 and L7 on the MAX2265, and C6 and L6 on the MAX2266. Use the recommended component values for optimal noise power (Table 1).

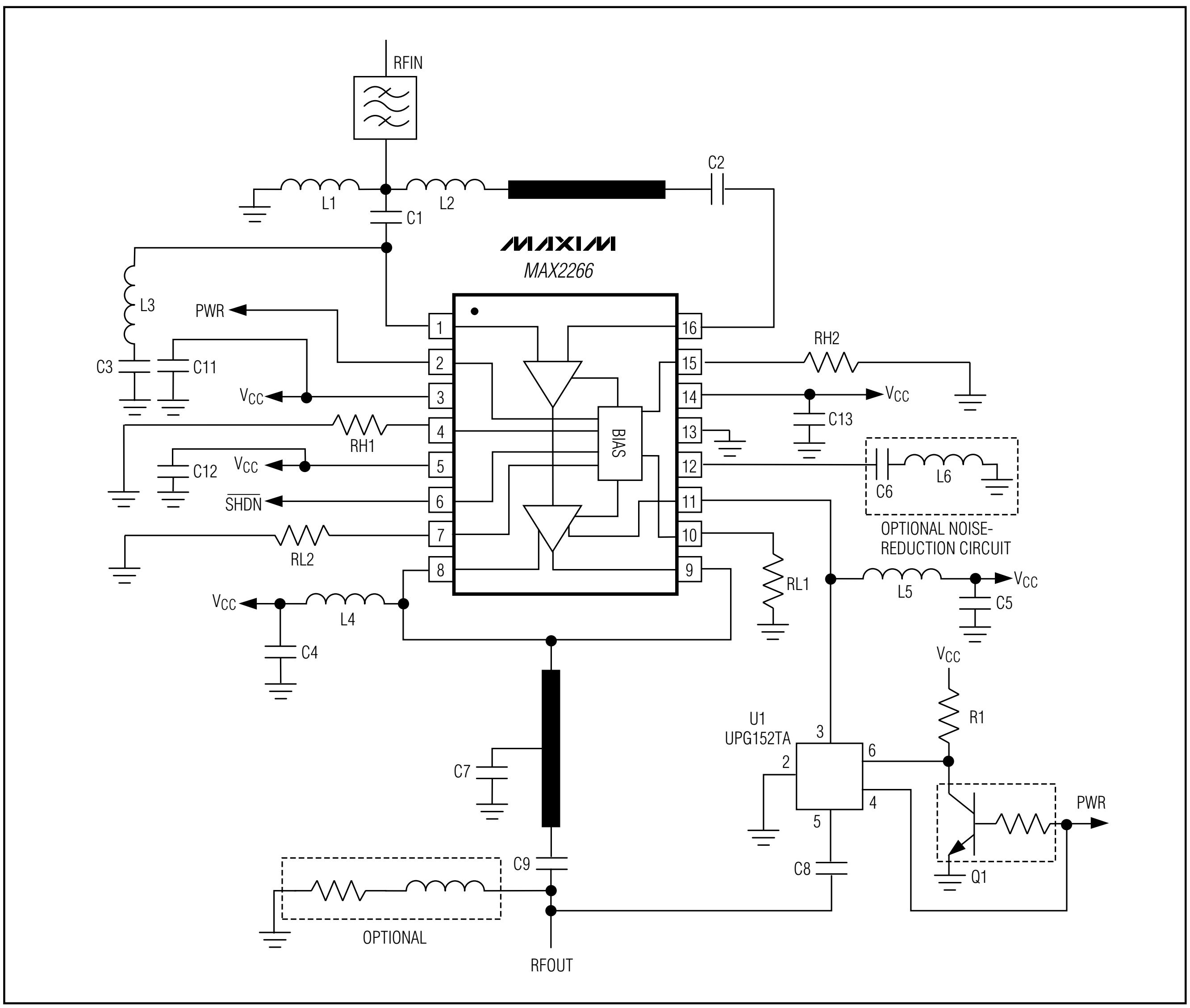
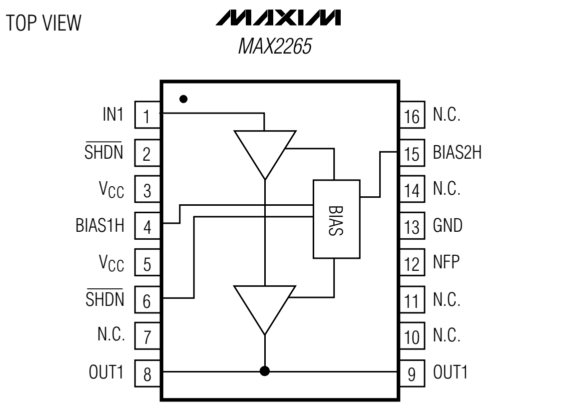


Figure 3. MAX2266 Typical Application Circuit

Pin Configurations (continued)



TSSOP-EP

Chip Information

TRANSISTOR COUNT: 1256

NOTES