



# 1:5 Differential (LV)PECL/(LV)ECL/HSTL Clock and Data Driver

MAX9316A

## General Description

The MAX9316A is a low-skew, 1-to-5 differential driver designed for clock and data distribution. This device allows selection between two inputs: one differential and one single ended. The selected input is reproduced at five differential outputs. The differential input can be adapted to accept a single-ended input by connecting the on-chip V<sub>BB</sub> supply to one input as a reference voltage.

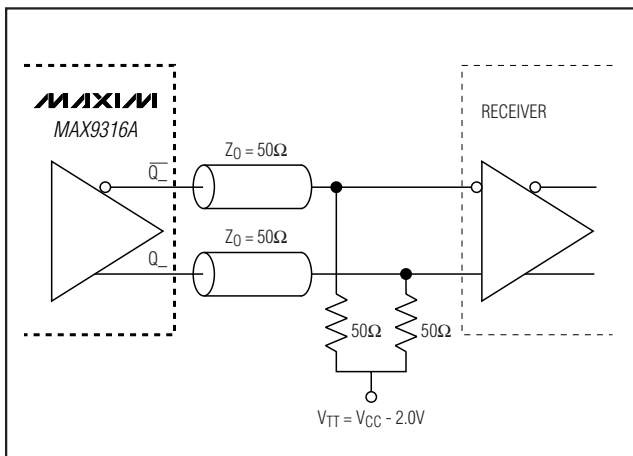
The MAX9316A features low output-to-output skew (20ps), making it ideal for clock and data distribution across a backplane or board. For interfacing to differential HSTL and (LV)PECL signals, this device operates over a 3.0V to 5.5V supply range, allowing high-performance clock or data distribution in systems with a nominal 3.3V or 5.0V supply. For differential (LV)ECL operation, this device operates with a -3.0V to -5.5V supply.

The MAX9316A is offered in a 20-pin wide SO package.

## Applications

- Precision Clock Distribution
- Low-Jitter Data Repeaters
- Data and Clock Drivers and Buffers
- Central-Office Backplane Clock Distribution
- DSLAM Backplane
- Base Stations
- ATE

## Typical Application Circuit



Functional Diagram appears at end of data sheet.

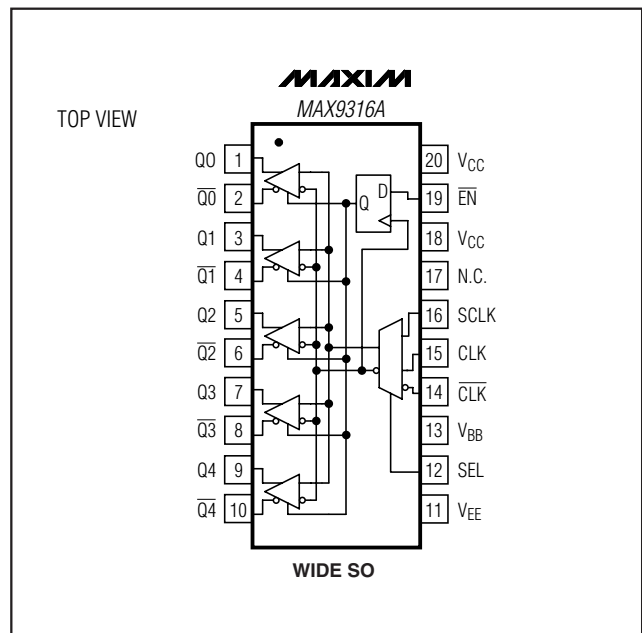
## Features

- ◆ Guaranteed 400mV Differential Output at 1.5GHz
- ◆ Selectable Single-Ended or Differential Input
- ◆ 130ps (max) Part-to-Part Skew at +25°C
- ◆ 20ps Output-to-Output Skew
- ◆ 365ps Propagation Delay
- ◆ Synchronous Output Enable/Disable
- ◆ On-Chip Reference for Single-Ended Inputs
- ◆ Input Biased to Low when Open
- ◆ Pin Compatible with MC100EL14

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9316AEWP	-40°C to +85°C	20 Wide SO

## Pin Configuration



# 1:5 Differential (LV)PECL/(LV)ECL/ HSTL Clock and Data Driver

## ABSOLUTE MAXIMUM RATINGS

V <sub>CC</sub> - V <sub>EE</sub> .....	6.0V	Junction-to-Ambient Thermal Resistance with 500LFPM Airflow Single-Layer PC Board 20-Pin Wide SO.....	+58°C/W
Single-Ended Inputs (SCLK, SEL, $\overline{\text{EN}}$ , CLK, $\overline{\text{CLK}}$ ) For V <sub>CC</sub> - V <sub>EE</sub> ≤ 4.2V.....	V <sub>EE</sub> - 0.3V to V <sub>CC</sub> + 0.3V	Junction-to-Case Thermal Resistance 20-Pin Wide SO.....	+20°C/W
For V <sub>CC</sub> - V <sub>EE</sub> > 4.2V.....	V <sub>EE</sub> - 4.2V to V <sub>CC</sub> + 0.3V	Operating Temperature Range.....	-40°C to +85°C
CLK to $\overline{\text{CLK}}$ .....	±3.0V	Junction Temperature.....	+150°C
Continuous Output Current.....	50mA	Storage Temperature Range.....	-65°C to +150°C
Surge Output Current.....	100mA	ESD Protection Human Body Model (Inputs and Outputs).....	2kV
V <sub>BB</sub> Sink/Source Current.....	±0.65mA	Lead Temperature (soldering, 10s).....	+300°C
Continuous Power Dissipation (T <sub>A</sub> = +70°C) Single-Layer PC Board 20-Pin Wide SO (derate 10mW/°C above +70°C).....	800mW		
Junction-to-Ambient Thermal Resistance in Still Air Single-Layer PC Board 20-Pin Wide SO.....	+100°C/W		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> - V<sub>EE</sub> = 3.0V to 5.5V, outputs loaded with 50Ω ±1% to V<sub>CC</sub> - 2V, SEL = high or low,  $\overline{\text{EN}}$  = low, unless otherwise noted. Typical values are at V<sub>CC</sub> - V<sub>EE</sub> = 5.0V, V<sub>IHD</sub> = V<sub>CC</sub> - 1V, V<sub>I LD</sub> = V<sub>CC</sub> - 1.5V.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>SINGLE-ENDED INPUTS (SCLK, SEL, <math>\overline{\text{EN}}</math>)</b>												
Input High Voltage	V <sub>IH</sub>		V <sub>CC</sub> - 1.095		V <sub>CC</sub>	V <sub>CC</sub> - 1.125		V <sub>CC</sub>	V <sub>CC</sub> - 1.125		V <sub>CC</sub>	V
Input Low Voltage	V <sub>IL</sub>	(V <sub>CC</sub> - V <sub>EE</sub> ) ≤ 4.2	V <sub>EE</sub>		V <sub>CC</sub> - 1.495	V <sub>EE</sub>		V <sub>CC</sub> - 1.495	V <sub>EE</sub>		V <sub>CC</sub> - 1.575	V
		(V <sub>CC</sub> - V <sub>EE</sub> ) > 4.2V	V <sub>CC</sub> - 4.2		V <sub>CC</sub> - 1.495	V <sub>CC</sub> - 4.2		V <sub>CC</sub> - 1.495	V <sub>CC</sub> - 4.2		V <sub>CC</sub> - 1.575	V
Input Current	I <sub>IN</sub>	V <sub>IL(MIN)</sub> , V <sub>IH(MAX)</sub>	-300		+300	-300		+300	-300		+300	μA
<b>DIFFERENTIAL INPUTS (CLK, <math>\overline{\text{CLK}}</math>)</b>												
Single-Ended Input High Voltage	V <sub>IH</sub>	$\overline{\text{CLK}}$ connected to V <sub>BB</sub> , Figure 1	V <sub>CC</sub> - 1.095		V <sub>CC</sub>	V <sub>CC</sub> - 1.125		V <sub>CC</sub>	V <sub>CC</sub> - 1.125		V <sub>CC</sub>	V
Single-Ended Input Low Voltage	V <sub>IL</sub>	$\overline{\text{CLK}}$ connected to V <sub>BB</sub> , Figure 1 (V <sub>CC</sub> - V <sub>EE</sub> ) ≤ 4.2V	V <sub>EE</sub>		V <sub>CC</sub> - 1.495	V <sub>EE</sub>		V <sub>CC</sub> - 1.495	V <sub>EE</sub>		V <sub>CC</sub> - 1.575	V
		$\overline{\text{CLK}}$ connected to V <sub>BB</sub> , Figure 1 (V <sub>CC</sub> - V <sub>EE</sub> ) > 4.2V	V <sub>CC</sub> - 4.2		V <sub>CC</sub> - 1.495	V <sub>CC</sub> - 4.2		V <sub>CC</sub> - 1.495	V <sub>CC</sub> - 4.2		V <sub>CC</sub> - 1.575	V
High Voltage of Differential Input	V <sub>IHD</sub>		V <sub>EE</sub> + 1.2		V <sub>CC</sub>	V <sub>EE</sub> + 1.2		V <sub>CC</sub>	V <sub>EE</sub> + 1.2		V <sub>CC</sub>	V
Low Voltage of Differential Input	V <sub>I LD</sub>		V <sub>EE</sub>		V <sub>CC</sub> - 0.095	V <sub>EE</sub>		V <sub>CC</sub> - 0.095	V <sub>EE</sub>		V <sub>CC</sub> - 0.095	V

# 1:5 Differential (LV)PECL/(LV)ECL/ HSTL Clock and Data Driver

**MAX9316A**

## DC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} - V_{EE} = 3.0V$  to  $5.5V$ , outputs loaded with  $50\Omega \pm 1\%$  to  $V_{CC} - 2V$ , SEL = high or low,  $\overline{EN} =$  low, unless otherwise noted. Typical values are at  $V_{CC} - V_{EE} = 5.0V$ ,  $V_{IHD} = V_{CC} - 1V$ ,  $V_{ILD} = V_{CC} - 1.5V$ .) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input Voltage	$V_{IHD} - V_{ILD}$		0.095		3.0	0.095		3.0	0.095		3.0	V
Input Current	$I_{IN}$	$V_{IH}, V_{IL}, V_{IHD}, V_{ILD}$	-300		+300	-300		+300	-300		+300	$\mu A$
<b>OUTPUTS (<math>Q_{-}, \overline{Q}_{-}</math>)</b>												
Single-Ended Output High Voltage	$V_{OH}$	Figure 1	$V_{CC} - 1.085$		$V_{CC} - 0.865$	$V_{CC} - 1.025$		$V_{CC} - 0.865$	$V_{CC} - 1.025$		$V_{CC} - 0.865$	V
Single-Ended Output Low Voltage	$V_{OL}$	Figure 1	$V_{CC} - 1.910$		$V_{CC} - 1.555$	$V_{CC} - 1.840$		$V_{CC} - 1.620$	$V_{CC} - 1.810$		$V_{CC} - 1.620$	V
Differential Output Voltage	$V_{OH} - V_{OL}$	Figure 1	550		910	550		910	550		910	mV
<b>REFERENCE (<math>V_{BB}</math>)</b>												
Reference Voltage Output (Note 4)	$V_{BB}$	$I_{BB} = \pm 0.5mA$	$V_{CC} - 1.40$		$V_{CC} - 1.19$	$V_{CC} - 1.40$		$V_{CC} - 1.22$	$V_{CC} - 1.48$		$V_{CC} - 1.22$	V
<b>POWER SUPPLY</b>												
Supply Current (Note 5)	$I_{EE}$			30	40		32	40		34	43	mA

# 1:5 Differential (LV)PECL/(LV)ECL/ HSTL Clock and Data Driver

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} - V_{EE} = 3.0V$  to  $5.5V$ , outputs are loaded with  $50\Omega \pm 1\%$  to  $V_{CC} - 2V$ , input frequency  $\leq 1.5GHz$ , input transition time =  $125ps$  (20% to 80%), SEL = high or low,  $\overline{EN} = low$ ,  $V_{IHD} = V_{EE} + 1.2V$  to  $V_{CC}$ ,  $V_{ILD} = V_{EE}$  to  $V_{CC} - 0.15V$ ,  $V_{IHD} - V_{ILD} = 0.15V$  to  $3V$ , unless otherwise noted. Typical values are at  $V_{CC} - V_{EE} = 5.0V$ .) (Notes 1, 6)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
CLK to Q_ Delay (Differential)	t <sub>PLHD1</sub> , t <sub>PHLD1</sub>	Figure 2	290	400		310	440		300	520		ps
SCLK to Q_ Delay	t <sub>PLHD3</sub> , t <sub>PHLD3</sub>	$V_{IL} = V_{CC} - 1.55V$ , $V_{IH} = V_{CC} - 1.09V$ , Figure 3	290	400		310	440		300	520		ps
Output-to-Output Skew (Note 7)	t <sub>SKOO</sub>			5	30		20	40		20	50	ps
Part-to-Part Skew (Note 8)	t <sub>SKPP</sub>				110			130			220	ps
Added Random Jitter (Note 9)	t <sub>RJ</sub>	f <sub>IN</sub> = 1.5GHz clock		0.8	1.2		0.8	1.2		0.8	1.2	ps (RMS)
Added Deterministic Jitter (Note 9)	t <sub>DJ</sub>	1.5Gbps 2E <sup>23</sup> - 1 PRBS pattern		50	70		50	70		50	70	P <sub>SP-P</sub>
Switching Frequency	f <sub>MAX</sub>	( $V_{OH} - V_{OL}$ ) $\geq 400mV$ , Figure 2		1.5			1.5			1.5		GHz
Output Rise/Fall Time (20% to 80%)	t <sub>R</sub> , t <sub>F</sub>	Figure 2	80		120	90		130	90		145	ps

**Note 1:** Measurements are made with the device in thermal equilibrium.

**Note 2:** Current into a pin is defined as positive. Current out of a pin is defined as negative.

**Note 3:** DC parameters are production tested at  $T_A = +25^\circ C$  and guaranteed by design over the full operating temperature range.

**Note 4:** Use  $V_{BB}$  only for inputs that are on the same device as the  $V_{BB}$  reference.

**Note 5:** All pins are open except  $V_{CC}$  and  $V_{EE}$ .

**Note 6:** Guaranteed by design and characterization. Limits are set at  $\pm 6$  sigma.

**Note 7:** Measured between outputs of the same part at the signal crossing points for a same-edge transition.

**Note 8:** Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.

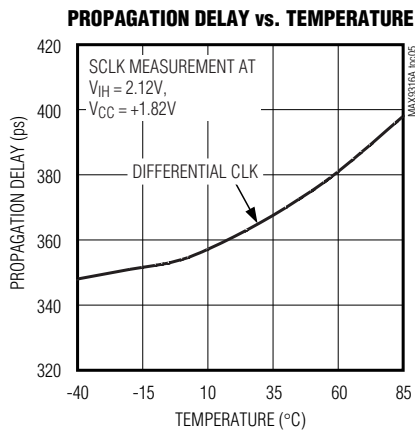
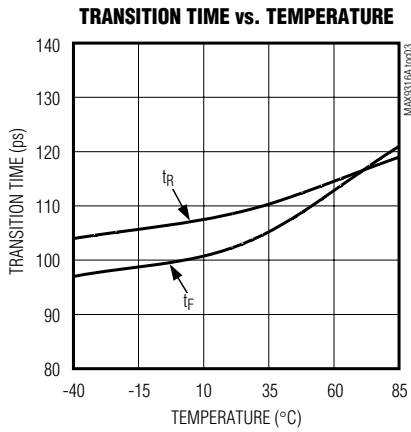
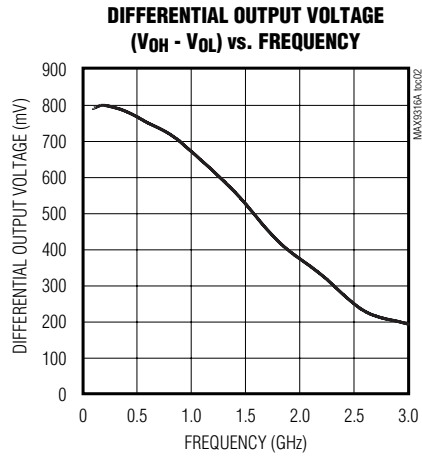
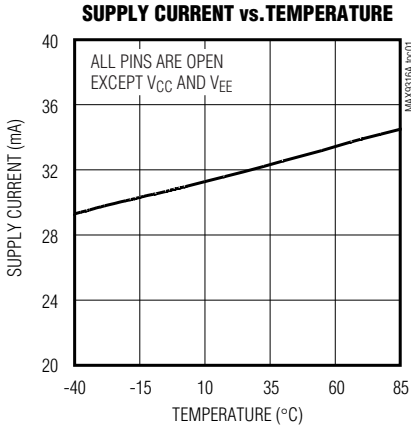
**Note 9:** Device jitter added to a jitter-free input signal.

# 1:5 Differential (LV)PECL/(LV)ECL/ HSTL Clock and Data Driver

MAX9316A

## Typical Operating Characteristics

( $V_{CC} = 5.0V$ ,  $V_{IHD} = V_{CC} - 1V$ ,  $V_{ILD} = V_{CC} - 1.15V$ , input transition time = 125ps (20% to 80%),  $f_{IN} = 1.5GHz$ , outputs loaded with  $50\Omega$  to  $(V_{CC} - 2V)$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# 1:5 Differential (LV)PECL/(LV)ECL/ HSTL Clock and Data Driver

## Pin Description

PIN	NAME	FUNCTION
1	Q0	Noninverting Q0 Output. Typically terminate with 50Ω resistor to (V <sub>CC</sub> - 2V).
2	$\overline{Q0}$	Inverting Q0 Output. Typically terminate with 50Ω resistor to (V <sub>CC</sub> - 2V).
3	Q1	Noninverting Q1 Output. Typically terminate with 50Ω resistor to (V <sub>CC</sub> - 2V).
4	$\overline{Q1}$	Inverting Q1 Output. Typically terminate with 50Ω resistor to (V <sub>CC</sub> - 2V).
5	Q2	Noninverting Q2 Output. Typically terminate with 50Ω resistor to (V <sub>CC</sub> - 2V).
6	$\overline{Q2}$	Inverting Q2 Output. Typically terminate with 50Ω resistor to (V <sub>CC</sub> - 2V).
7	Q3	Noninverting Q3 Output. Typically terminate with 50Ω resistor to (V <sub>CC</sub> - 2V).
8	$\overline{Q3}$	Inverting Q3 Output. Typically terminate with 50Ω resistor to (V <sub>CC</sub> - 2V).
9	Q4	Noninverting Q4 Output. Typically terminate with 50Ω resistor to (V <sub>CC</sub> - 2V).
10	$\overline{Q4}$	Inverting Q4 Output. Typically terminate with 50Ω resistor to (V <sub>CC</sub> - 2V).
11	V <sub>EE</sub>	Negative Supply Voltage
12	SEL	Clock Select Input (Single Ended). Drive low to select the CLK, $\overline{CLK}$ input. Drive high to select the SCLK input. The SEL threshold is equal to V <sub>BB</sub> . Internal 30kΩ pulldown to V <sub>EE</sub> and 30kΩ pullup to V <sub>CC</sub> .
13	V <sub>BB</sub>	Reference Output Voltage. Connect to the inverting or noninverting clock input to provide a reference for single-ended operation. When used, bypass with a 0.01μF ceramic capacitor to V <sub>CC</sub> ; otherwise, leave it unconnected.
14	$\overline{CLK}$	Inverting Differential Clock Input. Internal 45kΩ pullup to V <sub>CC</sub> and 45kΩ pulldown to V <sub>EE</sub> .
15	CLK	Noninverting Differential Clock Input. Internal 30kΩ pulldown to V <sub>EE</sub> and 45kΩ pullup to V <sub>CC</sub> .
16	SCLK	Single-Ended Clock Input. Internal 30kΩ pulldown to V <sub>EE</sub> and 45kΩ pullup to V <sub>CC</sub> .
17	N.C.	Not Internally Connected. Solder to PC board for package thermal dissipation.
18, 20	V <sub>CC</sub>	Positive Supply Voltage. Bypass V <sub>CC</sub> to V <sub>EE</sub> with 0.1μF and 0.01μF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
19	$\overline{EN}$	Output Enable Input. Outputs are synchronously enabled on the falling edge of the clock input when $\overline{EN}$ is low. Outputs are synchronously set to low on the falling edge of the clock input when $\overline{EN}$ is high. Internal 30kΩ pulldown to V <sub>EE</sub> and 30kΩ pullup to V <sub>CC</sub> .

### Detailed Description

The MAX9316A is a low-skew, 1-to-5 differential driver designed for clock or data distribution. A 2-to-1 MUX selects one of the two clock inputs, CLK,  $\overline{CLK}$  and SCLK. The CLK and  $\overline{CLK}$  inputs are differential while the SCLK is single ended. The MUX is switched by the single-ended SEL input. A logic low selects the CLK input and a logic high selects the SCLK input. The SEL logic threshold is set by the internal voltage reference V<sub>BB</sub>. SEL input can be driven by V<sub>CC</sub> and V<sub>EE</sub> or by a single-ended (LV)PECL/(LV)ECL signal. The selected input is reproduced at five differential outputs, Q0 to Q4.

### Synchronous Enable

The MAX9316A is synchronously enabled and disabled with outputs in the low state to eliminate shortened clock pulses.  $\overline{EN}$  is connected to the input of an edge-triggered D flip-flop. After power-up, drive  $\overline{EN}$  low and toggle the selected clock input to enable the outputs. The outputs are enabled on the falling edge of the selected clock input after  $\overline{EN}$  goes low. The outputs are disabled to a low state on the falling edge of the selected clock input after  $\overline{EN}$  goes high. The threshold for  $\overline{EN}$  is equal to V<sub>BB</sub>.

### Power Supply

For interfacing to differential HSTL and (LV)PECL signals, the V<sub>CC</sub> range is from 3.0 to 5.5V (with V<sub>EE</sub>

# 1:5 Differential (LV)PECL/(LV)ECL/ HSTL Clock and Data Driver

MAX9316A

grounded), allowing high-performance clock or data distribution in systems with a nominal 5.0V supply. For interfacing to differential (LV)ECL, the  $V_{EE}$  range is -3.0V to -5.5V (with  $V_{CC}$  grounded). Output levels are referenced to  $V_{CC}$  and are considered (LV)PECL or (LV)ECL, depending on the level of the  $V_{CC}$  supply. With  $V_{CC}$  connected to a positive supply and  $V_{EE}$  connected to ground, the outputs are (LV)PECL. The outputs are (LV)ECL when  $V_{CC}$  is connected to ground and  $V_{EE}$  is connected to a negative supply.

## Input Bias Resistors

When the CLK and  $\overline{\text{CLK}}$  inputs are open, the internal bias resistors set the inputs to differential low state. The inverting input ( $\overline{\text{CLK}}$ ) is biased with a 45k $\Omega$  pullup to  $V_{CC}$  and a 45k $\Omega$  pulldown to  $V_{EE}$ . The noninverting input (CLK) and SCLK are biased with a 45k $\Omega$  pullup to  $V_{CC}$  and a 30k $\Omega$  pulldown to  $V_{EE}$ . The single-ended inputs (SEL,  $\overline{\text{EN}}$ ) are each biased with a 30k $\Omega$  pulldown to  $V_{EE}$  and a 30k $\Omega$  pullup to  $V_{CC}$ .

## Differential Clock Input Limits

The maximum magnitude of the differential signal applied to the differential clock input is 3.0V. This limit also applies to the difference between any reference voltage input and a single-ended input. Specifications for the high and low voltages of a differential input ( $V_{IHD}$  and  $V_{ILD}$ ) and the differential input voltage ( $V_{IHD} - V_{ILD}$ ) apply simultaneously.

## Single-Ended Clock Input and $V_{BB}$

The differential clock input can be configured to accept a single-ended input. This is accomplished by connecting the on-chip reference voltage,  $V_{BB}$ , to the inverting or noninverting input of the differential input as a reference. For example, the differential CLK,  $\overline{\text{CLK}}$  input is converted to a noninverting, single-ended input by connecting  $V_{BB}$  to  $\overline{\text{CLK}}$  and connecting the single-ended input signal to CLK. Similarly, an inverting configuration is obtained by connecting  $V_{BB}$  to CLK and connecting the single-ended input to  $\overline{\text{CLK}}$ . With a differential input configured as single ended (using  $V_{BB}$ ), the single-ended input can be driven to  $V_{CC}$  and  $V_{EE}$  or with a single-ended (LV)PECL/(LV)ECL signal. Note that the single-ended input must be least  $V_{BB} \pm 95\text{mV}$  or a differential input of at least 95mV to switch the outputs to the  $V_{OH}$  and  $V_{OL}$  levels specified in the *DC Electrical Characteristics* table.

When using the  $V_{BB}$  reference output, bypass it with a 0.01 $\mu\text{F}$  ceramic capacitor to  $V_{CC}$ . If the  $V_{BB}$  reference is not used, leave it open. The  $V_{BB}$  reference can source or sink 0.5mA. Use  $V_{BB}$  only for an input that is on the same device as the  $V_{BB}$  reference.

## Applications Information

### Supply Bypassing

Bypass  $V_{CC}$  to  $V_{EE}$  with high-frequency, surface-mount, ceramic, 0.1 $\mu\text{F}$  and 0.01 $\mu\text{F}$  capacitors in parallel as close to the device as possible, with the 0.01 $\mu\text{F}$  capacitor closest to the device. Use multiple parallel vias to minimize parasitic inductance. When using the  $V_{BB}$  reference output, bypass it with a 0.01 $\mu\text{F}$  ceramic capacitor to  $V_{CC}$  (if the  $V_{BB}$  reference is not used, it can be left open).

### Controlled-Impedance Traces

Input and output trace characteristics affect the performance of the MAX9316A. Connect input and output signals with 50 $\Omega$  characteristic impedance traces. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50 $\Omega$  characteristic impedance through cables and connectors. Reduce skew within a differential pair by matching the electrical length of the traces.

### Output Termination

Terminate outputs with 50 $\Omega$  to  $V_{CC} - 2\text{V}$  or use an equivalent Thevenin termination. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if Q0 is used as a single-ended output, terminate both Q0 and  $\overline{\text{Q0}}$ .

## Chip Information

TRANSISTOR COUNT: 616

PROCESS: Bipolar

# 1:5 Differential (LV)PECL/(LV)ECL/ HSTL Clock and Data Driver

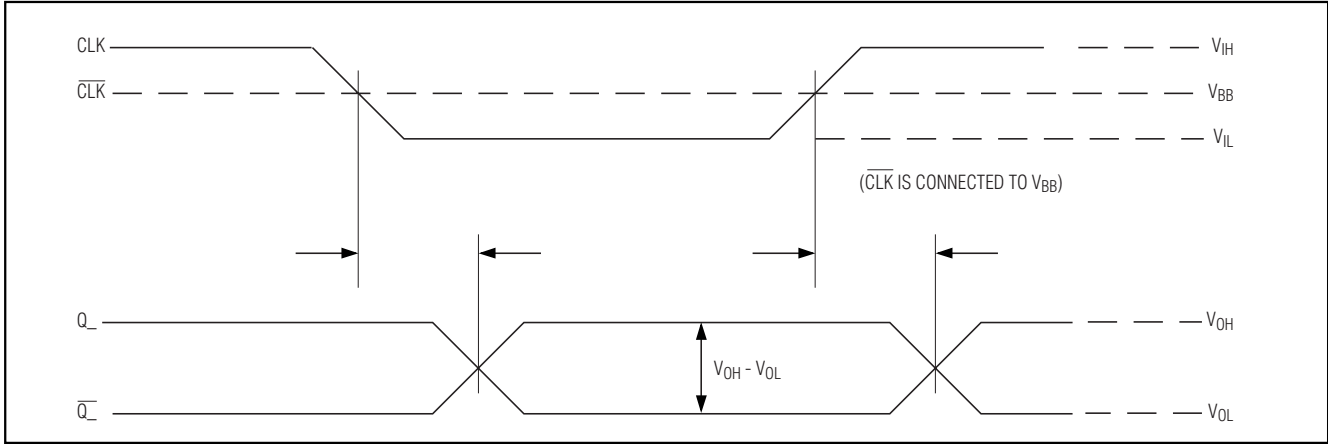


Figure 1. MAX9316A Switching Characteristics with Single-Ended Input

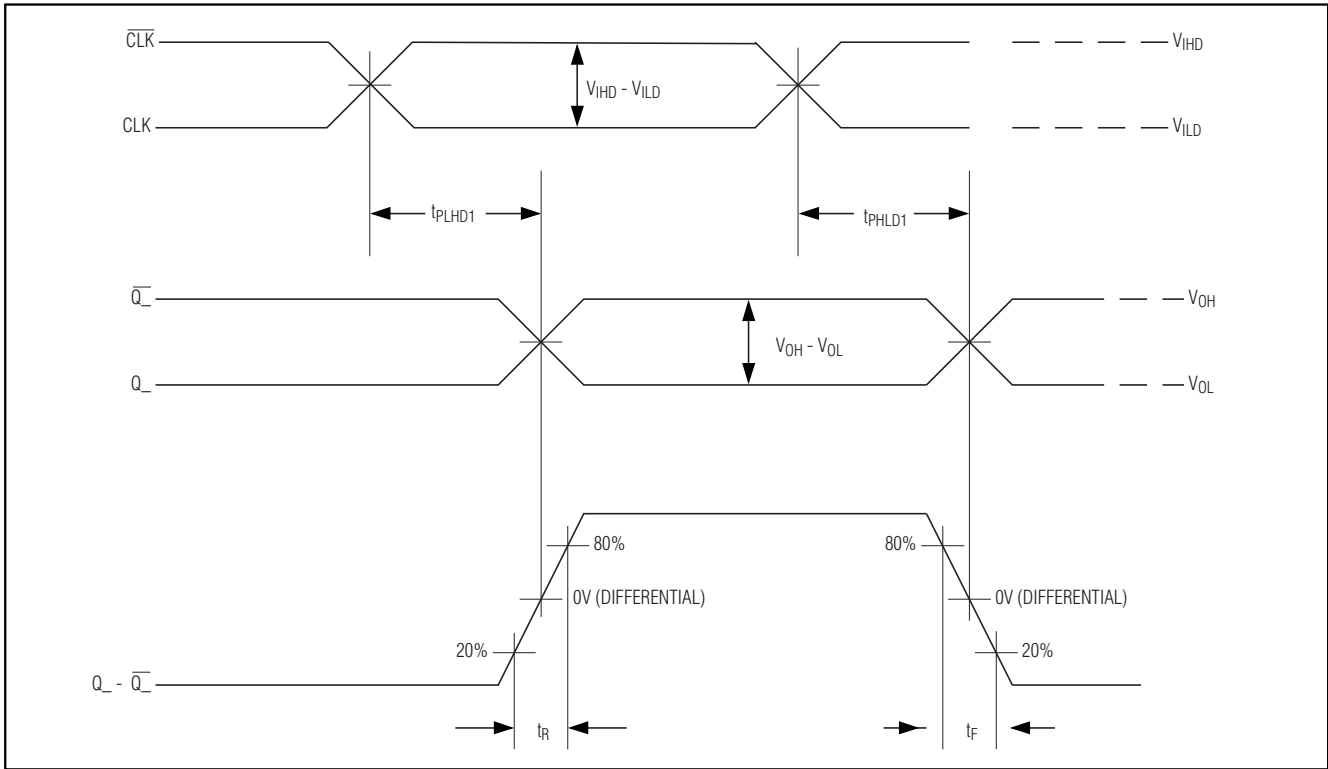


Figure 2. MAX9316A Timing Diagram



# 1:5 Differential (LV)PECL/(LV)ECL/ HSTL Clock and Data Driver

MAX9316A

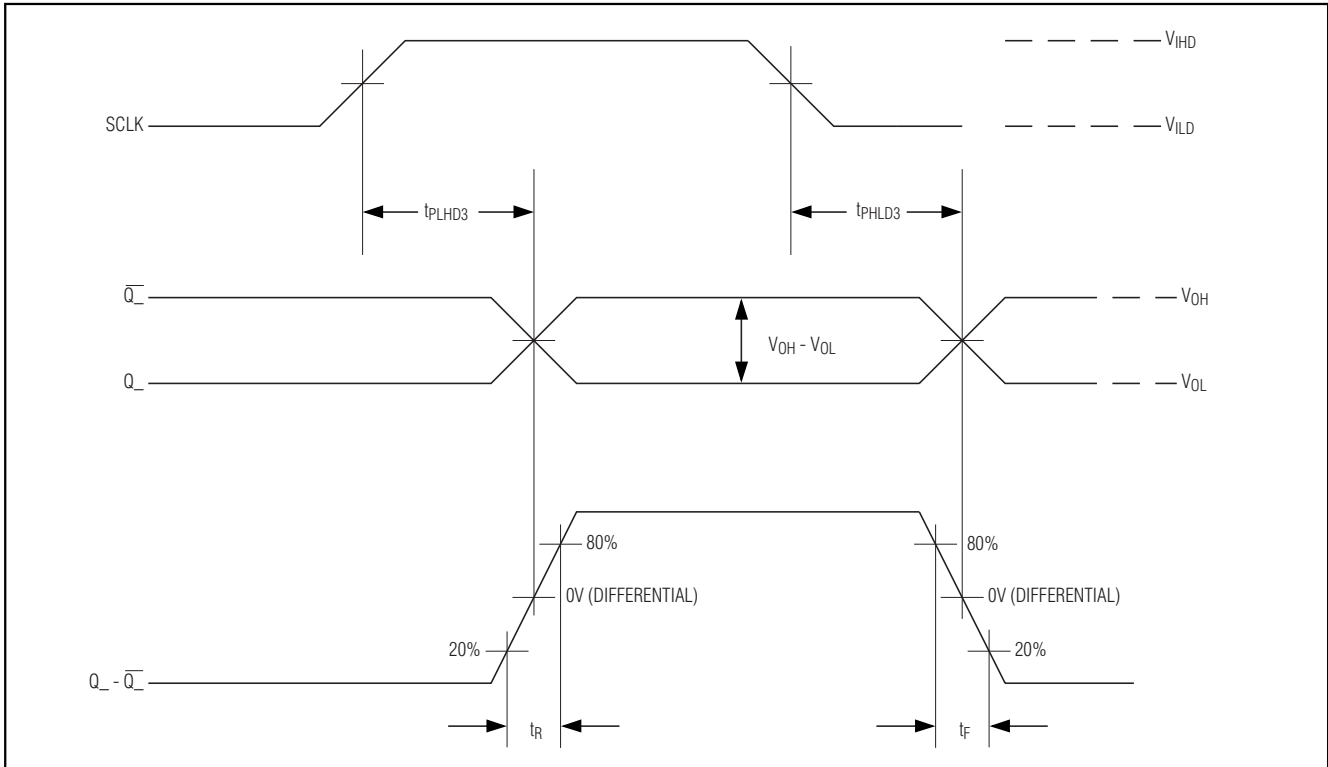


Figure 3. MAX9316A Timing Diagram for SCLK

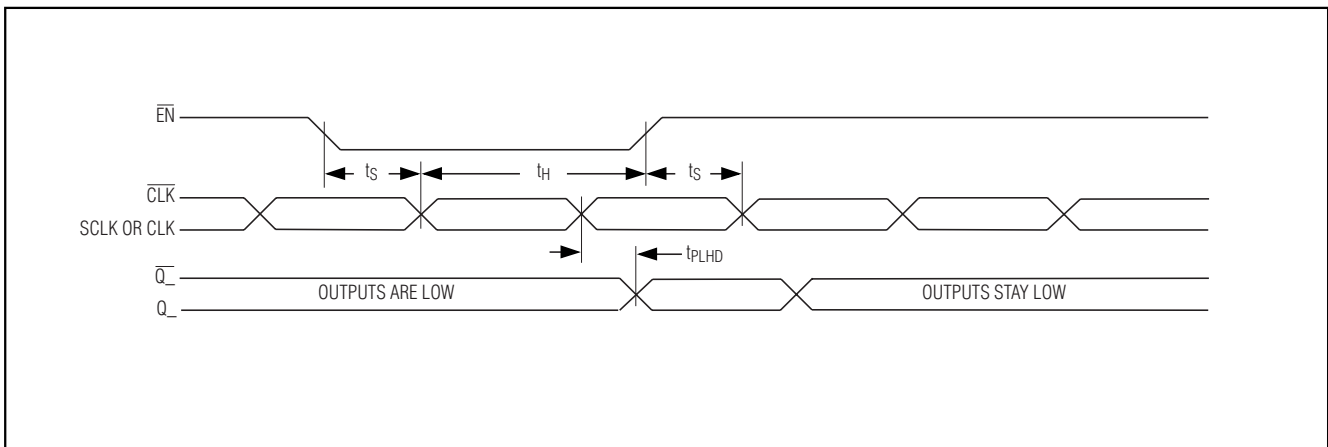
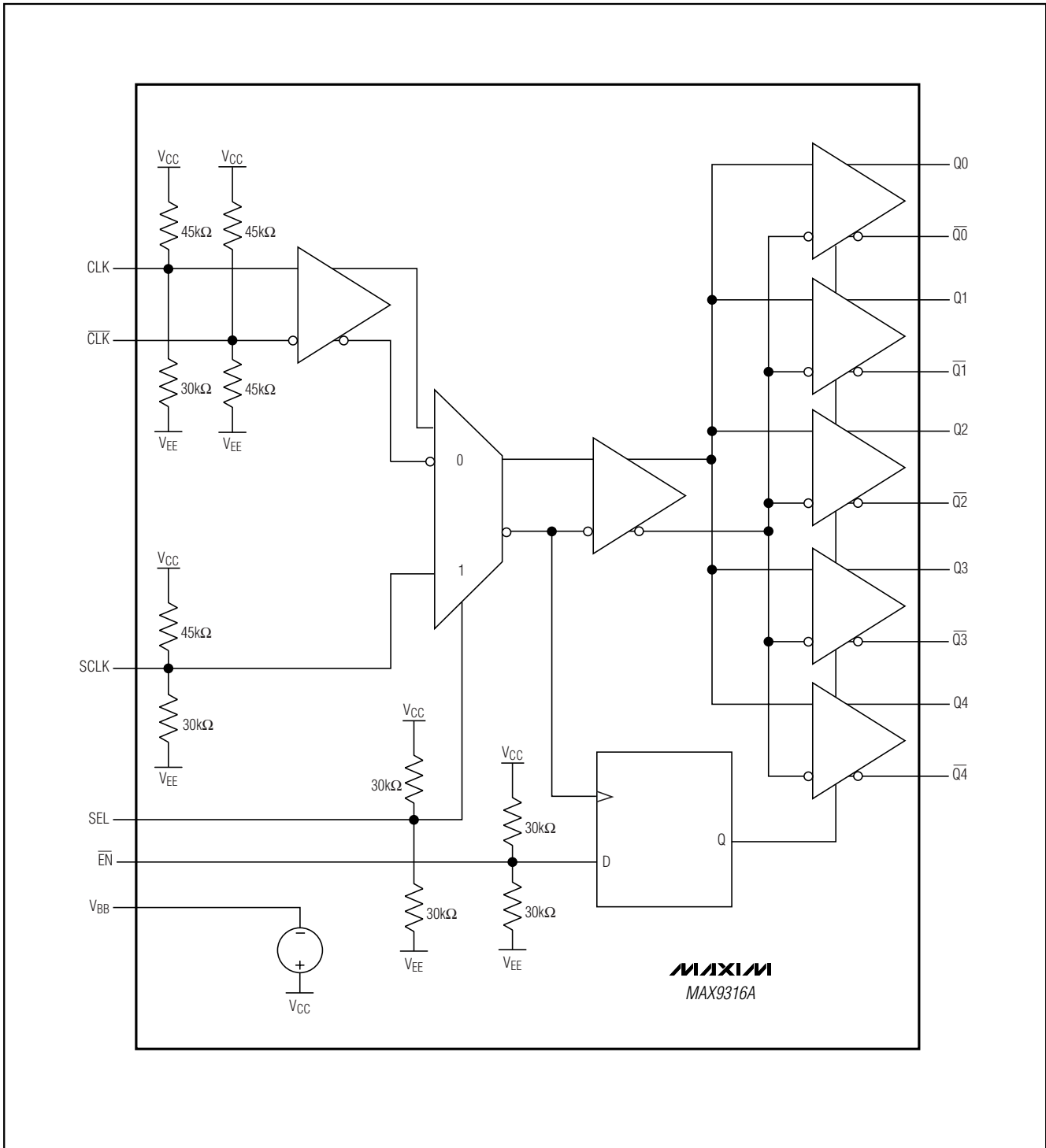


Figure 4. MAX9316A  $\bar{EN}$  Timing Diagram

# 1:5 Differential (LV)PECL/(LV)ECL/ HSTL Clock and Data Driver

## Functional Diagram

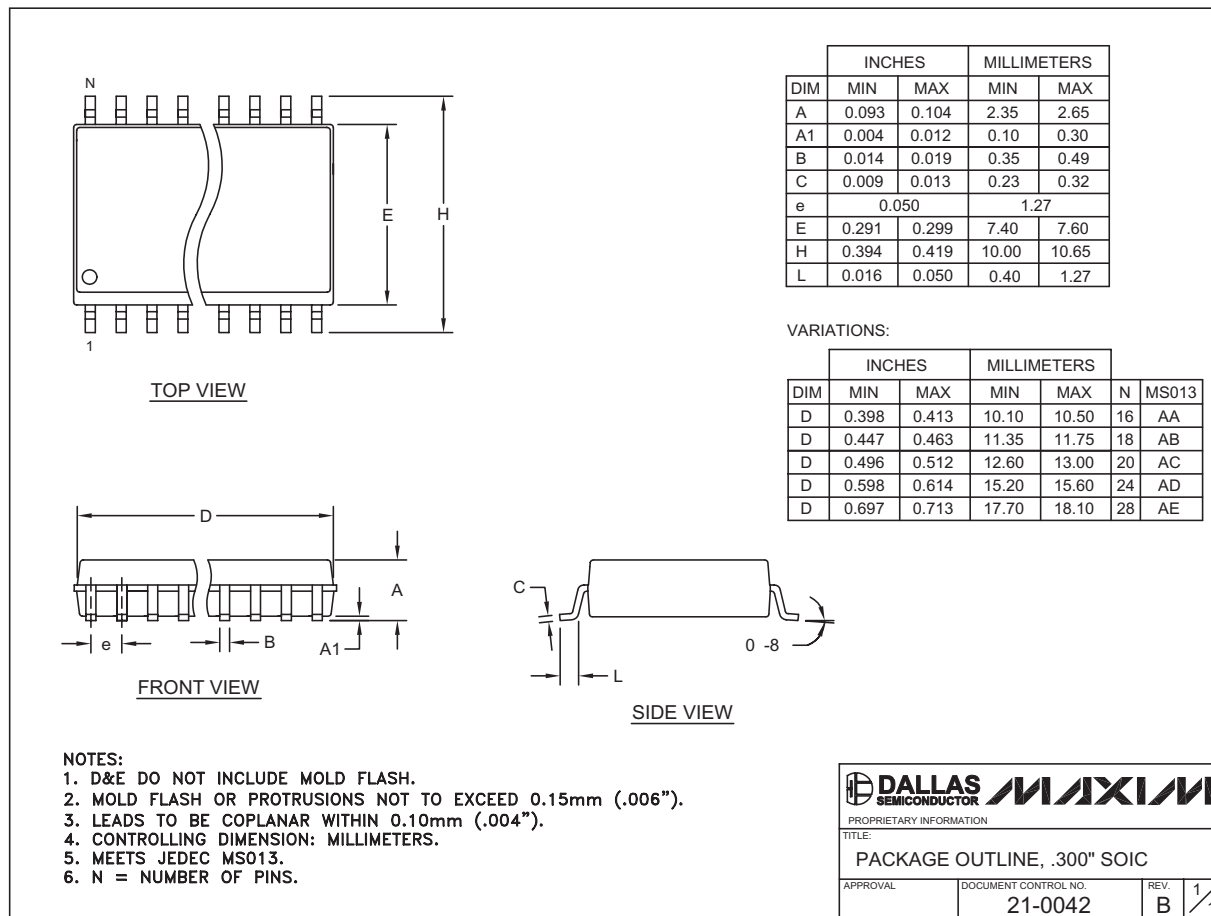


# 1:5 Differential (LV)PECL/(LV)ECL/ HSTL Clock and Data Driver

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

**MAX9316A**



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 11