MX9691A

SINGLE CHIP SOLID STATE DISK CONTROLLER

FEATURES

Host Interface

- Fully compatible with PCMCIA Release 2.1, and PC Card ATA Release 1.02 specification.
- Compatible with all PC Card Services and Socket Service.
- Fast ATA host-to-buffer burst transfer rates up to 20MB/sec. which support PIO mode 4(16.6MB/sec) and DMA mode 3(16.6MB/sec).
- Automatic sensing of PCMCIA or ATA host interface.
- Integrated PCMCIA attribute memory of 256 bytes (CIS).
  - CIS and Buffer RAM use same SRAM area to simplify internal bus design
- PCMCIA card configuration register support.
- Polarity control for host reset signal.
- PCMCIA twin card support.
- PCMCIA based ATA address decode support.
- Emulate the IBM task file for PC/AT.
- Separate status for Bus reset and Host program reset.
- Separate Host and Disk interrupt pins.

Flash Memory Interface

- Support all the control signals to execute read/write/erase operation for flash memory.
- Upto 32MB(unformatted) capacity for 16 pcs. 16Mbit flash memory or 64MB(unformatted) capacity for 16 pcs. 32Mbit flash memory.
- Flash Memory Power Down or write protect control support.
  - Don't power down the flash memory chip which used to store firmware
- Flash Memory Ready/Busy status detect.
- Inverted data bus control to reduce program operation in DOS FAT and ECC code field.
- Optional store firmware in flash memory array w/o externalROM.
  - Shadow ROM control to allow code fetch during data program or erase
- Media speed is upto 8MB/sec, sustain read data rate and 125KB/sec write data rate.

Buffer RAM control

- Dual port circular Buffer RAM control
- 1KB data Buffer RAM.
- Automatically correct error data in Buffer RAM.
  - Single word error correct and double word detect.
- Provide logic to speed up Buffer RAM access.
- Support 8 bit as well as 16 bit transfer on host bus.

DSP core

- High performance MX93011 DSP (21Mips) core.
- 4KB Internal RAM(direct access).
- 2KB Internal expansion RAM(indirect access) for store data or shadow ROM space.
- ICE debugging mode supported to ease system verification.
- Lower power and automatic power saving operation

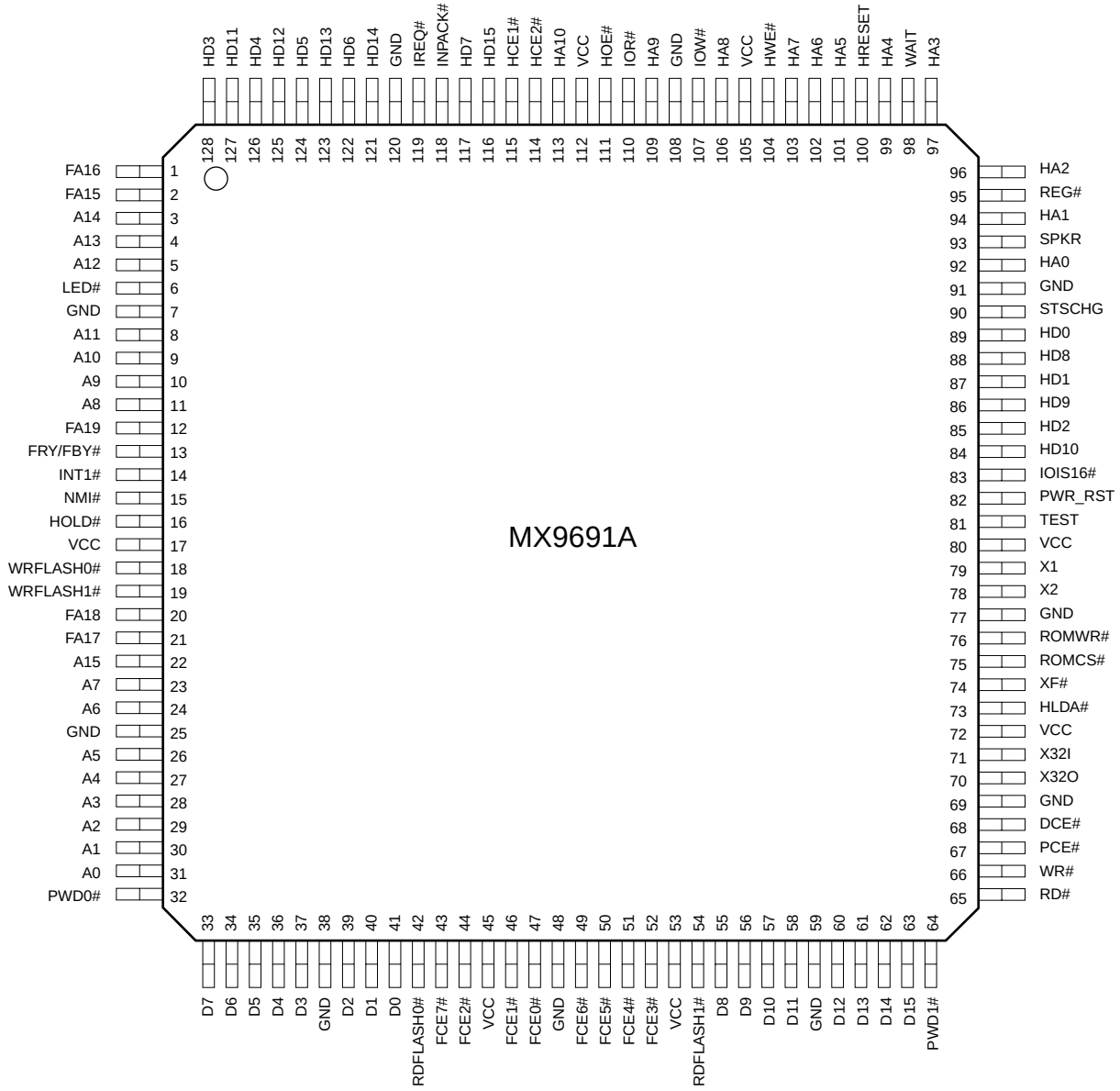
Technology

- 128 pin LQFP
- 0.6um Low-power, High-speed CMOS technology.
- 5V±10% or 3.3V±5%

Utility Support

- Upload firmware from Host.
- Physical Devices test.
- Preformat.
- CIS Manufacturer code and Model code edit.

PIN CONFIGURATION



GENERAL DESCRIPTION

The Macronix's Solid State Disk controller is fully integrated flash memory controller that provides all the control logic for a PC Card ATA flash memory. The MX9691A combines 1KB dual-port buffer and buffer manager, integrated MX93011 DSP core , and a complete host interface for both the PC Card ATA and ATA standard.

The MX9691A is typically configured with up to 32MB(unformatted) capacity for 16 pcs. 16Mbit flash memory or 64MB(unformatted) capacity for 16 pcs. 32Mbit flash memory. The MX9691A supports all the control signals to execute read/write/erase operation for flash memory chip.

The MX9691A is fully compliant with the PC Card ATA specification. It includes 256 bytes of integrated attribute memory(for the required Card Information Structure) and four Card Configuration registers. The PCMCIA device driver can access the MX9691A ATA command block through four different modes by writing the different modes by writing the configuration index of the attribute memory configuration option register.

PIN DESCRIPTION

Host Interface

Symbol	No.	Type	Description
HA[10:0]	92,94, 96-97, 99,101-103, 106,109,113	I	Host address line 10-0. These pins include internal pull-up resistors.
HD[15:0]	84-89,116-117, 121-128	I/O	Host data line 15-0. These pins include internal bus holder circuit that keep previous state when tri-state.
HOE#,HWE#	104,111	I	Host memory read/write/mode select : Both pins include internal pull-up resistors that is default in PCMCIA mode.
IOR#,IOW#	107,110	I	Host I/O access. Both pins include internal pull-up resistors.
HRESET/ HRESET#	100	I	The host reset signal, when active, initializes the control/status registers and stops any command in process.In PCMCIA mode, the signal is active high. In ATA extension mode, this signal is active low. This signal include internal pull-down resistor.
WAIT/ IOCHRDY	98	O,OD	WAIT or INPUT CHANNEL READY : In both PCMCIA and ATA extension modes, this signal holds host transfers until the controller is ready to respond.
RDY/BSY#/ IREQ#/ HOSTINT	119	O,Z	READY/BUSY or HOST INTERRUPT : In PCMCIA mode, this signal has two functions. In PCMCIA common memory mode, this signal is ready/busy. It is asserted busy by the reset logic, and can be deasserted by the local uC. In PCMCIA I/O mode, this signal is IREQ#. In ATA extension mode, this active high signal is HOSTINT, which, when enable, send an interrupt to the host.

Symbol	No.	Type	Description
WP/IOCS16#	83	O,OD	WRITE PROTECT or 16-bit I/O TRANSFER : In PCMCIA mode, this bit has two functions. In PCMCIA common-memory mode,this signal indicates write protect. In PCMCIA I/O mode, when IOIS16# is as serted low, it indicates that a 16-bit data transfer is active on PCMCIA bus. In ATA extension mode, the IOCS16# signal indicates that a 16-bit buffer transfer is active on the host bus. This open drain signal is only driven on assertion(low).
REG#/DACK#	95	I	Attribute memory and I/O select : In PCMCIA mode, this signal is used to select attribute memory and I/O space. In ATA extension mode, this signal is used during DMA with the DREQ, IOR# and IOW# signals to transfer data between the host and the MX9691A. This pin includes an internal pull-up resistor.
HCE1#/ CS1FX#	115	I	Card enable 1 or Chip select 0: In PCMCIA mode,this signal is card enable 1. This signal can enable either even or odd numbered-address bytes onto HD7:0. In ATA extension mode, this signal accesses the MX9691A command block registers. This input is ignored during DMA data transfer, i.e. when the DACK# signal is low. This pin includes an internal pull-up resistor.
HCE2#/ CS3FX#	114	I	Card enable 2 or Chip select 1: In PCMCIA mode,this signal is card enable 2. This signal can enable odd numbered-address bytes onto HD15:8. In ATA extension mode, this signal accesses the MX9691A control block registers. This pin includes an internal pull-up resistor.
INPACK#/ DREQ	118	O	Input Acknowledge or DMA request : In PCMCIA mode, this signal is asserted when the MX9691A is configured to respond to I/O card read cycles at all addresses. In ATA extension mode, this signal is DREQ and is issued during DMA transfers to indicate that the MX9691A is ready for DMA transfer.
SPKR/DASP#	93	I/O	Speaker or slave present : In PCMCIA mode, the output-enable for this signal is controlled by the card configuration registers. In ATA extension mode, this signal is used as the slave-present detector.
STSCHG/ PDIAG#	90	I/O	Status change or pass diagnostics : In PCMCIA mode, this signal is used to indicate changes in the RDY/BSY#,WP signals in card con figuration registers. In ATA extension mode, this active low signal is used between two embedded ATA drive to indicate that the drive in slave mode has passed diagnostics.

Microcontroller interface :

Symbol	No.	Type	Description
D[15:0]	33-37, 39-41, 55-58, 60-63	I/O	DSP IO/RAM/ROM/FLASH memory array external data bus. These pins in clude internal pull-up resistors.
A[15:0]	3-5, 8-11, 22-24, 26-31	I/O	In normal mode, these signals are output that used as DSP IO/RAM/ ROM external address. A14-A0 are for flash memory array address also. In upgrade mode, these address is used for ROM address that controlled by CYH,CYL registers. In ICE debugging mode, these ad dress are input,asserted by external MX93011 DSP. The internal DSP is disabled. These pins include internal pull-up resistors.
PCE#	67	I/O	In normal mode, this signal is output that is used as external program chip enable. In upgrade mode, this signal is drived to high. In ICE de bugging mode, this signal is input, asserted by external MX93011 DSP. The internal DSP is disabled. This pin includes a bus holder circuit.
DCE#	68	I/O	In normal mode, this signal is output that is used as external data chip enable. In upgrade mode, this signal is drived to high. In ICE debug ging mode, this signal is input, asserted by external MX93011 DSP. The internal DSP is disabled. This pin includes a bus holder circuit.
RD#	65	I/O	In normal mode, this signal is output that is used as DSP IO/RAM/ ROM external read. In upgrade mode, this signal is output and as serted when the data register is read in host interface. In ICE debug ging mode, this signal is input, asserted by external MX93011 DSP. The internal DSP is disabled. This pin includes a bus holder circuit.
WR#	66	I/O	In normal mode, this signal is output that is used as DSP IO/RAM/ ROM external write. In upgrade mode, this signal is drived to high. In ICE debugging mode, this signal is input, asserted by external MX93011 DSP. The internal DSP is disabled. This pin includes a bus holder cir cuit.
NMI#	15	I	Non maskable interrupt pin. This pin includes an pull-up resistor.
INT1#	14	I/O	In normal mode, this signal is input that is used as interrupt pin. Interrupt will be internally asserted also when data transfer done, or command end. In ICE debugging mode, this signal is output and as serted when data transfer done, or command end. This pin includes an pull-up resistor.

Symbol	No.	Type	Description
HOLD#	16	I/O	In normal mode, this signal is input that is used as holding DSP clock down and release bus. Bus hold will be internally asserted also when upgrade mode enable. In ICE debugging mode, this signal is output and asserted when upgrade mode enable. In ICE debugging mode, this signal is output and asserted when upgrade mode enable. This pin includes an pull-up resistor.
HLDA#	73	I/O	In normal mode, this signal is output that is used as ack to HOLD# signal. This signal will be internally sent to PCMCIA/ATA interface also when upgrade mode enable. In ICE debugging mode, this signal is input and ack to HOLD# when upgrade mode enable. This pin in cludes an pull-up resistor.
XF#/CPURST#	74	O	External flag, this pin can be directly written by one DSP instruction. Default inactive (logic high). In ICE debugging mode, this signal is used to reset CPU.

Flash Memory Interface :

Symbol	No.	Type	Description
FA19/CLE	12	O	In random mode, this signal is used as flash memory chip high address line 19. In sequential mode, this signal is used as flash memory chip command latch enable.
FA18/ALE/	20	I/O	In random mode, this signal is used as flash memory chip high address line 18. In sequential mode, this signal is used as flash memory chip address latch enable. This signal is used to select whether the MX9691A initializes in normal mode or in ICE debugging mode at power-on reset. If this pin go high, then the MX9691A will switch to normal mode at power-on reset,and if this pin remains low, then the MX9691 A will initializes in ICE debugging mode. This pin includes an internal pull-up resistor. ICEMODE ICE debugging mode select : ICEMODE=1 —> Normal mode ICEMODE=0 —> ICE debugging mode

Symbol	No.	Type	Description
FA17/EROM	21	I/O	This signal is used as flash memory chip high address line 17. This signal is used to select whether the firmware store in flash memory array or in separate external ROM at power-on reset. If this pin go high, then the firmware will be executed in flash memory array, and if this pin remains low, then the firmware will be executed in separate external ROM. Store firmware in external ROM or Flash memory array: EROM = 0 —> Store in External ROM EROM = 1 —> Store in flash memory array This pin includes an internal pull-up resistor.
FA[16:15]/ ATADET[1:0]	1-2	I/O	This signal is used as flash memory chip high address line 16-15. These signals are used to select configuration in ATA extension mode at power-on reset. ATADET1 is connected to DSP's IPT1. ATADET0 is connected to DSP's IPT0. VDD is connected to IPT2. Master/Slave selection in ATA mode : ATADET1 ATADET0 mode selected 1 1 one drive 0 0 master of two drives 1 0 slave of two drives This power-on configuration can be accessed from PCMCIA/ATA port 601Ch bit3-2. These pins include internal pull-up resistors.
RDFLASH1#	54	O	Flash memory ouptut enable 1 for bank1: This signal will be asserted by flash memory read operation when flash memory read address latch, port 601Dh bit 8 = 1(i.e. FA23=1). Note: Flash memory access window is mapped to 32KW data and code space 8000h~ffffh.
RDFLASH0#	42	O	Flash memory ouptut enable 0 for bank0: This signal will be asserted by flash memory read operation when flash memory read address latch, port 601Dh bit 8 = 0(i.e. FA23=0).
WRFLASH1#	19	O	Flash memory write enable 1 for bank1: This signal will be asserted by flash memory write operation when flash memory write address latch, port 601Fh bit 8 = 1(i.e. FA23=1).
WRFLASH0#	18	O	Flash memory write enable 0 for bank0: This signal will be asserted by flash memory write operation when flash memory write address latch, port 601Fh bit 8 = 0(i.e. FA23=0).

Symbol	No.	Type	Description
FCE[7:0]#	43-44,46-47, 49-52	O	Flash memory chip enable 7-0 : In random mode, These signals are decoded from port 601Dh bit 7-5 when flash memory read or port 601Fh bit 7-5 when flash memory write. Decoding combination : bit7 bit6 bit5 FCE[7:0]# 0 0 0 11111110 0 0 1 11111011 0 1 0 11101111 0 1 1 10111111 1 0 0 11111101 1 0 1 11110111 1 1 0 11011111 1 1 1 01111111 In sequential mode, These are decoded from port 601Dh bit 7-5 only when port 601Eh bit 2 is set.
PWD0#	32	O	Deep power down output 0 for bank0: This signal will put the flash memory chips of bank0 in deep power-down mode. PWD0# is active low;PWD0# high enables normal operation. PWD0# also locks out erase or program operation when active low providing data protection during power transitions. Power down pin PWD0# will be active if FA23=1.
PWD1#	64	O	Deep power down output 1 for bank1: This signal will put the flash memory chips of bank1 in deep power-down mode. PWD1# is active low;PWD1# high enables normal operation. PWD1# also locks out erase or program operation when active low providing data protection during power transitions. Power down pin PWD1# will be active if FA23=0.
FRY/FBY#	13	I	Flash memory Ready/busy input: This signal indicate the state of erase or program operation in flash memory chips.This pin includes an internal pull-up resistor.

Control ROM interface :

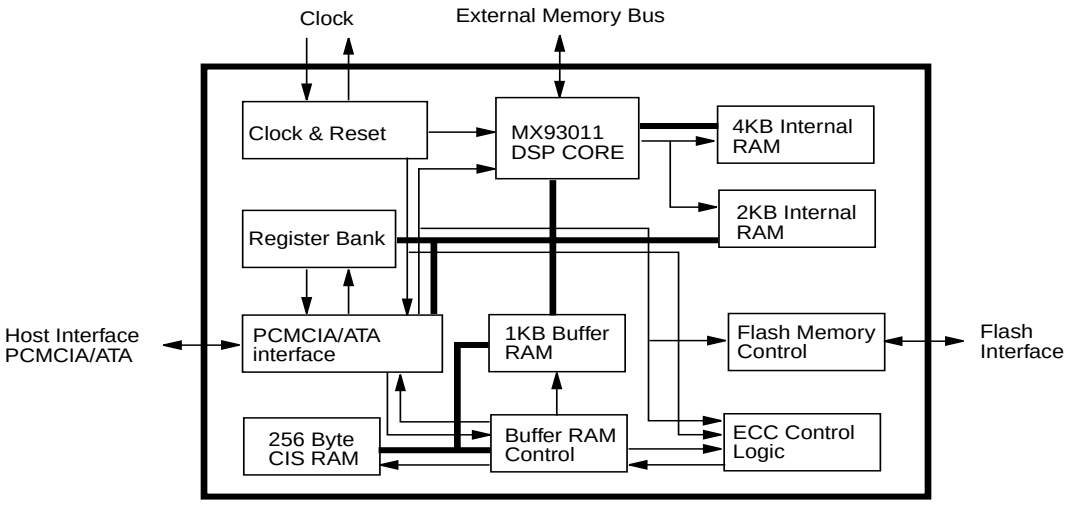
Symbol	No.	Type	Description
ROMCS#/ FWIN#	75	O	ROM chip select/Flash memory data buffer enable : In normal mode, this signal is used as ROM chip enable if firmware that stored in external ROM. In ICE debugging mode, this signal is used as flash memory data buffer (74640) enable if firmware that stored in flash memory array.
ROMWR#/ FDIR	76	O	ROM write enable/Flash memory data buffer direction control: In normal mode, this signal is used as ROM write enable if firmware that stored in external ROM. In ICE debugging mode, this signal is used as flash memory data buffer (74640) direction control if firmware that stored in flash memory array.

Miscellaneous :

Symbol	No.	Type	Description
X1	79	I	Crystal input.
X2	78	O	Crystal ouput.
X32I	71	I	32K Crystal input.
X32O	70	I	32K Crystal output.
TEST	81	I	This signal is used to select the main system clock, either from external clock source if this signal is high or from internal PLL circuit if this signal is low. This pin includes an internal pull-up resistor.
PWR_RST#	82	I	Power on reset, CMOS Schmite-triggered: The MX9691A include debouncing circuit to stabilize internal DSP reset signal.
LED#	6	O	LED output: This signal is connected to external LED in debugging system to indicate system status. The LED will be turn-on during reset. The contorl firmware will turn off the LED after H/W initialization and pass diagnostics. If system fail, the control firmware will flash the LED to indicate some error occur. This signal will be high if port 601Ch bit0 set to 1 or OPTR bit2 set to 1.
VCC	17,45,53,72, 80,105,112		5 volt or 3.3 volt Power pin
GND	7,25,38,48, 59,69,77,91, 108,120		Ground pin

Functional and Operation Description

Block Diagram



MX9691A Signal Chip Solid State Disk Controller

Power-on detection:

(1). Store firmware in external ROM or Flash memory array :

FA17/EROM = 0 —> Store in External ROM
FA17/EROM = 1 —> Store in flash memory array

(2). Master/Slave selection in ATA extension mode :

FA16/ATADET1	FA15/ATADET0	mode selected
1	1	one drive
0	0	master of two drives
1	0	slave of two drives

(3). ICE debugging mode select :

FA18/ICEMDOE = 0 —> ICE debugging mode
FA18/ICEMODE = 1 —> Normal mode

(4). Flash memory data buffer control

ROMCS# is replaced by FWIN# if ICE debugging mode & firmware in flash memory array ROMWR# is replaced by FDIR if ICE debugging mode&firmware in flash memory array

(5). PCMCIA or ATA extension select

HOE#	HWE#	mode
0	0	ATA extension mode
others		PCMCIA mode

System Memory Map :

(1). Data Space :

Address	Function & Usage
0000h~007fh	Internal RAM (128W) to store control variables
0080h~07ffh	Internal RAM(1920W) for flash memory algorithm usage
0800h~5fffh	User define (22kW)
6000h~63ffh	I/O range(1kW): ATA CTL. use I/O range (6000h~601fh)
6400h~6fffh	User define (3kW)
7000h~73ffh	User define (1kW)
7400h~77ffh	Internal RAM (1kW) for expansion RAM or shadow ROM space
7800h~7fffh	ROM Data space(2kW)
8000h~ffffh	Flash memory access windows(32kW)

(2). Program Space :

Address	Function & Usage
0000h~77ffh	ROM program space (32kW)
7800h~7fffh	Unused
8000h~ffffh	Flash memory access windows(32kW)

Registers definition:

(1). Register List :

Type of Register	Location
PCMCIA/ATA Interface	6000h, 6001h, 6002h, 6003h, 6004h, 6005h, 6006h, 6007h, 600Bh, 6010h, 6011h, 6012h, 6013h, 6019h, 601Ah, 601Bh, 601Ch
PC INTERRUPT CONTROL	6009h, 600Ah
BUFFER MANAGER AND DMA	6008h, 6014h, 6015h, 6016h, 6017h, 6018h
ECC Control	600Ch, 600Dh, 600Eh, 600Fh
Flash Memory Interface	601Dh, 601Eh, 601Fh

(2). Register Description :

Port 6000h :

Bit	Function Description
	AT CONTROL/STATUS REGISTER Default reset value : 01h
7	R/W: DRIVE READY (drive 0)
6	R/W: DRIVE SEEK COMPLETE (drive 0)
5	R/W: CORRECTED DATA
4	R: ATA INT. ENABLE
3	R: AT SOFTWARE RESET
2	R/W: HOST INTERRUPT
1	R/W: ERROR BIT
0	R/W: BUSY BIT

Port 6001h :

Bit	Function Description
	Default reset value : 00h
7:0	R/W: ERROR REGISTER (map to command block 1f1h)

Port 6002h :

Bit	Function Description
	Default reset value : 01h
7:0	R/W: SECTOR COUNT REGISTER (map to command block 1f2h)

Port 6003h :

Bit	Function Description
	Default reset value : 01h
7:0	R/W: SECTOR NUMBER REGISTER (map to command block 1f3h)

Port 6004h :

Bit	Function Description
	Default reset value : 00h
7:0	R/W: CYCLINDER LOW REGISTER (map to command block 1f4h)

Port 6005h :

Bit	Function Description
	Default reset value : 00h
7:0	R/W: CYCLINDER HIGH REGISTER (map to command block 1f5h)

Port 6006h :

Bit	Function Description
	Default reset value : A0h
7:0	R/W: DRIVE/HEAD REGISTER (map to command block 1f6h)

Port 6007h :

Bit	Function Description
	Default reset value : 00h
7:0	R: COMMAND REGISTER (map to command block 1f7h)

Port 6008h :

Bit	Function Description
	BUFFER RAM SIZE CONTROL REGISTER Default reset value : 40h
7	R/W: TEST MODE 1 for HAP/DAP test 0 : DISABLE 1 : ENABLE
6	R/W: BIT WRITE GATE STATE OF DRIVE 0 : ENABLE 1 : DISABLE

Bit	Function Description
5	R: PCMCIA/ATA 0 : ATA extension mode 1 : PCMCIA mode
4	R/W: Auto DAP increment 0 : Disable 1 : Enable
3	R/W: Shadow ROM control 0 : Disable 1 : Enable
2:0	R/W: BUFFER RAM SIZE CONTROL 00x : 32KW 010 : 16KW 011 : 8KW 100 : 4KW 101 : 2KW 110 : 1KW 111 : 512W

Port 6009h :

Bit	Function Description
	HOST INTERRUPT STATUS Default reset value : 00h
7	R: Power-Down timer time-out detected
6	R: Card configuration register write detected
5	R: CIS accessed detected
4	R: Hreset detected
3	R: PC SRST(or PCMCIA SRST) DETECTED
2	R: PC STATUS READ DETECTED
1	R: PC SELECTION
0	R: PC TRANSFER DONE

Port 600Ah :

Bit	Function Description
	HOST INTERRUPT ENABLE
	Default reset value : 00h
7	R/W: Power-Down timer time-out detected enable.
6	R/W: Card configuration register write detected enable
5	R/W: CIS accessed detected enable
4	R/W: Hreset detected enable
3	R/W: PC SRST(PCMCIA SRST) DETECTED ENABLE
2	R/W: PC STATUS READ DETECTED ENABLE
1	R/W: PC SELECTION ENABLE
0	R/W: PC TRANSFER DONE ENABLE

Port 600Bh :

Bit	Function Description
	Default reset value : 00h
7:0	R: Feature register (map to command block 1f1h)

Port 600Ch :

Bit	Function Description
	ECC CONTROL REGISTER
	Default reset value : 00h
7	R/W: ECC FUNCTION SUSPEND
	0 : NORMAL
	1 : SUSPEND
6	R/W: CORRECTION SPEED SELECT
	0 : FULL SPEED
	1 : HALF SPEED
5	R/W: ENCODE/DECODE FUNCTION SELECTION
	0 : ENCODE
	1 : DECODE
4	R/W: RESET ECC CIRCUIT
	0 : RESET
	1 : NORMAL
3	R: UNCORRECTABLE ERROR FLAG
2	R: CORRECTABLE ERROR FLAG
1	R: CORRECTION DONE FLAG
0	R/W: START ECC CORRECT FUNCTION ENABLE/DISABLE
	0 : DISABLE
	1 : ENABLE

Port 600Dh :

Bit	Function Description
	Default reset value : 0000h
15:0	R/W : ECC 0 REGISTER

Port 600Eh :

Bit	Function Description
	Default reset value : 0000h
15:0	R/W : ECC 1 REGISTER

Port 600Fh :

Bit	Function Description
	Default reset value : 0000h
15:0	R/W : ECC 2 REGISTER

Port 6010h :

Bit	Function Description
	Default reset value : 00h
7:0	R: Configuration Option register (map to attribute memory 200h)

Port 6011h :

Bit	Function Description
	Default reset value : 00h
7:0	R: Card Configuration and status register (map to attribute memory 202h)

Port 6012h :

Bit	Function Description
	Default reset value : 0Ch
7:0	R: Pin replacement register (map to attribute memory 204h)

Port 6013h :

Bit	Function Description
	Default reset value : 00h
7:0	R: Socket and copy register (map to attribute memory 206h)

Port 6014h :

Bit	Function Description
	Default reset value : 0000h
15:0	R/W : HOST ADDRESS POINTER

Port 6015h :

Bit	Function Description
	Default reset value : 00ffh
15:0	R/W : AT STOP POINTER

Port 6016h :

Bit	Function Description
	Default reset value : 0000h
15:0	R/W : DISK ADDRESS POINTER

Port 6017h :

Bit	Function Description
	DMA CONTROL REGISTER
	Default reset value : 08h
7	R/W: DRIVE READY (drive 1)
6	R/W: DRIVE SEEK COMPLETE (drive 1)
5	R/W: set BSY upon XFER done
	0 : DISABLE
	1 : ENABLE
4	R/W: ENABLE AUTO INTERRUPTS - AT ONLY
	0 : DISABLE
	1 : ENABLE
3	R/W: BUFFER RAM CHIP ENABLE
	0 : ENABLE
	1 : DISABLE
2	R/W: HOST BUS DIRECTION
	0 : START BUFFER -> AT BUS
	1 : START AT BUS -> BUFFER WHEN SET
1	R: A COMPLETION OF AT DMA XFER
0	R/W: START DATA TRANSFER BETWEEN AT BUS AND BUFFER RAM
	0 : DISABLE
	1 : ENABLE

Port 6018h :

Bit	Function Description
15:0	R/W : ACCESS PORT INTO BUFFER RAM

Port 6019h :

Bit	Function Description
	PCMCIA control register
7	R: ATA extension mode
6	R: Common memory mode
5	R: I/O mode
4	R/W: host ready
3	R/W: no drive address
2	R/W: Internal registers write pulse width 0 : 2 system clock 1 : 1 system clock
1	R/W: Force ATA mode
0	R/W: Force PCMCIA mode

Port 601Ah :

Bit	Function Description
	Auxi_ctl_1 reg. Default reset value : 00h
7	R/W : DASP
6	R/W : Host Interrupt level mode or pulse mode select 0: Level mode 1: Pulse mode
5	R/W : PDIAG
4	R/W : DASP output enable
3	R/W: write protect enable 0: Disable 1: Enable
2	R/W: PDIAG output enable
1	R/W: master/slave mode enable 0: Disable 1: Enable
0	R/W: master/salve of ATA mode 0: master 1: slave

Port 601Bh :

Bit	Function Description
	Auxi_ctl_2 reg. Default reset value : 00h
7:4	Reserved.
3	R/W: Force the CPU that fetch codes from flash memory array
2	R/W: Force the system that become ICE debugging mode
1	R/W: Host interface RESET polarity 0: Low active 1: High active
0	R/W: Disk interrupt polarity 0: Low active 1: High active

Port 601Ch :

Bit	Function Description
	Auxi_ctl_3 reg. Default reset value : 0000h
15	Reserved
14	R/W : Test mode 2 for timer 0 : Normal mode 1 : Test mode enable
13	R : DRQ
12	R : Time out status 1 : Time out event occurence
11	R/W: Timer enable/disable 0 : Disable 1 : Enable

Port 601Ch :

Bit	Function Description
10:9	R/W: Power-down timer time-out select for 25MHz main clock 00 : 16 x 1.28 = 20.48 sec. 01 : 8 x 1.28 = 10.24 sec. 10 : 4 x 1.28 = 5.12 sec. 11 : 2 x 1.28 = 2.56 sec.
8	R : ICE debugging mode detected 0 : ICE debugging mode 1 : Normal
7	R/W : Inverted data bus for access flash memory. 0 : Inverted 1 : Non-inverted
6	R: External ROM detect. 0: Firmware stored in external ROM 1: Firmware stored in flash memory array
5:4	R/W: Shadow ROM space control 00 : 512 bytes, Range: 7400h ~ 74ffh 01 : 1Kbytes, Range: 7400h ~ 75ffh 10 : 1.5Kbytes, Range: 7400h ~ 76ffh 11 : 2Kbytes, Range: 7400h ~ 77ffh
3:2	R : Master/Slave mode detect in ATA mode 00 : Master of two drives 10 : Slave of two drives 11 : One drive
1	R/W: PIO/DMA mode select 0: PIO mode 1: DMA mode
0	R/W: LED output

Port 601Dh :

Bit	Function Description
	Default reset value : 0000h
9:0	R/W : Flash memory Read address FA[24:15] latch for random mode When data space 8000h ~ ffffh is read, the output of the flash memory read address latch will be used.

For sequential mode this register has different definitions

9:8	Reserved
7:5	R/W: FCE select for sequential mode 000: FCE0 001: FCE2 010: FCE4 011: FCE6 100: FCE1 101: FCE3 110: FCE5 111: FCE7
4	R/W: Command latch enable (FA19/CLE) 0 : Disable 1 : Enable
3	R/W: Address latch enable (FA18/ALE) 0 : Disable 1 : Enable
2:0	Reserved

Port 601Eh :

Bit	Function Description
	Flash memory control register Default reset value : 08Ah
7	R/W: Flash memory deep power down control 0 0 : Enable Power Down pin PWD0# active or FA23=1 for 16Mbit Random access flash memory 1 : Disable
6	R : Ready / Busy status 0 : BUSY 1 : READY
5:4	R/W: Flash memory type select 00 : 4M flash memory /Bank 0 select for sequential select 01 : 16M flash memory /Bank 1 select for sequential select 10 : Reserved 11 : Reserved

Bit	Function Description
3	R/W: Flash memory deep power down control 1 0 : Enable Power Down pin PWD1# active or FA23=0 for 16Mbit Random access flash memory 1 : Disable
2	R/W: CE# enable for sequential mode 0 : Disable 1 : Enable
1	R/W: Sequential mode select 0 : Random mode 1 : Sequential mode
0	R/W: Flash memory write pulse width control 0 : 1 system clock 1 : 2 system clock

Port 601Fh :

Bit	Function Description
	Default reset value : 0000h R/W : Flash memory Write address FA[24:15] latch for random mode When data space 8000h ~ ffffh is write or program space 8000h ~ ffffh is read, the output of the flash memory write address latch will be used. For sequential mode this register is reserved.

ELECTRICAL SPECIFICATIONS

DC Characteristics 1 : Ta = 0°C to 70 °C, VCC = 5V±10%

Symbol	Parameter	Min	Max	Units	Conditions
VCC	Power Supply voltage	4.5	5.5	V	
VIL1	Input Low voltage (TTL)		0.8	V	VCC=5V
VIH1	Input High voltage (TTL)	2.0		V	VCC=5V
VIL2	Input Low voltage (CMOS)		0.8	V	VCC=5V
VIH2	Input High voltage (CMOS)	3.5		V	VCC=5V
VOL	Output Low voltage		0.4	V	IOL=8mA
VOH	Output High voltage	2.4		V	IOH=-8mA
ICC1	Supply Current 1		40	mA	f = 25Mhz, Active mode, CL = 0pf, VCC=5.5Volt, Temperature= 0°C
ICC2	Supply Current 2		35	mA	f = 25Mhz, Idle mode, CL = 0pf, VCC=5.5Volt, Temperature= 0°C
ICC3	Supply Currect 3		10	mA	f = 25Mhz, Standby mode, CL = 0pf, VCC=5.5Volt, Temperature= 0°C
ICC4	Supply Current 4		1	mA	f = 0Mhz, Sleep mode, CL = 0pf, VCC=5.5Volt, Temperature= 0°C
IL	Input Leakage		±10	uA	0< VIN < VCC
CIN	Input Capacitance		14	pf	VIN=0V
COUT	Output Capacitance		16	pf	VOUT=0V

Note : During transitions, inputs may undershoot to -2.0V for periods less than 20ns and overshoot to VCC + 2.0V for periods less than 20ns.

DC Characteristics 2 : Ta = 0 °C to 70 °C, VCC = 3.3V±5%

Symbol	Parameter	Min	Max	Units	Conditions
VCC	Power Supply voltage	3.1	3.5	V	
VIL1	Input Low voltage(TTL)		0.8	V	VCC=3.3V
VIH1	Input High voltage(TTL)	2.0		V	VCC=3.3V
VIL2	Input Low voltage(CMOS)		0.8	V	VCC=3.3V
VIH2	Input High voltage(CMOS)	2.7		V	VCC=3.3V
VOL	Output Low voltage		0.4	V	IOL=4mA
VOH	Output High voltage	2.2		V	IOH=-4mA
ICC1	Supply Current 1		20	mA	f = 16Mhz, Active mode, CL = 0pf, VCC=3.5Volt,Temperature= 0°C
ICC2	Supply Current 2		15	mA	f = 16Mhz, Idle mode, CL = 0pf, VCC=3.5Volt,Temperature= 0°C
ICC3	Supply Currect 3		5	mA	f = 16Mhz, Standby mode, CL = 0pf, VCC=3.5Volt,Temperature= 0°C
ICC4	Supply Current 4		0.5	mA	f = 0Mhz, Sleep mode, CL = 0pf, VCC=3.5Volt,Temperature= 0°C
IL	Input Leakage		±10	uA	0< VIN < VCC
CIN	Input Capacitance		14	pf	VIN=0V
COUT	Output Capacitance		16	pf	VOUT=0V

Note : During transitions, inputs may undershoot to -2.0V for periods less than 20ns and overshoot to VCC + 2.0V for periods less than 20ns.

AC Characteristics (Condition : Ta=0 °C to 70 °C, VCC = 5V±10% or VCC = 3.3V±5%)

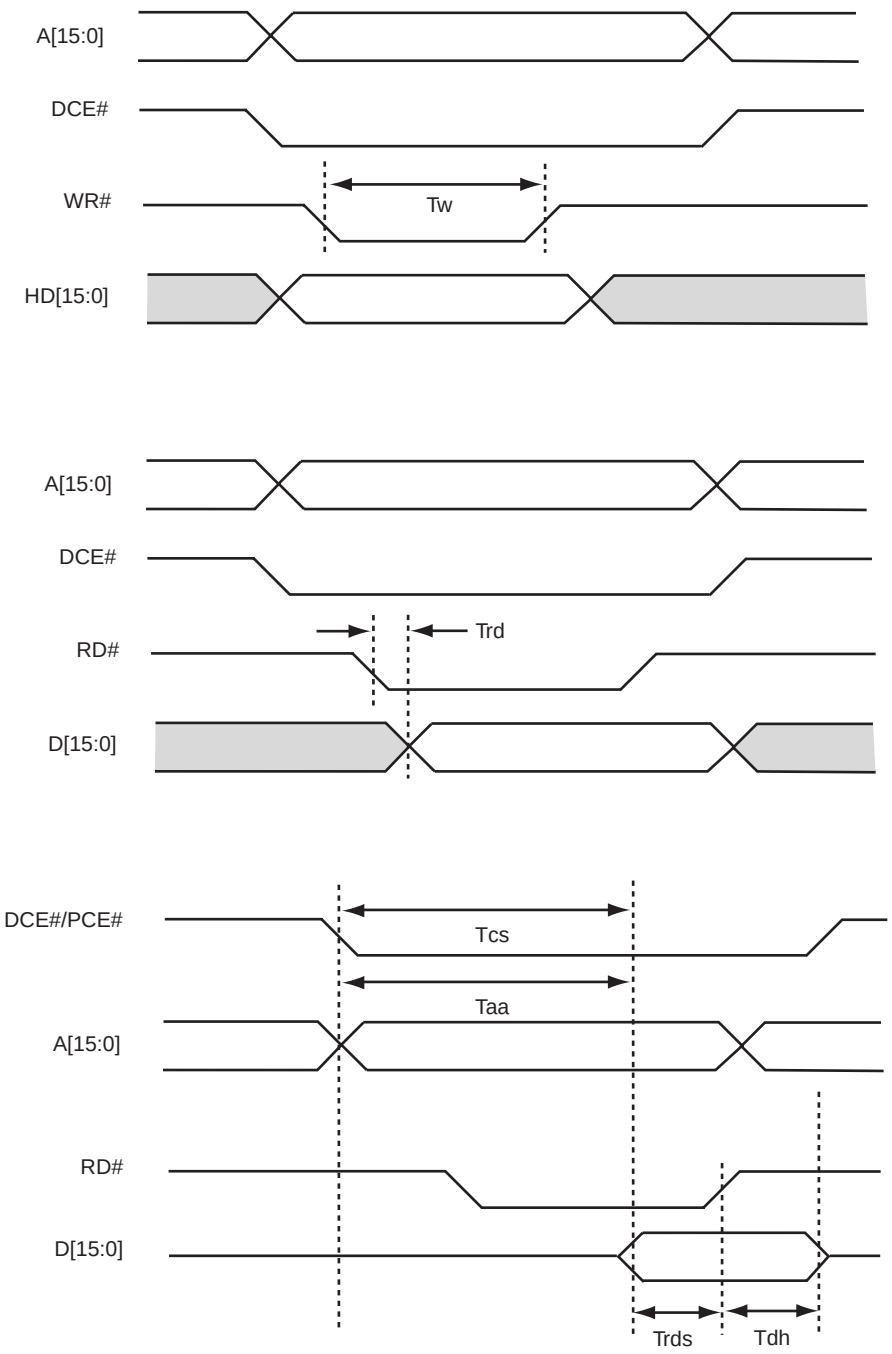
DSP Interface Timing

VCC = 5V±10%

Symbol	Description	Min.	Typ.	Max.	Unit
Tw	In ICE mode, WR# pulse duration when the data are accessed by external DSP.	4Tc			
Trd	In ICE mode, RD# to output delay when the data are accessed by external DSP.			34	ns
Tcs	Chip select access cycle	1.5Tc		4.5Tc	ns
Taa	Address access cycle	1.5Tc		4.5Tc	ns
Trds	Data setup time before RD# high	12			ns
Tdh	Data hold time after RD# high	0			ns

VCC = 3.3V±5%

Symbol	Description	Min.	Typ.	Max.	Unit
Tw	In ICE mode, WR# pulse duration when the data are accessed by external DSP.	4Tc			
Trd	In ICE mode, RD# to output delay when the data are accessed by external DSP.			34	ns
Tcs	Chip select access cycle	1.5Tc		4.5Tc	ns
Taa	Address access cycle	1.5Tc		4.5Tc	ns
Trds	Data setup time before RD# high	15			ns
Tdh	Data hold time after RD# high	0			ns


A[15:0]
DCE#
WR#
Tw
HD[15:0]
A[15:0]
DCE#
RD#
Trd
D[15:0]
DCE#/PCE#
Tcs
Taa
A[15:0]
RD#
D[15:0]
Trds
Tdh

Power Reset Timing

VCC = 5V±10% or VCC = 3.3V±5%

Symbol	Description	Min.	Typ.	Max.	Unit
Tw(rst)	Reset low pulse width	3Tc			ns

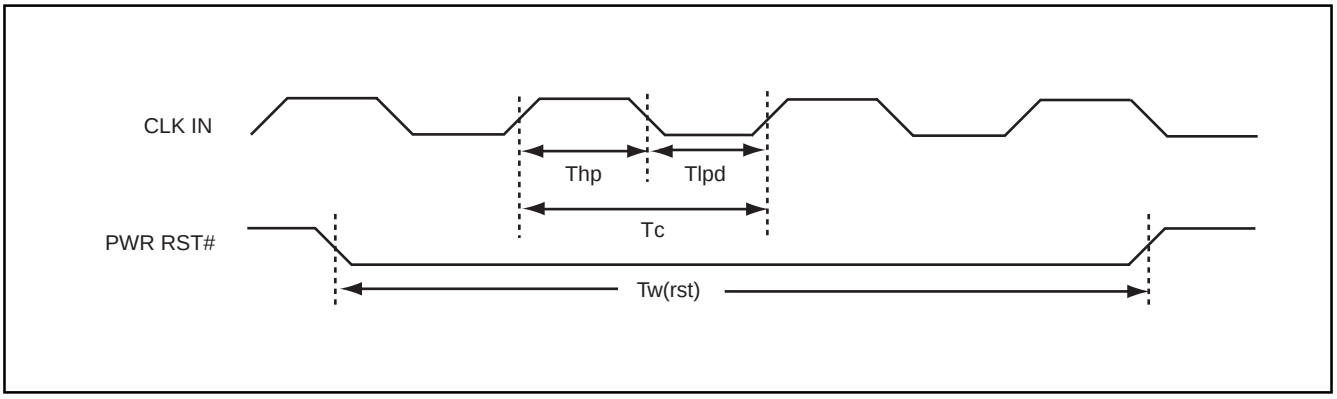
Clock Timing

VCC = 5V±10%

Symbol	Description	Min.	Typ.	Max.	Unit
Tc(c)	Clock cycle time	40			ns
Tlpd(c)	Clock low pulse duration(Tc=40ns)	16		24	ns
Thpd(c)	Clock high pulse duration(Tc=40ns)	16		24	ns

VCC = 3.3V±5%

Symbol	Description	Min.	Typ.	Max.	Unit
Tc(c)	Clock cycle time	62.5			ns
Tlpd(c)	Clock low pulse duration(Tc=62.5ns)	25		37.5	ns
Thpd(c)	Clock high pulse duration(Tc=62.5ns)	25		37.5	ns



Interrupt Timing

VCC = 5V±10%

Symbol	Description	Min.	Typ.	Max.	Unit
Tw	INT1# low pulse duration	1.5Tc			ns
Tf	INT1# fall time			10	ns

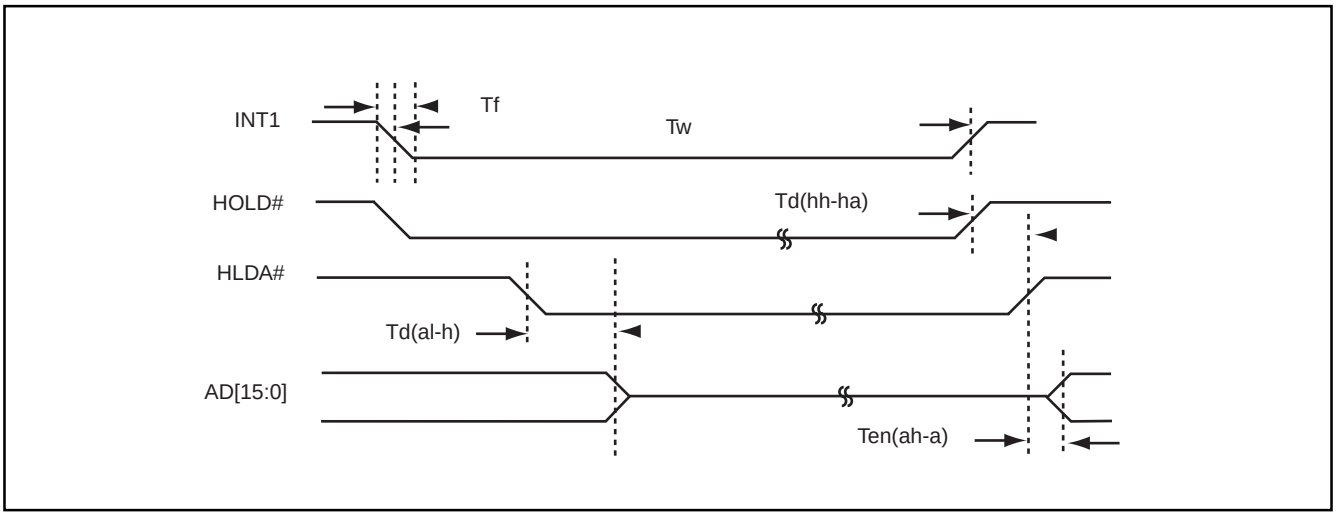
VCC = 3.3V±5%

Symbol	Description	Min.	Typ.	Max.	Unit
Tw	INT1# low pulse duration	1.5Tc			ns
Tf	INT1# fall time				ns

HOLD# Timing

VCC = 5V±10% or VCC = 3.3V±5%

Symbol	Description	Min.	Typ.	Max.	Unit
Td(al-h)	HLDA# low to address tri-state	0			ns
Td(hh-ha)	HOLD# high to HLDA# high	0	0.5Tc	0.5Tc+10	ns
Ten(ah-a)	Address driven after HLDA# high	0.5Tc -10	0.5Tc	Tc	ns



PCMCIA Bus Timing 1: Common Memory and Attribute memory Access Timing

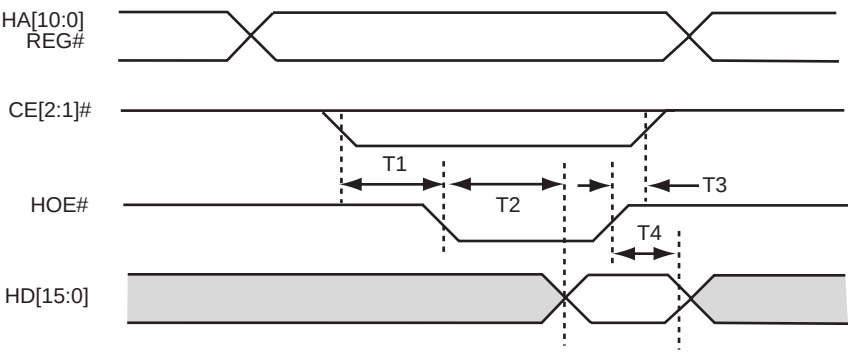
VCC = 5V±10%

Symbol	Parameter	Min (ns)	Max (ns)
T1	Chip enable setup time before output enable	0	
T2	Output data enable time from HOE#		31
T3	Chip disable hold time following output disable	1.5	
T4	Output data disable time following HOE#		10.5
T5	Chip enable setup time before HWE#	0	
T6	Chip disable hold time following write disable	2	
T7	Data setup time before HWE#	0	
T8	Data hold time following HWE#	2.5	

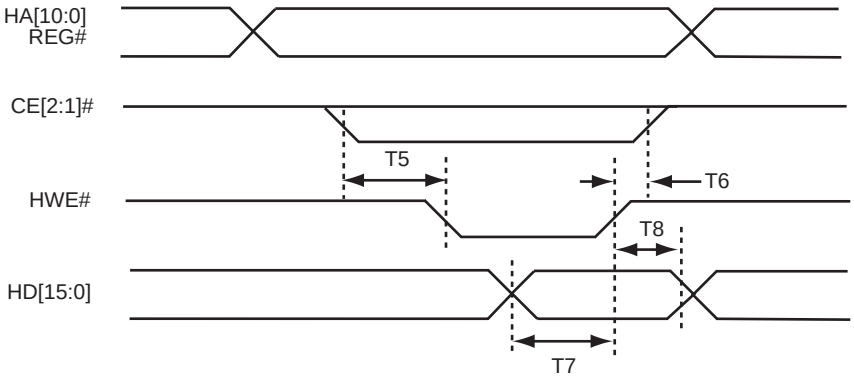
VCC = 3.3V±5%

Symbol	Parameter	Min (ns)	Max (ns)
T1	Chip enable setup time before output enable	0	
T2	Output data enable time from HOE#		47
T3	Chip disable hold time following output disable	3	
T4	Output data disable time following HOE#		17
T5	Chip enable setup time before HWE#	0	
T6	Chip disable hold time following write disable	2.5	
T7	Data setup time before HWE#	0	
T8	Data hold time following HWE#	3	

Common Memory and Attribute Memory Read Timing



Common Memory and Attribute Memory WriteTiming



PCMCIA Bus Timing 2: I/O mode Access Timing

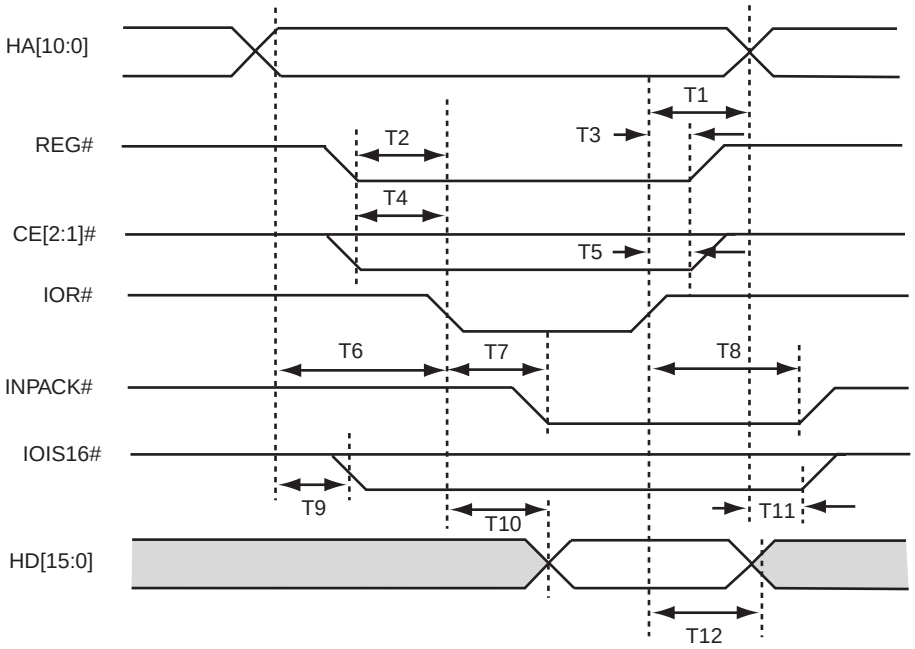
VCC = 5V±10%

Symbol	Parameter	Min (ns)	Max (ns)
T1	Address hold time following IOR#	2	
T2	REG# setup time before IOR#	0	
T3	REG# hold time following IOR#	0	
T4	CE# setup time before IOR#	0	
T5	CE# hold time following IOR#	2	
T6	Address setup time before IOR#	0	
T7	INPACK delay from IOR# falling		10
T8	INPACK delay from IOR# rising		10.5
T9	IOIS16 falling delay after Address changed		14
T10	Data delay after IOR# falling		32
T11	IOIS16 rising delay after Address changed		12.5
T12	Data hold time following IOR#		20
T13	Address hold time following IOW#	3	
T14	REG# setup time before IOW#	0	
T15	REG# hold time following IOW#	0	
T16	CE# setup time before IOW#	0	
T17	CE# hold time following IOW#	2	
T18	Address setup time before IOW#	0	
T19	IOIS16 rising delay after Address changed		10.5
T20	IOIS16 falling delay after Address changed		14
T21	Data setup time before IOW#	0	
T22	Data hold time following IOW#	2.5	

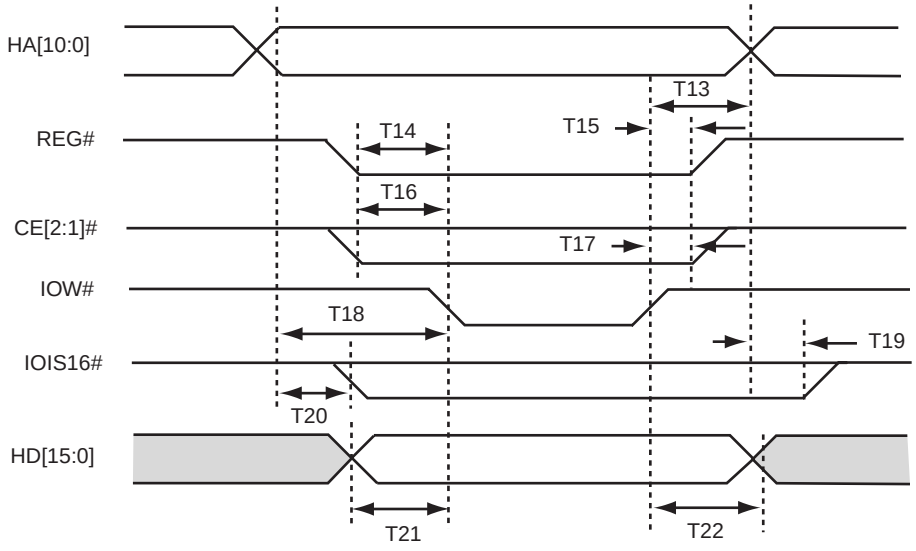
VCC = 3.3V±5%

Symbol	Parameter	Min (ns)	Max (ns)
T1	Address hold time following IOR#	2	
T2	REG# setup time before IOR#	0	
T3	REG# hold time following IOR#	0	
T4	CE# setup time before IOR#	0	
T5	CE# hold time following IOR#	2	
T6	Address setup time before IOR#	0	
T7	INPACK delay from IOR# falling		18
T8	INPACK delay from IOR# rising		18
T9	IOIS16 falling delay after Address changed		23.5
T10	Data delay after IOR# falling		47
T11	IOIS16 rising delay after Address changed		20
T12	Data hold time following IOR#	31	
T13	Address hold time following IOW#	4	
T14	REG# setup time before IOW#	0	
T15	REG# hold time following IOW#	0	
T16	CE# setup time before IOW#	0	
T17	CE# hold time following IOW#	2.5	
T18	Address setup time before IOW#	0	
T19	IOIS16 rising delay after Address changed		20
T20	IOIS16 falling delay after Address changed		23.5
T21	Data setup time before IOW#	0	
T22	Data hold time following IOW#	3	

ID Read Timing



I/O Write Timing



Flash Memory Interface Timing

VCC = 5V±10%

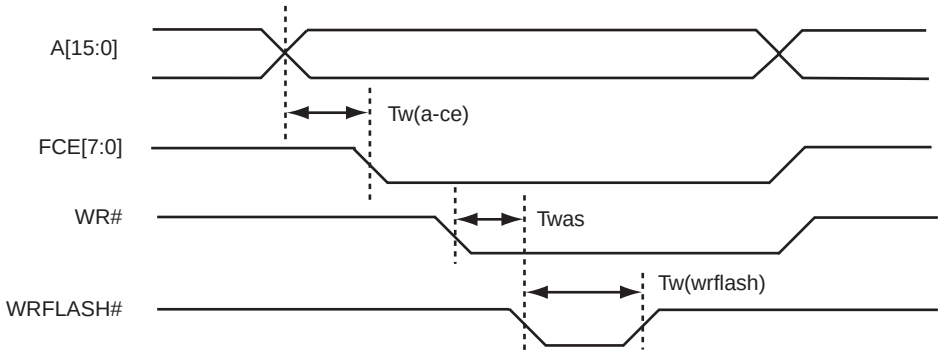
Symbol	Parameter	Min.	Max.	Unit
Tw(a-ce)	FCE# fall time after DSP address decode when write	5.5	15	ns
Twas	FCE# setup time before WRFLASH# falling edge	10	30	ns
Tw(wrflash)	WRFLASH# low pulse duration	1Tc*		ns
Tr(a-ce)	FCE# fall time after DSP address decode when read	5.5	15	ns
Tr(rd-0e)	RDFLASH# fall time after RD# falling edge	4.5	11.5	ns

VCC = 3.3V±5%

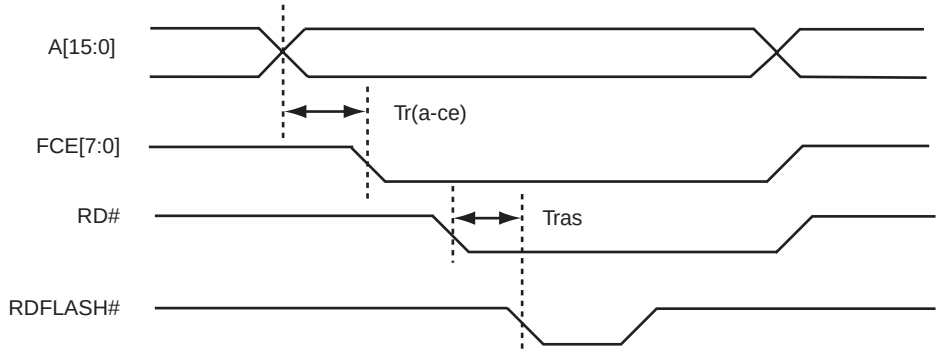
Symbol	Parameter	Min.	Max.	Unit
Tw(a-ce)	FCE# fall time after DSP address decode when write	8	24.5	ns
Twas	FCE# setup time before WRFLASH# falling edge	15	50	ns
Tw(wrflash)	WRFLASH# low pulse duration	1Tc*		ns
Tr(a-ce)	FCE# fall time after DSP address decode when read	8	25	ns
Tr(rd-0e)	RDFLASH# fall time after RD# falling edge	7	20	ns

* Note:These timing are only for 1-system clock of flash memory write pulse is employed (601E[0]=0). If 2-system clock of pulse width is selected (601E[0]=1), the minimum of Tw(wrflash) is 2Tc.

Flash memory write timing



Flash memory Read timing



Latchup Characteristics

	Min.	Max.
Input Voltage with respect to GND on all VCC pins	-2.0V	12.0V
Input Voltage with respect to GND on all I/O pins	-2.0V	VCC+2.0V
Current	-100mA	+100mA
Includes all pins except GND. Test conditions : VCC=5.0V, one pin at a time.		

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