

### Applications

- SONET/SDH-based transmission systems, test equipment and modules
- OC-48 fibre optic modules
- Gigabit Ethernet
- Fibre Channel
- Wideband RF gain block

### Features

- Single +3.3 V supply
- Power dissipation = 230 mW (typ)
- Noise figure < 12 dB
- Small signal gain = 23.5 dB differential
- Fully integrated AGC function
- On-chip 50 Ω input and output terminations
- Wide bandwidth (–3 dB) > 2.0 GHz
- Maximum input level of 200 mVpk
- AGC output level of 370 mVpk differential
- Loss of signal functionality
- Single-ended or differential operation
- Minimal external components
- Operating ambient temperature range = -40°C to +85°C
- Equivalent to Nortel Networks AC10

### Product Description

SiGe Semiconductor offers a portfolio of optical networking ICs for use in high-performance optical transmitter and receiver functions, from 155 Mb/s up to 12.5 Gb/s.

SiGe Semiconductor's SE1230 is a fully integrated AGC amplifier aimed primarily at SONET OC-48 and SDH STM-16 systems. The device may also be used in any datacom application with input data rates up to 2.5 Gb/s.

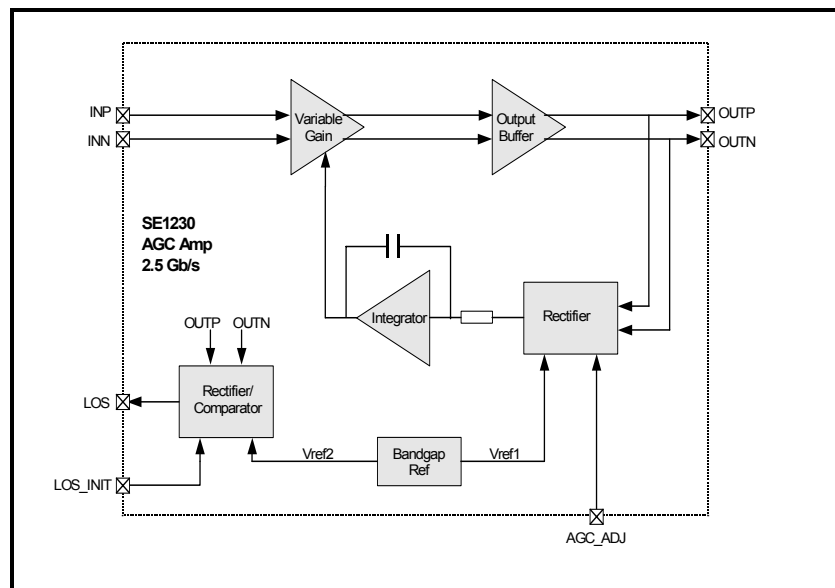
The device is designed with differential I/Os and signal levels compatible with SiGe Semiconductor's SE1030 and SE1031 transimpedance amplifiers. A system block diagram is shown after the functional description, on page 4.

Optimum performance is provided by differential connections but with appropriate terminations, the device can also be used in single-ended mode if required by the application.

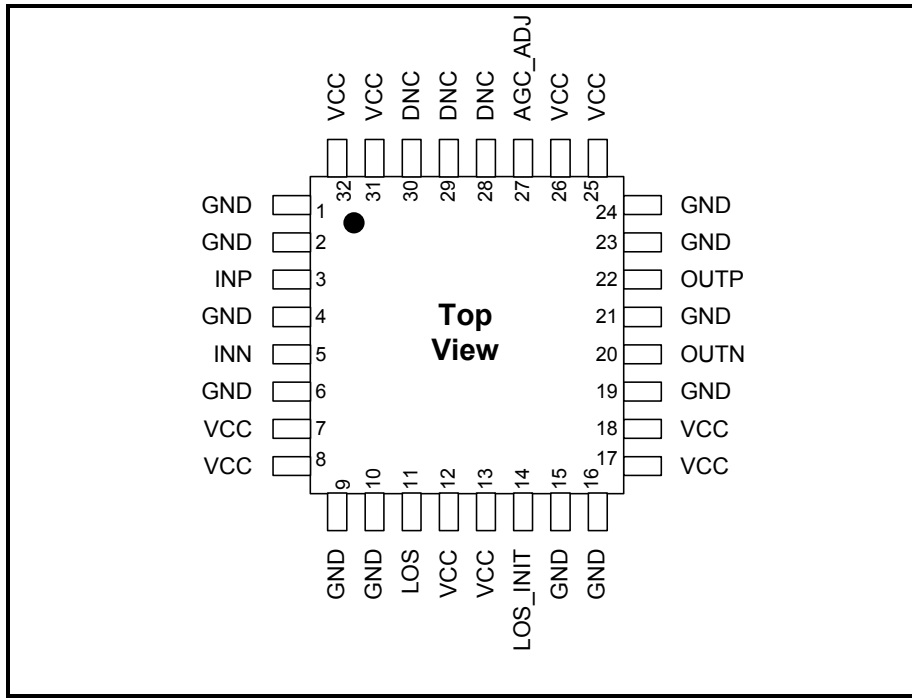
### Ordering Information

Type	Package	Remark
SE1230Q	5 mm, 32 pin LQFP	None

### Functional Block Diagram



**Pin Out Diagram**



**Pin Out Description**

Pin No.	Name	Description
1	GND	Negative supply (0 V)
2	GND	Negative supply (0 V)
3	INP	Non-inverting input (50 $\Omega$ impedance)
4	GND	Negative supply (0 V)
5	INN	Inverting input (50 $\Omega$ impedance)
6	GND	Negative supply (0 V)
7	VCC	Positive supply (3.3 V)
8	VCC	Positive supply (3.3 V)
9	GND	Negative supply (0 V)
10	GND	Negative supply (0 V)
11	LOS	Loss of signal output (open collector)
12	VCC	Positive supply (3.3 V)
13	VCC	Positive supply (3.3 V)
14	LOS_INIT	Sets initial state of LOS output

15	GND	Negative supply (0 V)
16	GND	Negative supply (0 V)
17	VCC	Positive supply (3.3 V)
18	VCC	Positive supply (3.3 V)
19	GND	Negative supply (0 V)
20	OUTN	Inverted output (50 $\Omega$ impedance)
21	GND	Negative supply (0 V)
22	OUTP	Non-inverted output (50 $\Omega$ impedance)
23	GND	Negative supply (0 V)
24	GND	Negative supply (0 V)
25	VCC	Positive supply (3.3 V)
26	VCC	Positive supply (3.3 V)
27	AGC_ADJ	AGC output level adjust
28	DNC	Do not connect
29	DNC	Do not connect
30	DNC	Do not connect
31	VCC	Positive supply (3.3 V)
32	VCC	Positive supply (3.3 V)

## Functional Description

The SE1230 is configured as a variable gain amplifier, with automatic gain control. It comprises a variable-gain block driving a 50 Ω output driver (see the functional block diagram on page 1). The device requires a single +3.3 V power supply.

## System Inputs

The inputs INP and INN are differential and are each internally terminated to 50 Ω. To avoid problems with offset or common-mode voltage, use AC-coupling for differential or single-ended connection (for the latter, AC-couple the unused input to ground via 50 Ω). The maximum input level is 200 mVpk, applied single-ended or differentially.

## System Outputs

The outputs OUTP and OUTN are differential and are each internally terminated to 50 Ω. To avoid problems with offset or common-mode voltage, use AC-coupling for differential or single-ended connection (for the latter, AC-couple the unused output to ground via 50 Ω). The default output level (under AGC) is 370 mVpk differential.

## Automatic Gain Control (AGC)

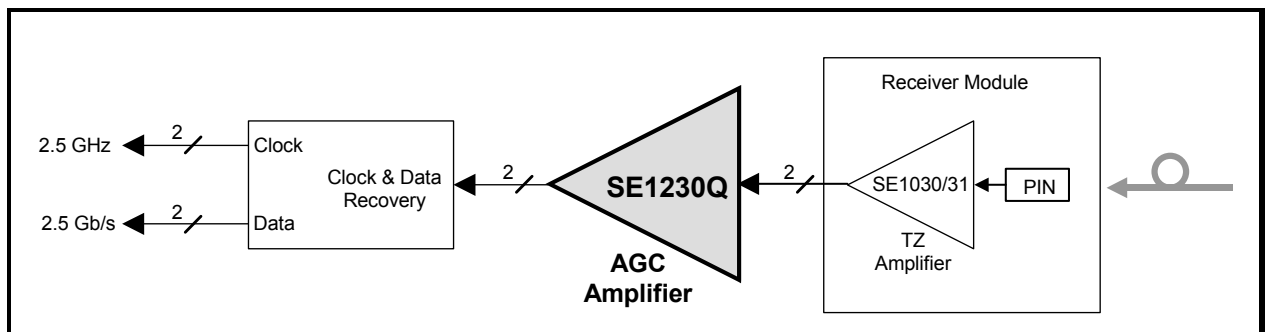
A rectifier compares the output signal voltage with a reference level to invoke gain control. When operating in the controlled gain region, the fully integrated long time-constant integrator provides filtered control voltages to the variable gain stages to maintain a fixed output level. This output level may be varied by injecting current into AGC\_ADJ (leave unconnected if adjustment is not required).

## Loss of Signal

A two-level comparator block is used to detect the input signal level. If it drops below the lower threshold, LOS goes low. This output is an open collector to allow wired-OR connection to other system alarm signals; it requires an external pull-up resistor. It goes high only when the input level exceeds the upper comparator threshold level. If this function is not required, LOS may be left unconnected.

By connecting an external series-RC to the LOS\_INIT pin, LOS can be forced low on first power up if the signal level is between the upper and lower comparator thresholds. If this function is not required, leave LOS\_INIT unconnected.

## System Block Diagram



### Absolute Maximum Ratings

These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of the device. Avoid operating the device outside the recommended operating conditions defined below.

Symbol	Parameter	Min	Max	Unit
VCC	Supply Voltage	-0.5	5.0	V
V <sub>IO</sub>	Voltage at any input or output	-0.5	VCC+0.5	V
I <sub>IO</sub>	Current sourced into any input or output, except OUTP and OUTN	-20	20	mA
I <sub>IO</sub>	Current sourced into pins OUTP and OUTN	-40	40	mA
V <sub>ESD</sub>	Electrostatic Discharge (100 pF, 1.5 kΩ), all pins	-2	2	kV
T <sub>stg</sub>	Storage Temperature	-65	150	°C

### Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Supply Voltage	3.1	3.3	3.5	V
I <sub>LOS</sub>	LOS Output Load Current			5	mA
R <sub>LOSI</sub>	LOS_INIT Resistor		1		kΩ
C <sub>LOSI</sub>	LOS_INIT Capacitor (increase value for slow power supply rise time)		1		μF
I <sub>AGC_ADJ</sub>	AGC Threshold Adjust Input Current (on AGC_ADJ pin) – note 1	0		150	μA
T <sub>a</sub>	Operating Ambient Temperature	-40		85	°C

Note 1: This current can be produced by connecting a suitable resistor between VCC and AGC\_ADJ.

### DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
I <sub>CC</sub>	Supply current		70	100	mA
P <sub>D</sub>	Power Dissipation		230	350	mW
V <sub>AGC_ADJ</sub>	Open-circuit AGC_ADJ Voltage		0.37		V
V <sub>LOS</sub>	Output Low Voltage on LOS, with I <sub>LOS</sub> = 1 mA			0.4	V
R <sub>T</sub>	Input/Output Termination Resistance		50		Ω

### AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
BW (3dB)	Small Signal Bandwidth at -3dB point	2.0			GHz
Gain	Small Signal Gain (f = 100 MHz), differential input / output	21	23.5	26	dB
$V_{in}$	Maximum Input Signal Level			200	mV pk (differential)
	Input Signal Level at AGC Threshold ( $I_{AGC\_ADJ} = 0 \mu A$ ) – note 2		25		
	Lower LOS Threshold (LOS = low)	5	8		
	Upper LOS Threshold (LOS = high)		12	18	
$V_{out}$	Output AGC Signal Level ( $I_{AGC\_ADJ} = 0 \mu A$ ) – note 3	250	370	500	mV pk (differential)
	Output AGC Signal Level ( $I_{AGC\_ADJ} = 150 \mu A$ ) – note 3	80	170	300	
$S_{11}$	Input Reflection Coefficient (< 1.3 GHz)			-10	dB
$S_{22}$	Output Reflection Coefficient (< 1.3 GHz)			-10	dB
NF	Noise Figure (diff. in / diff. out)			12	dB
$t_R / t_F$	Output Rise / Fall Time (Input rise / fall time = 20 ps)		120		ps

Note 2:  $V_{in}$  at AGC threshold is calculated by dividing  $V_{out}$  by the small signal gain.

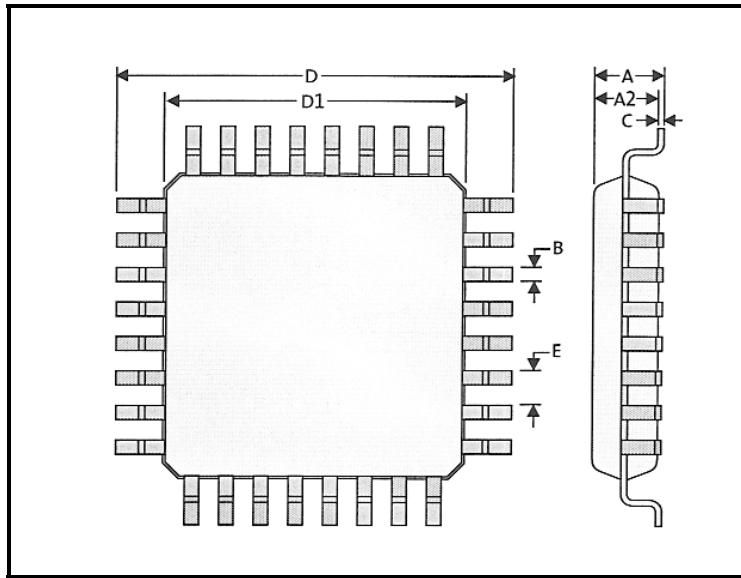
Note 3: Measured at  $V_{in} = 100$  mV pk,  $f = 100$  MHz. For intermediate values of  $I_{AGC\_ADJ}$  the output amplitude can be estimated by linear interpolation.

DC and AC electrical characteristics are specified over the recommended operating conditions, and with load resistor ( $R_L$ ) of 50  $\Omega$ , AC coupled via 100 nF, for each output. All characteristics are specified for differential signals on inputs and outputs.

## Package Information

The device is packaged in a 5 mm, 32 pin plastic low profile quad flat pack (LQFP).

### Package Outline

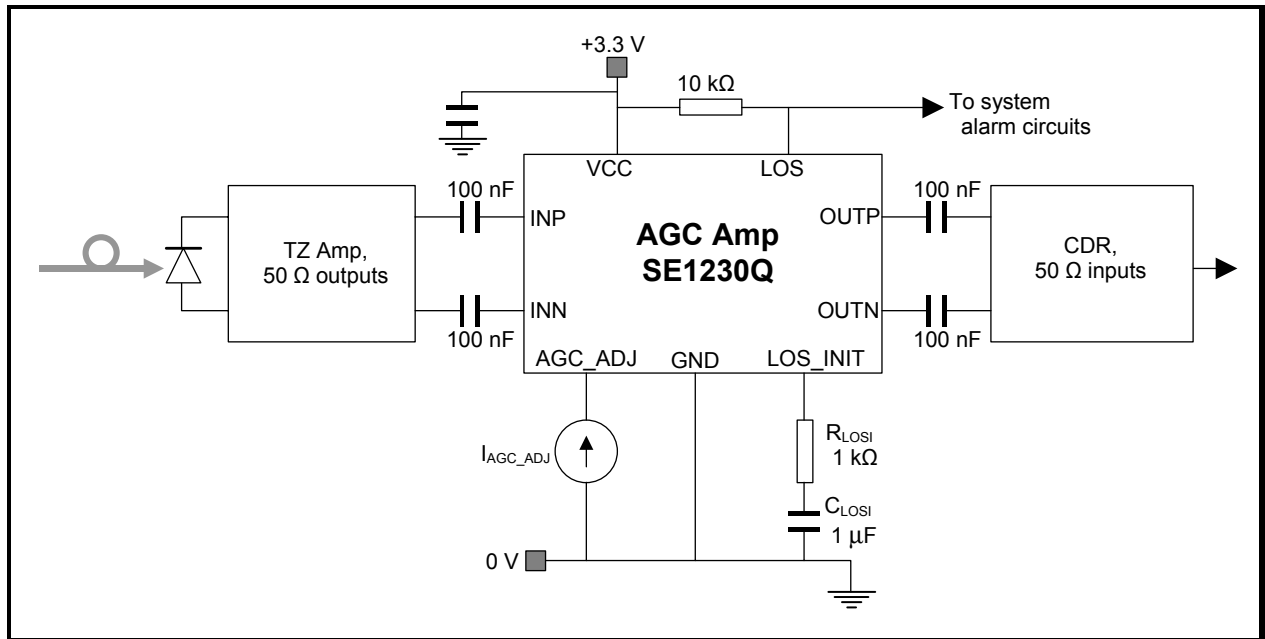


### Package Dimensions

Dimension	Min (mm)	Nom (mm)	Max (mm)
Lead Count		32	
Lead Pitch (E)		0.5	
Body Size (D1)		5.00	
Component Tip-to-Tip (D)		7.00	
Component Height (A)			1.60
Component Standoff	0.05		0.15
Body Thickness (A2)	1.35	1.40	1.45
Lead width (plated) (B)	0.17	0.22	0.27
Lead Thickness (plated) (C)	0.09		0.175

## Applications Information

For optimum performance it is recommended that the device be used in differential mode with the circuit shown in the diagram below. Components connected to LOS, LOS\_INIT and AGC\_ADJ are optional, depending on whether or not the loss of signal and/or AGC adjust functions are required.





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<http://www.sige.com>

**Headquarters: Canada**

Phone: +1 613 820 9244

Fax: +1 613 820 4933

2680 Queensview Drive

Ottawa ON K2B 8J9 Canada

[sales@sige.com](mailto:sales@sige.com)

**San Diego**

Phone: +1 858 668 3541

Fax: +1 858 668 3546

**Hong Kong**

Phone: +1 852 9177 1917

**United Kingdom**

South Building, Walden Court  
Parsonage Lane, Bishop's Stortford  
Hertfordshire CM23 5DB

Phone: +44 1279 464 200

Fax: +44 1279 464 201

Product Preview

The datasheet contains information from the product concept specification. SiGe Semiconductor Inc. reserves the right to change information at any time without notification.

Preliminary Information

The datasheet contains information from the design target specification. SiGe Semiconductor Inc. reserves the right to change information at any time without notification.

Final

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