3-W High-Voltage Switchmode Regulator

FEATURES

- 10- to 120-V Input Range
- Current-Mode Control
- On-chip 200-V, 7-Ω MOSFET Switch
- $\overline{\text{SHUTDOWN}}$ and RESET
- High Efficiency Operation (> 80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)

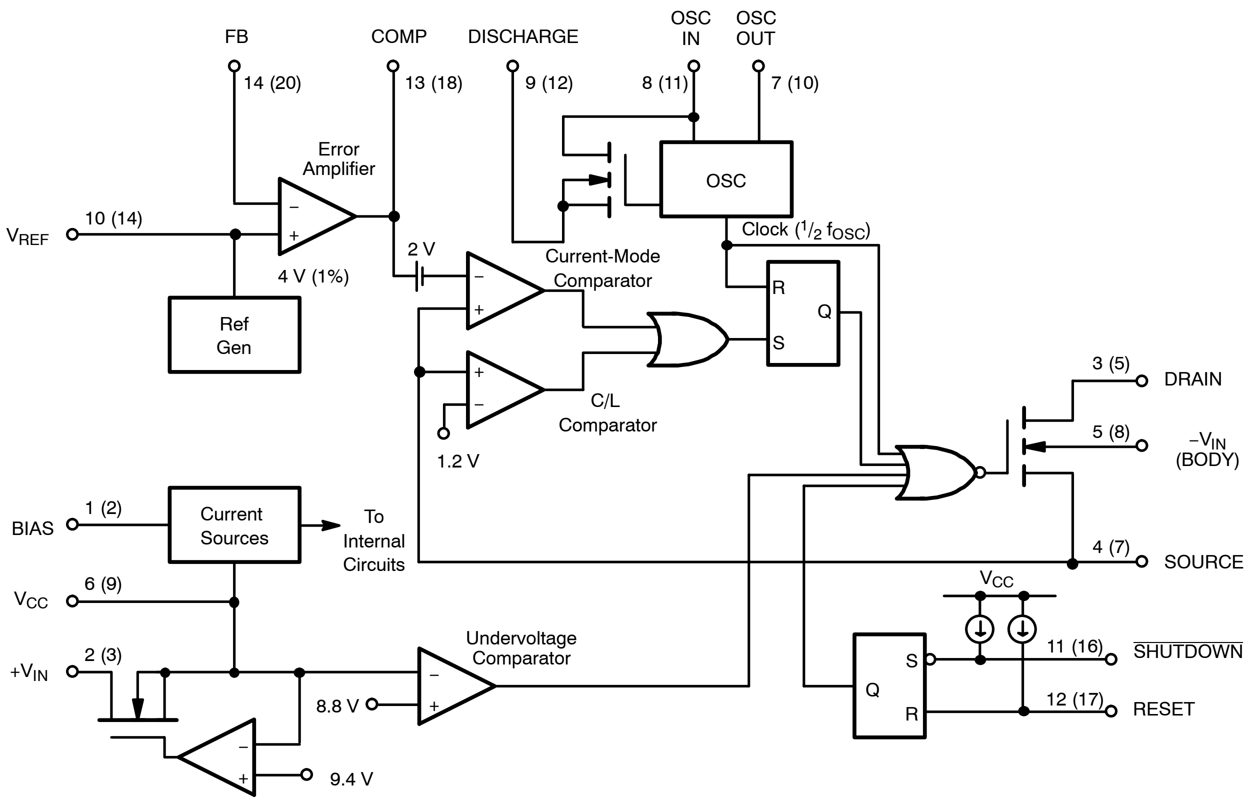
DESCRIPTION

The Si9102 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc-to-dc converter up to 3 watts. It can either be operated from a low-voltage dc supply, or directly from a 10- to 120-V unregulated dc power source.

This device may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward).

The Si9102 is available in both standard and lead (Pb)-free 14-pin plastic DIP and 20-pin PLCC packages which are specified to operate over the industrial temperature range of −40°C to 85°C.

FUNCTIONAL BLOCK DIAGRAM



Note: Figures in parenthesis represent pin numbers for 20-pin package.

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} . . . 15 V
$+V_{IN}$ . . . 120 V
V_{DS} . . . 200 V
I_D (Peak) (Note: 300 µs pulse, 2% duty cycle) . . . 2 A
I_D (rms) . . . 250 mA
Logic Inputs (RESET, $\overline{SHUTDOWN}$, OSC IN) . . . –0.3 V to V_{CC} + 0.3 V
Linear Inputs (FEEDBACK, SOURCE) . . . –0.3 V to 7 V
HV Pre-Regulator Input Current (continuous) . . . 3 mA
Storage Temperature . . . –65 to 125°C
Operating Temperature . . . –40 to 85°C

Junction Temperature (T_J) . . . 150°C
Power Dissipation (Package)a
14-Pin Plastic DIP (J Suffix)[b] . . . 750 mW
20-Pin PLCC (N Suffix)[c] . . . 1400 mW
Thermal Impedance (Θ_{JA})
14-Pin Plastic DIP . . . 167°C/W
20-Pin PLCC . . . 90°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25°C
c. Derate 11.2 mW/°C above 25°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$
V_{CC} . . . 9.5 V to 13.5 V
R_{OSC} . . . 25 kΩ to 1 MΩ
Linear Inputs . . . 0 to 7 V
$+V_{IN}$ . . . 10 V to 120 V
f_{OSC} . . . 40 kHz to 1 MHz
Digital Inputs . . . 0 to V_{CC}

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix –40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
Reference							
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) R_L = 10 MΩ	Room Full	3.92 3.86	4.0	4.08 4.14	V
Output Impedance[e]	Z_{OUT}		Room	15	30	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$	Room	70	100	130	µA
Temperature Stability[e]	T_{REF}		Full		0.5	1.0	mV/°C
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 kΩ[g]	Room	80	100	120	kHz
		R_{OSC} = 150 kΩ[g]	Room	160	200	240	
Voltage Stability	Δf/f	Δf/f = f(13.5 V) – f(9.5 V)/f(9.5 V)	Room		10	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	Room	3.96	4.00	4.04	V
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V, OSC IN = $-V_{IN}$ (OSC Disabled)	Room		25	500	nA
Open Loop Voltage Gain[e]	A_{VOL}		Room	60	80		dB
Unity Gain Bandwidth[e]	BW		Room	0.7	1		MHz
Dynamic Output Impedance[e]	Z_{OUT}		Room		1000	2000	Ω
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)	Room		–2.0	–1.4	mA
Input OFFSET Voltage	V_{OS}	OSC IN = $-V_{IN}$ (OSC Disabled)	Room		±15	±40	mV

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Error Amplifier							
Output Current	I_{OUT}	Sink (V_{FB} = 4.5 V)	Room	0.12	0.15		mA
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V	Room	50	70		dB
Current Limit							
Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC} V_{FB} = 0 V	Room	1.0	1.2	1.4	V
Delay to Output[e]	t_d	R_L = 100 Ω from DRAIN to V_{CC} V_{SOURCE} = 1.5 V, See Figure 1	Room		100	200	ns
Pre-Regulator/Start-Up							
Input Voltage	$+V_{IN}$	I_{IN} = 10 μA	Room			120	V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 10 V	Room			10	μA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 μs, V_{CC} = 7 V	Room	8	15		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 μA	Room	7.8	9.4	9.7	
Undervoltage Lockout	V_{UVLO}	R_L = 100 Ω from DRAIN to V_{CC} See Detailed Description	Room	7.0	8.8	9.2	V
V_{REG}, $-V_{UVLO}$	V_{DELTA}		Room	0.3	0.6		
Supply							
Supply Current	I_{CC}		Room	0.45	0.6	1.0	mA
Bias Current	I_{BIAS}		Room	10	15	20	μA
Logic							
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	V_{SOURCE} = $-V_{IN}$, See Figure 2	Room		50	100	
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}		Room	50			
RESET Pulse Width[e]	t_{RW}	See Figure 3	Room	50			ns
Latching Pulse Width[e] $\overline{\text{SHUTDOWN}}$ and RESET Low	t_{LW}		Room	25			
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	8.0			
Input Current Input Voltage High	I_{IH}	V_{IN} = 10 V	Room		1	5	μA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	−35	−25		
MOSFET Switch							
Breakdown Voltage	$V_{BR(DSS)}$	I_{DRAIN} = 100 μA	Full	200	220		V
Drain-Source On Resistance[f]	$r_{DS(on)}$	I_{DRAIN} = 100 mA	Room			7	Ω
Drain Off Leakage Current	I_{DSS}	V_{DRAIN} = 100 V	Room		5	10	μA
Drain Capacitance	C_{DS}		Room		35		pF

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. Temperature coefficient of $r_{DS(on)}$ is 0.75% per °C, typical.
g. C_{STRAY} Pin 8 = ≤ 5 pF

TIMING WAVEFORMS

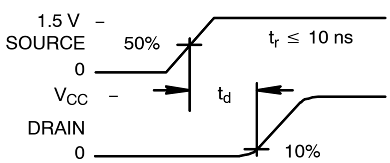


FIGURE 1.

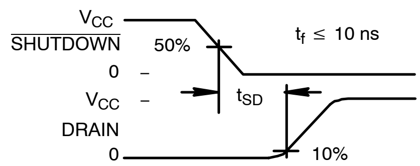


FIGURE 2.

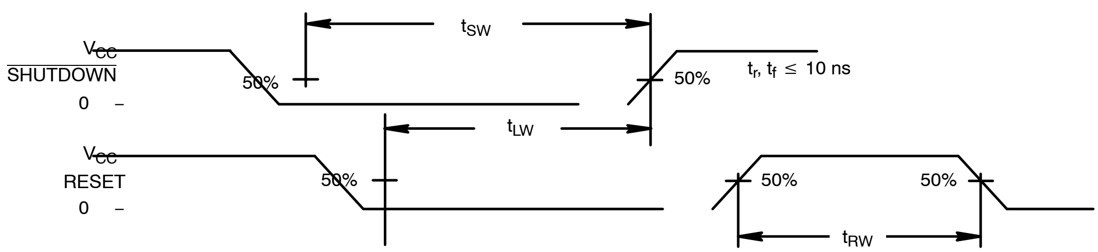


FIGURE 3.

TYPICAL CHARACTERISTICS

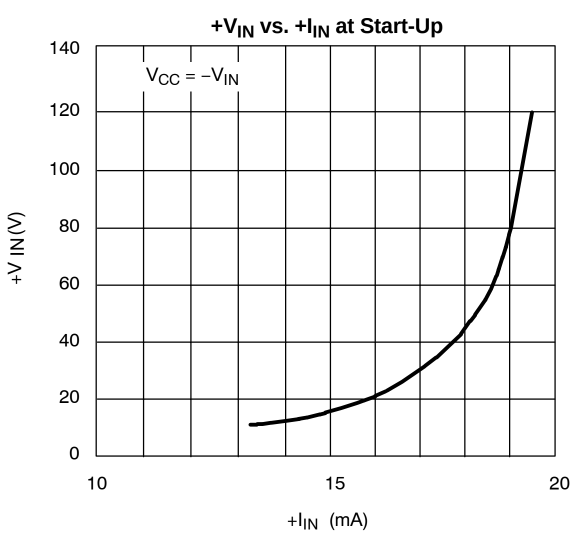


FIGURE 4.

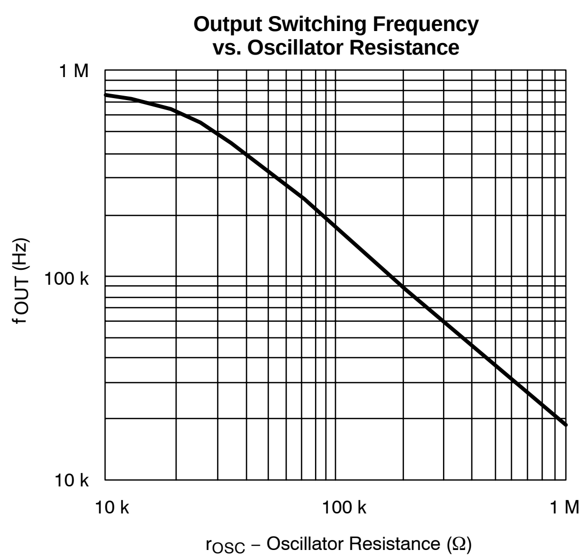
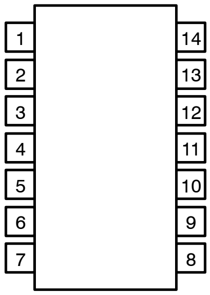


FIGURE 5.

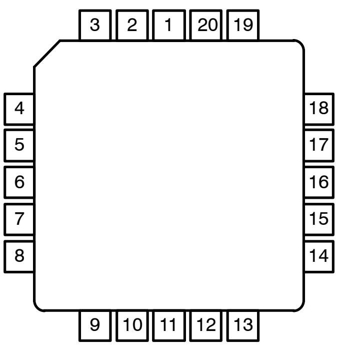
PIN CONFIGURATIONS

PDIP-14



Top View

PLCC-20



Top View

PIN DESCRIPTION

Function	Pin	
	14-Pin DIP	20-Pin PLCC*
BIAS	1	2
$+V_{IN}$	2	3
DRAIN	3	5
SOURCE	4	7
$-V_{IN}$	5	8
V_{CC}	6	9
OSC OUT	7	10
OSC IN	8	11
DISCHARGE	9	12
V_{REF}	10	14
SHUTDOWN	11	16
RESET	12	17
COMP	13	18
FB	14	20

*Pins 1, 4, 6, 13, 15, and 19 = N/C

ORDERING INFORMATION

Standard Part Number	Lead (Pb)-Free Part Number	Temperature Range	Package
Si9102DJ02	Si9102DJ02—E3	–40 to 85 °C	PDIP-14
Si9102DN02	Si9102N02—E3		PLCC-20

DETAILED DESCRIPTION

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9102 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC}. This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 9.4 V. If V_{CC} is not forced to exceed the 9.4-V threshold, then V_{CC} will be regulated to a nominal value of 9.4 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.8-V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will not exceed the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

Note: During start-up or when V_{CC} drops below 9.4-V the start-up circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48-V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. Figure 4 gives the typical pre-regulator current at start-up as a function of input voltage.

BIAS

To properly set the bias for the Si9102, a 390-kΩ resistor should be tied from BIAS to $-V_{IN}$. This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

Reference Section

The reference section of the Si9102 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9102 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ± 1% of 4 V. This automatically compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with “around-the-amplifier” compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC in and OSC out pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤ 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a synchronization pulse into the OSC IN terminal. For a 5-V pulse amplitude and 0.5-μs pulse width, typical values would be 100 pF in series with 3 kΩ to OSC IN.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ and RESET are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Table 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
↑	L	Off (Latched, No Change)

Output Switch

The output switch is a 7-Ω , 200-V lateral DMOS device. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9102 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

APPLICATIONS

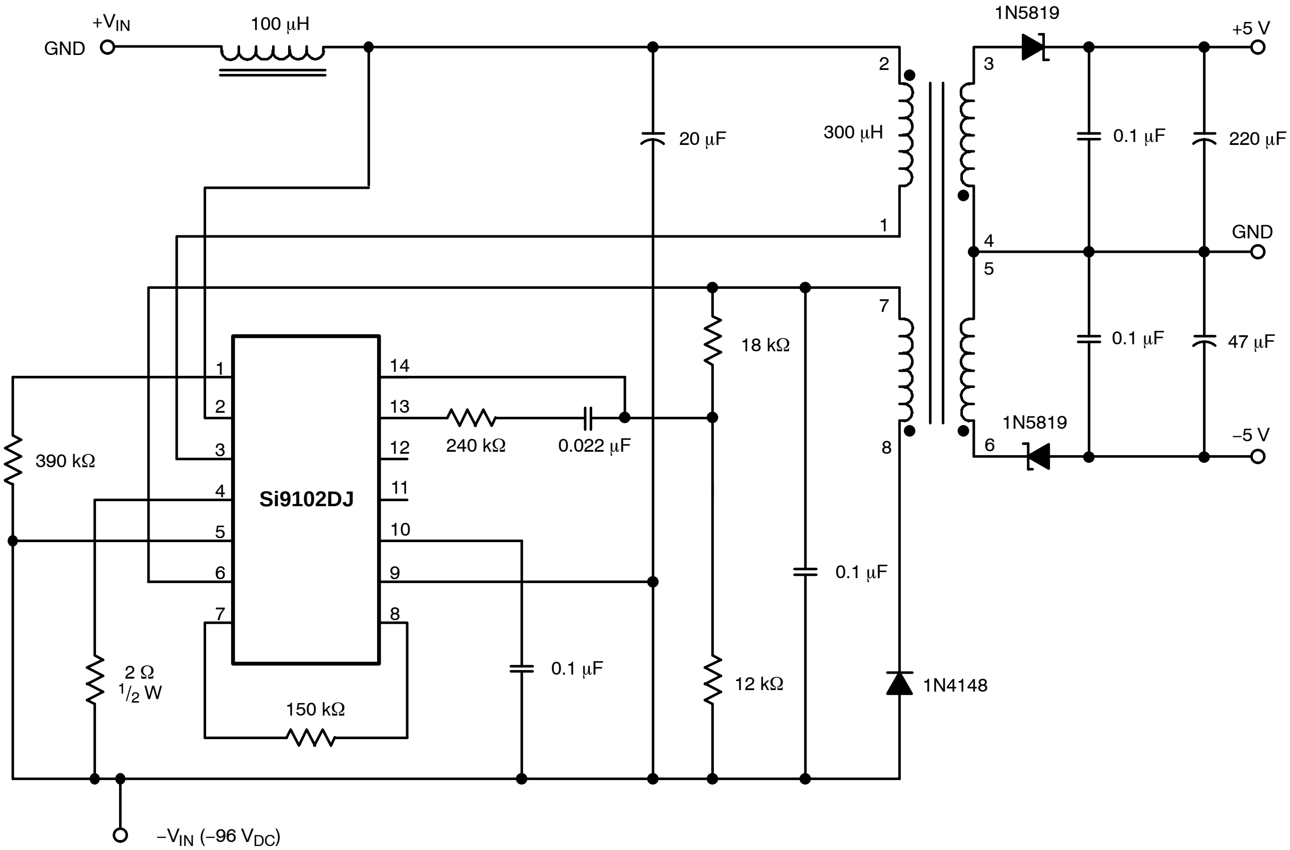


FIGURE 6. Flyback Converter for Double Battery Telecommunications Power Supplies

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?70001.