WM8739 / WM8739L

Stereo Audio ADC

DESCRIPTION

The WM8739 is a stereo audio ADC. The WM8739 is designed specifically for portable MP3 audio and speech players and recorders. The WM8739 is also ideal for MD, CD-RW machines and DAT recorders.

Stereo line-level audio inputs are provided, along with a mute and volume function, and master or slave mode clocking schemes. The device also has a programmable high pass filter to remove residual DC offsets.

Stereo 24-bit multi-bit sigma delta ADCs are used with oversampling digital interpolation and digital filters. Digital audio output word lengths from 16-32 bits and sampling rates from 8KHz to 96KHz are supported.

The device is controlled via a 2 or 3 wire serial interface. The interface provides access to all features including volume controls, mutes, de-emphasis and extensive power management facilities. The device is available in a small 20-pin SSOP package.

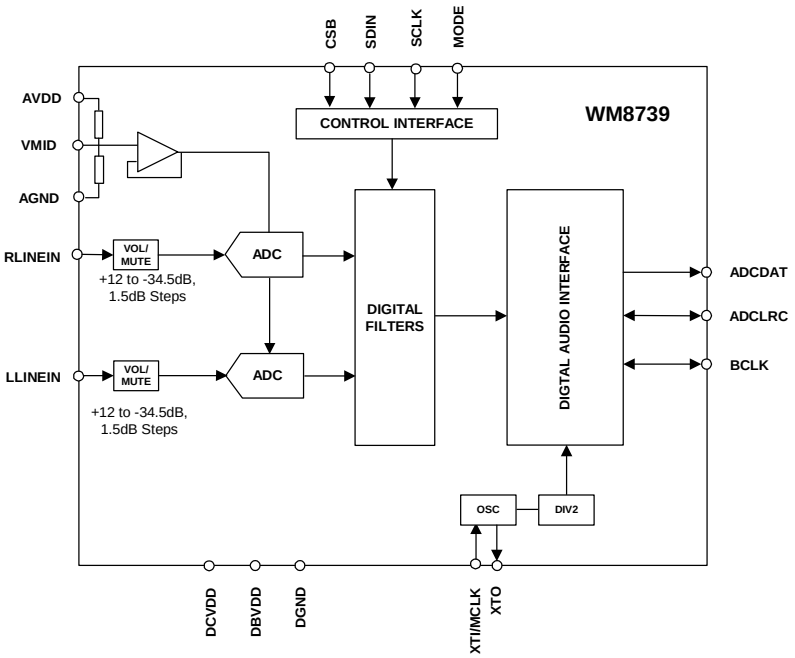
FEATURES

- 90dB SNR ('A' weighted @ 48kHz) ADC
- Low Power
  - 12mW all-on, 1.4mW standby ('L' version)
  - 41mW all-on, 5.3mW standby (standard version)
- Low Supply Voltages
  - 1.8 – 3.6V Analogue Supply ('L' version)
  - 2.7 – 3.6V Analogue Supply (standard version)
  - 1.42 – 3.6V Digital Supply (both versions)
- Input Volume and Mute Controls
- ADC Sampling Frequency: 8KHz – 96KHz
- Selectable ADC High Pass Filter
- 2 or 3-Wire MPU Serial Control Interface
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
  - Master or Slave Clocking Mode
- 20-Pin SSOP or 5x5mm QFN Package Options

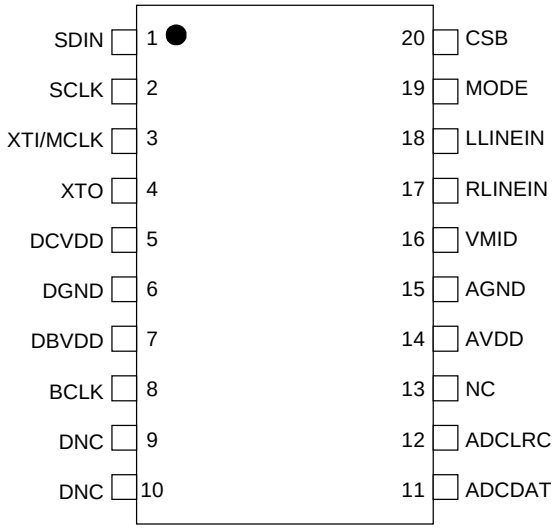
APPLICATIONS

- CD, Minidisc and DAT Recorders
- General Purpose Audio Digitisation

BLOCK DIAGRAM



PIN CONFIGURATION (SSOP)



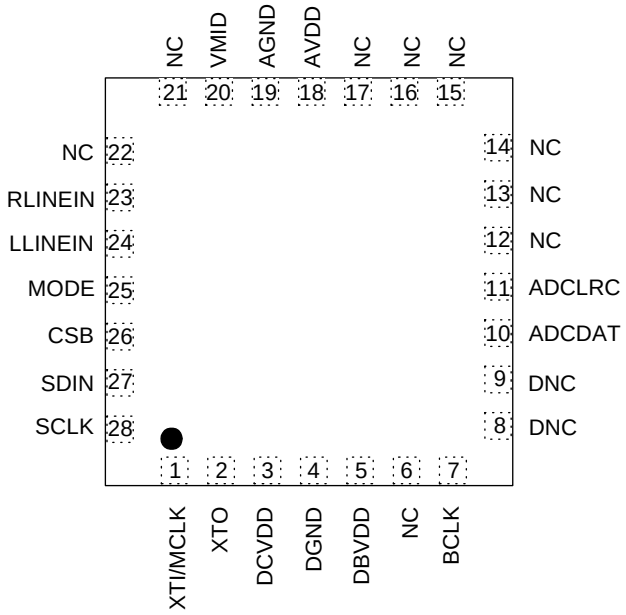
ORDERING INFORMATION (SSOP)

DEVICE	AVDD RANGE	PACKAGE
XWM8739EDS	2.7 to 3.6V	20-pin SSOP
XWM8739LEDS	1.8 to 3.6V	20-pin SSOP

PIN DESCRIPTION (SSOP PACKAGE)

PIN	NAME	TYPE	DESCRIPTION
1	SDIN	Digital Input	3-Wire MPU Data Input / 2-Wire MPU Data Input
2	SCLK	Digital Input	3-Wire MPU Clock Input / 2-Wire MPU Clock Input
3	XTI/MCLK	Digital Input	Crystal Input or Master Clock Input (MCLK)
4	XTO	Digital Output	Crystal Output
5	DCVDD	Supply	Digital Core VDD
6	DGND	Ground	Digital GND
7	DBVDD	Supply	Digital Buffers VDD
8	BCLK	Digital Input/Output	Digital Audio Port Clock
9	DNC	Test pin	Do not connect (leave this pin floating)
10	DNC	Test pin	Do not connect (leave this pin floating)
11	ADCDAT	Digital Output	ADC Digital Audio Data Output
12	ADCLRC	Digital Input/Output	ADC Sample Rate Clock
13	NC		No Internal Connection
14	AVDD	Supply	Analogue VDD
15	AGND	Ground	Analogue GND
16	VMID	Analogue Output	Mid-rail reference decoupling point
17	RLINEIN	Analogue Input	Right Channel Line Input (AC coupled)
18	LLINEIN	Analogue Input	Left Channel Line Input (AC coupled)
19	MODE	Digital Input	Control Interface Selection, Pull up (on power up only)
20	CSB	Digital Input	3-Wire MPU Chip Select/ 2-Wire MPU interface address selection

PIN CONFIGURATION (QFN)



ORDERING INFORMATION (QFN)

DEVICE	AVDD RANGE	PACKAGE
XWM8739EFL	2.7 to 3.6V	28-pin QFN (5x5x0.9 mm)
XWM8739LEFL	1.8 to 3.6V	

PIN DESCRIPTION (QFN PACKAGE)

PIN	NAME	TYPE	DESCRIPTION
1	XTI/MCLK	Digital Input	Crystal Input or Master Clock Input (MCLK)
2	XTO	Digital Output	Crystal Output
3	DCVDD	Supply	Digital Core VDD
4	DGND	Ground	Digital GND
5	DBVDD	Supply	Digital Buffers VDD
6	NC		No Internal Connection
7	BCLK	Digital Input/Output	Digital Audio Port Clock
8, 9	DNC	Test pin	Do not connect (leave this pin floating)
10	ADCDAT	Digital Output	ADC Digital Audio Data Output
11	ADCLRC	Digital Input/Output	ADC Sample Rate Clock
12 - 17	NC		No Internal Connection
18	AVDD	Supply	Analogue VDD
19	AGND	Ground	Analogue GND
20	VMID	Analogue Output	Mid-rail reference decoupling point
21, 22	NC		No Internal Connection
23	RLINEIN	Analogue Input	Right Channel Line Input (AC coupled)
24	LLINEIN	Analogue Input	Left Channel Line Input (AC coupled)
25	MODE	Digital Input	Control Interface Selection, Pull up (on power up only)
26	CSB	Digital Input	3-Wire MPU Chip Select/ 2-Wire MPU interface address selection

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+3.63
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		18.432MHz
Operating temperature range, T_A	-10°C	+70°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C
Package body temperature (soldering 10 seconds)		+240°C
Package body temperature (soldering 2 minutes)		+183°C

Notes

1. Analogue and digital grounds must always be within 0.3V of each other.
2. The digital supply core voltage must always be less than or equal to the analogue supply voltage or digital supply buffer voltage.
3. The digital supply buffer voltage must always be less than or equal to the analogue supply voltage.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		1.42	3.3	3.6	V
Digital supply range (Buffer)	DBVDD		2.7	3.3	3.6	V
Analogue supply range	AVDD	WM8739	2.7	3.3	3.6	V
		WM8739L	1.8	3.3	3.6	V
Ground	DGND,AGND			0		V
Standby Current Consumption				5		uA

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.3 x VDD	V
Input HIGH level	V_{IH}		0.7 x VDD			V
Output LOW	V_{OL}				0.1 x VDD	V
Output HIGH	V_{OH}		0.9 x VDD			V
Analogue Reference Levels						
Reference voltage	V_{VMID}			AVDD/2		V
Potential divider resistance	R_{VMID}			50K		Ohms
Input to ADC						
Input Signal Level (0dB)	V_{INLINE}	AVDD = 3.3V		1.0 0		Vrms dB
		AVDD = 1.8V (WM8739 only)		0.316 -10	0.545 -5.27	Vrms dBV
Signal to Noise Ratio (Note 1,2)	SNR	A-weighted, 0dB gain	85	90		dB
		A-weighted, 0dB gain @ fs = 96kHz		90		dB
		A-weighted, 0dB gain, AVDD = 2.7V		88		dB
		A-weighted, 0dB gain, AVDD = 1.8V (WM8739L only)		76		dB
Dynamic Range (Note 2)	DNR	A-weighted, -60dBV	85	90		dB
Total Harmonic Distortion	THD	-1dBV input, 0dB gain		-84 0.006	-74 0.02	dB %
		-10dBV, 0dB gain		-74 0.02		dB %
ADC channel separation		1kHz input		90		dB
Programmable Gain		1kHz input Rsource < 50 Ohms	-34.5	0	+12	dB
Programmable Gain Step Size				1.5		dB
Mute attenuation		0dB, 1kHz input		80		dB
Input Resistance	R_{INLINE}	0dB gain	20k	30k		Ohms
		12dB gain	10k	15k		Ohms
Input Capacitance	C_{INLINE}			10		pF

Notes

1. Ratio of output level with 1kHz full scale input, to the output level with all zero's into the digital input over a 20Hz to 20kHz bandwidth using an Audio analyser.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with a zero signal applied. (No 'Auto-zero' or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the r.m.s. values, of (Noise + Distortion)/Signal.
4. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

POWER CONSUMPTION

MODE DESCRIPTION	POWEROFF	OSCPD	ADCPD	LINEINPD	TYP. SUPPLY CURRENTS (MILLIAMPS)			
					I_{AVDD}	I_{DBVDD}	I_{DCVDD}	POWER (mW)
WM8739 (AVDD = 3.3V, DBVDD = 3.3V, DCVDD = 1.5V)								
ADC Running	0	0	0	0	9.79	1.58	2.40	41.12
Standby	0	0	1	1	0.014	1.56	0.074	5.31
Power Down	1	0	X	X	0.001	1.57	0.074	5.30
Power Down, Oscillator disabled	1	1	X	X	0.001	0.003	0.056	0.097
WM8739L (AVDD = 1.8V, DBVDD = 1.8V, DCVDD = 1.42V)								
ADC Running	0	0	0	0	3.93	0.875	2.35	11.99
Standby	0	0	1	1	0.007	0.755	0.018	1.397
Power Down	1	0	X	X	0.001	0.755	0.018	1.386
Power Down, Oscillator disabled	1	1	X	X	0.001	<1µA	<1µA	0.002

Table 1 Powerdown Mode Current Consumption Examples

Notes

1. T_A = +25°C. Slave Mode, fs = 48kHz, XTI/MCLK = 256fs (12.288MHz).
2. All figures are quiescent, with no signal.

DIGITAL AUDIO INTERFACE TIMING

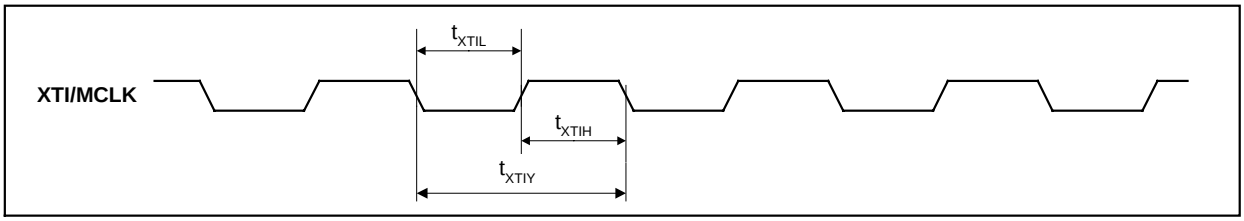


Figure 1 System Clock Timing Requirements

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
XTI/MCLK System clock pulse width high	T_{XTIH}		20			ns
XTI/MCLK System clock pulse width low	T_{XTIL}		20			ns
XTI/MCLK System clock cycle time	T_{XTIY}		50			ns

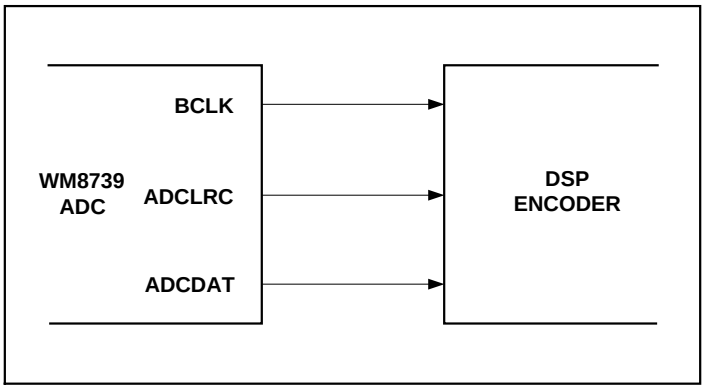


Figure 2 Master Mode Connection

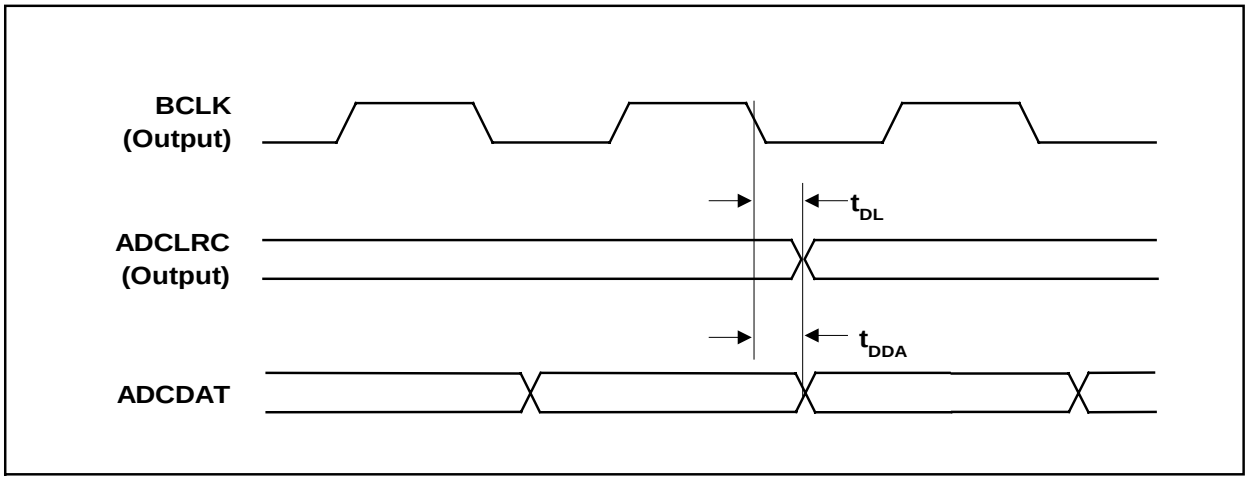


Figure 3 Digital Audio Data Timing – Master Mode

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
ADCLRC propagation delay from BCLK falling edge	t_{DL}		0		10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}		0		10	ns

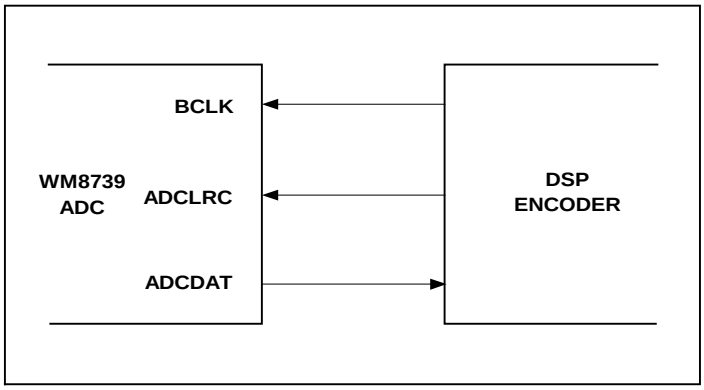


Figure 4 Slave Mode Connection

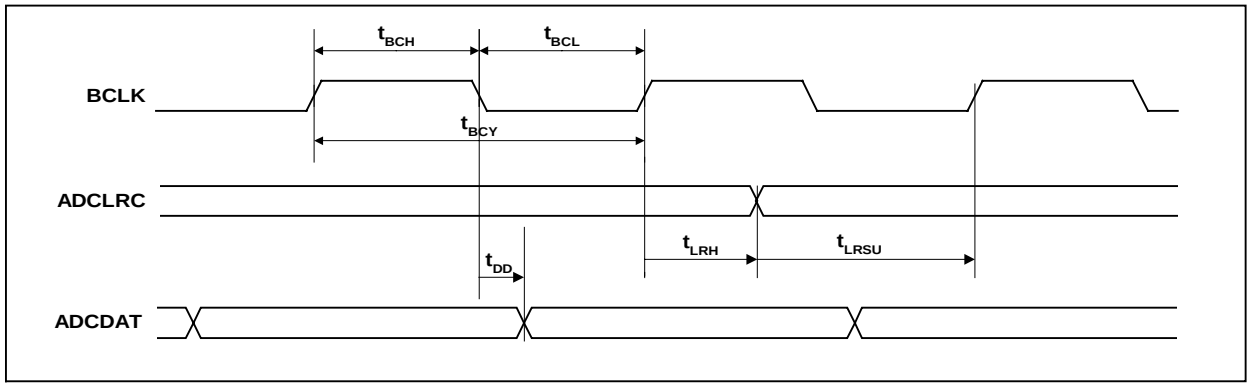


Figure 5 Digital Audio Data Timing – Slave Mode

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCLK cycle time	t_{BCY}		50			ns
BCLK pulse width high	t_{BCH}		20			ns
BCLK pulse width low	t_{BCL}		20			ns
ADCLRC set-up time to BCLK rising edge	t_{LRSU}		10			ns
ADCLRC hold time from BCLK rising edge	t_{LRH}		10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}		0		10	ns

MPU INTERFACE TIMING

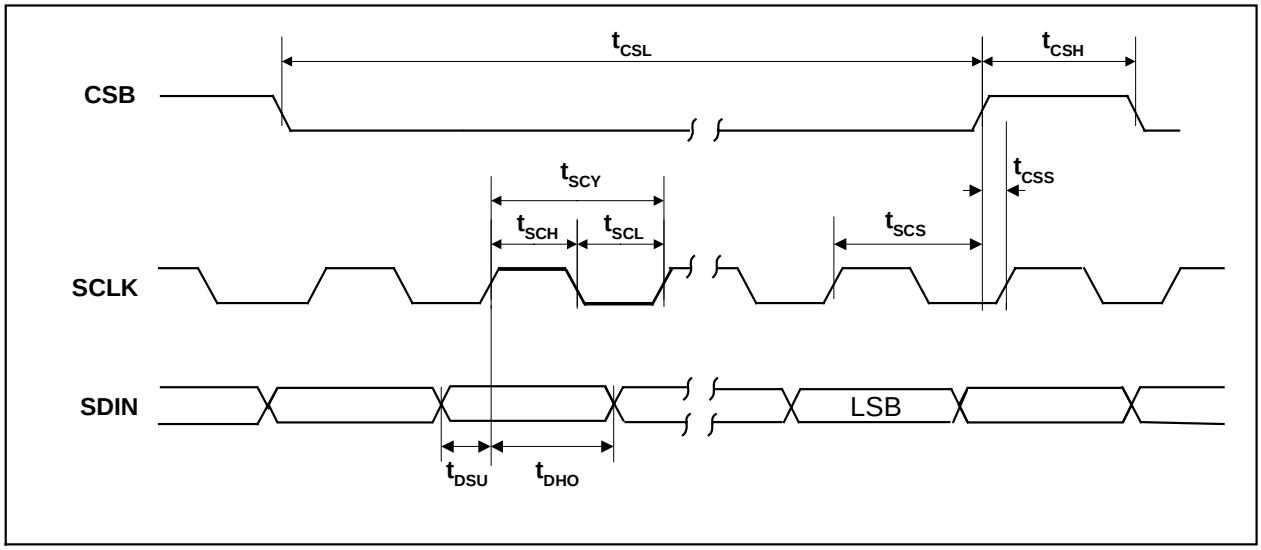


Figure 6 Program Register Input Timing – 3-Wire MPU Serial Control Mode

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCLK rising edge to CSB rising edge	t_{SCS}		500			ns
SCLK pulse cycle time	t_{SCY}		80			ns
SCLK pulse width low	t_{SCL}		20			ns
SCLK pulse width high	t_{SCH}		20			ns
SDIN to SCLK set-up time	t_{DSU}		20			ns
SCLK to SDIN hold time	t_{DHO}		20			ns
CSB pulse width low	t_{CSL}		20			ns
CSB pulse width high	t_{CSH}		20			ns
CSB rising to SCLK rising	t_{CSS}		20			ns

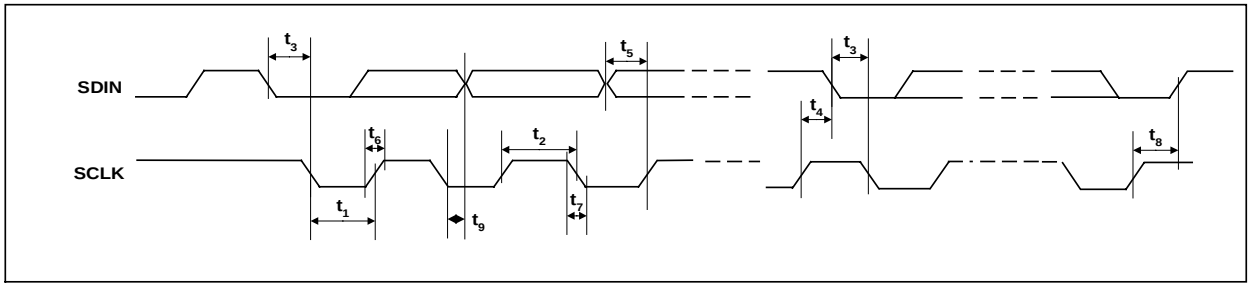


Figure 7 Program Register Input Timing – 2-Wire MPU Serial Control Mode

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCLK Frequency			0		400	kHz
SCLK Low Pulse-Width	t_1		600			ns
SCLK High Pulse-Width	t_2		1.3			us
Hold Time (Start Condition)	t_3		600			ns
Setup Time (Start Condition)	t_4		600			ns
Data Setup Time	t_5		100			ns
SDIN, SCLK Rise Time	t_6				300	ns
SDIN, SCLK Fall Time	t_7				300	ns
Setup Time (Stop Condition)	t_8		600			ns
Data Hold Time	t_9				900	ns

DEVICE DESCRIPTION

INTRODUCTION

The WM8739 is a low power analogue to digital converter (ADC) designed for audio recording. Its features, performance and low power consumption make it ideal for recordable CD players, MP3 players and portable mini-disc players.

The device includes programmable level line inputs, a crystal oscillator, configurable digital audio interface and a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs.

The WM8739 has low noise line inputs with programmable +12dB to –34.5dB logarithmic volume adjustments and mute.

The ADC is of a high quality using a multi-bit high-order oversampling architecture delivering optimum performance with low power consumption. The output from the ADC is available on the digital audio interface. The ADC includes a digital high pass filter to remove unwanted dc components from the audio signal.

The design of the WM8739 has given much attention to power consumption without compromising performance. It includes the ability to power off parts of the circuitry under software control, including a standby and power off mode.

The device caters for a number of different sampling rates including industry standard 8kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz.

There are two unique schemes featured within the programmable sample rates of the WM8739: Normal industry standard 256/384 fs sampling mode may be used. A special USB sampling mode is also included, whereby all audio sampling rates can be generated from a 12.00MHZ USB clock. The WM8739's unique sample rate converter thus allows the user to generate the required sampling rate clocks from the 12MHz USB clock. The digital filters used for recording are optimised for each sampling rate used.

The digitised output is available in a number of audio data formats I^2S, DSP Mode (a burst mode in which frame sync plus 2 data packed words are transmitted), MSB-First, left justified and MSB-First, right justified. The digital audio interface can operate in both master or slave modes.

The WM8739 can generate the system master clock using an on-chip crystal oscillator, or alternatively it can accept an external master clock from the audio system. All features are software controlled using either a 2 or 3-wire MPU interface.

LINE INPUTS

The WM8739 provides Left and Right channel line inputs (RLINEIN and LLINEIN). The inputs are high impedance and low capacitance, thus ideally suited to receiving line level signals from external Hi-Fi and other audio equipment.

Both line inputs include independent programmable volume level adjustments and mutes. The scheme is illustrated in Figure 8. Passive RF and active Anti-Alias filters are also incorporated within the line inputs. These prevent high frequencies aliasing into the audio band or otherwise degrading performance.

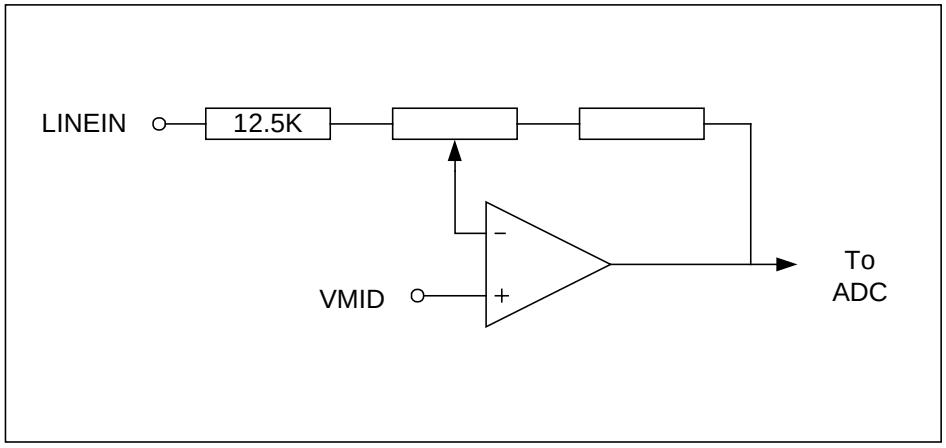


Figure 8 Line Input Schematic

LINE INPUT SCHEMATIC

The gain between the line inputs and the ADC is logarithmically adjustable from +12dB to –34.5dB in 1.5dB steps under software control. The ADC Full Scale input is 1.0V rms at AVDD = 3.3 volts. Any voltage greater than full scale will possibly overload the ADC and cause distortion. Note that the full scale input tracks directly with AVDD. The gain is independently adjustable on both Right and Left Line Inputs. However, by setting the INBOTH bit whilst programming the volume control, both channels are simultaneously updated. Use of INBOTH reduces the required number of software writes required. The line inputs can be muted in the analogue domain under software control. The software control registers are shown below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000000 Left Line In	4:0	LINVOL[0:4]	10111 (0dB)	Left Channel Line Input Volume Control 11111 = +12dB . . 1.5dB steps down to 00000 = -34.5dB
	7	LINMUTE	1	Left Channel Line Input Mute 1 = Enable Mute 0 = Disable Mute
	8	LRINBOTH	0	Left to Right Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of LINVOL[0:4] and LINMUTE to RINVOL[0:4] and RINMUTE 0 = Disable Simultaneous Load
0000001 Right Line In	4:0	RINVOL[0:4]	10111 (0dB)	Right Channel Line Input Volume Control 11111 = +12dB . . 1.5dB steps down to 00000 = -34.5dB
	7	RINMUTE	1	Left Channel Line Input Mute 1 = Enable Mute 0 = Disable Mute
	8	RLINBOTH	0	Right to Left Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of RINVOL[0:4] and RINMUTE to LINVOL[0:4] and LINMUTE 0 = Disable Simultaneous Load

Table 2 Line Input Software Control

The line inputs are biased internally through the operational amplifier to VMID. Whenever the line inputs are muted or the device placed into standby mode, the line inputs are kept biased to VMID using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when re-activating the inputs.

The external components required to complete the line input application are shown in the Figure 9.

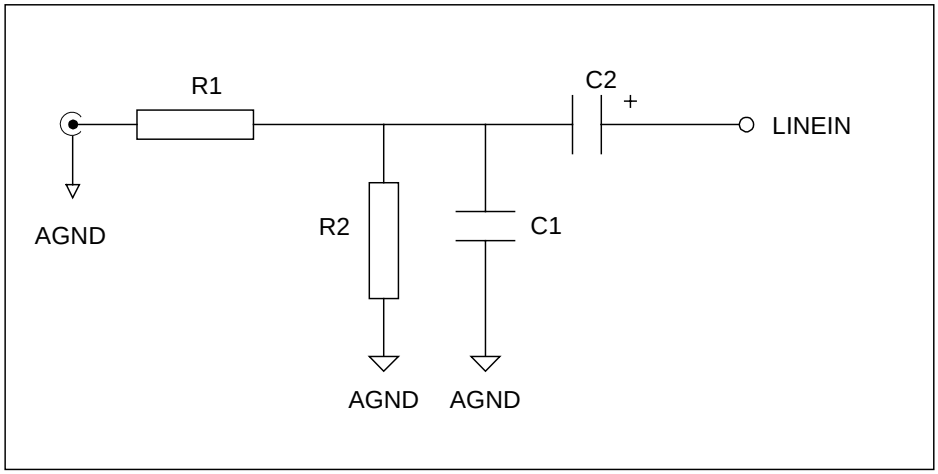


Figure 9 Line Input Application Drawing

For interfacing to a typical CD system, it is recommended that the input is scaled to ensure that there is no clipping at the input. R1 = 5K, R2= 5K, C1=47pF, C2=470nF (10V ceramic type).

R1 and R2 form a resistive divider to attenuate the 2 Vrms output from a CD player to a 1 Vrms level, so avoiding overloading the inputs. R2 also provides a discharge path for C2, thus preventing the input to C2 charging to an excessive voltage which may otherwise damage any equipment connected that is not suitably protected against high voltages. C1 forms an RF low pass filter for increasing the rejection of RF interference picked up on any cables. C2 forms a DC blocking capacitor to remove the DC path between the WM8739 and the driving audio equipment. C2 together with the input impedance of the WM8739 form a high pass filter.

ADC

The WM8739 uses a multi-bit oversampled sigma-delta ADC. A single channel of the ADC is illustrated in the Figure 10.

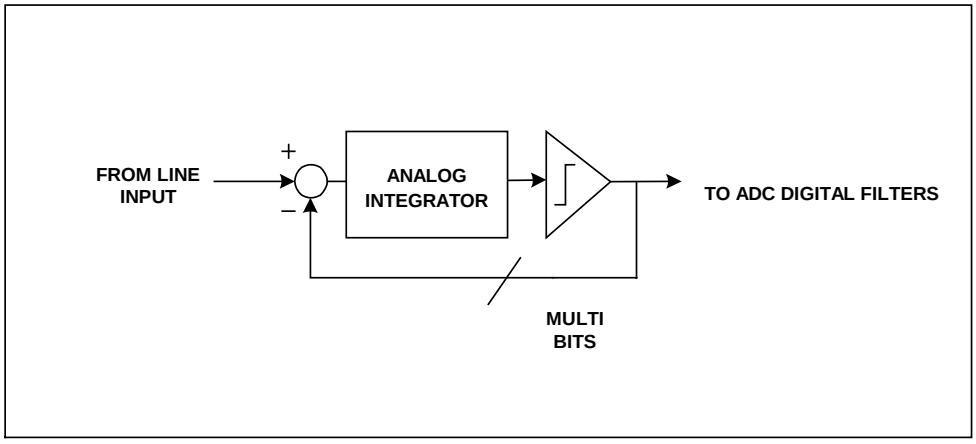


Figure 10 Multi-Bit Oversampling Sigma Delta ADC Schematic

The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise.

The ADC Full Scale input is 1.0V rms at AVDD = 3.3 volts. Any voltage greater than full scale will possibly overload the ADC and cause distortion. Note that the full scale input tracks directly with AVDD.

The device employs a pair of ADCs. The two channels cannot be selected independently.

The digital data from the ADC is fed for signal processing to the ADC Filters.

ADC FILTERS

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. Figure 11 illustrates the digital filter path.

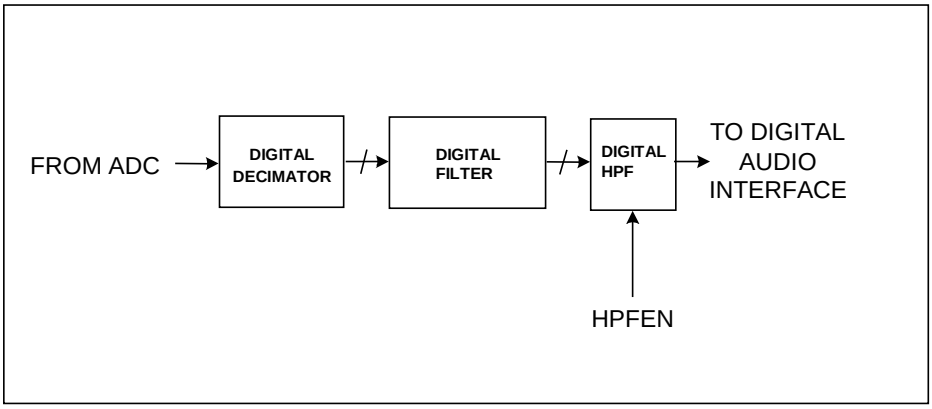


Figure 11 ADC Digital Filter

ADC DIGITAL FILTER

The ADC digital filters contain a digital high pass filter, selectable via software control. The high-pass filter response is detailed in the Digital Filter Characteristics section. When the high-pass filter is enabled the dc offset is continuously calculated and subtracted from the input signal. By setting HPOR the last calculated dc offset value is stored when the high-pass filter is disabled and will continue to be subtracted from the input signal. If the dc offset changed, the stored and subtracted value will not change unless the high-pass filter is enabled. The software control is shown in Table 3.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000101 Audio Path Control	0	ADCHPD	0	ADC High Pass Filter Enable (Digital) 1 = Disable High Pass Filter 0 = Enable High Pass Filter
	4	HPOR	0	Store dc offset when High Pass Filter disabled 1 = store offset 0 = clear offset

Table 3 ADC Software Control

There are several types of ADC filter, the frequency and phase responses of which are shown in Digital Filter Characteristics. The filter types are automatically configured depending on the sample rate chosen. Refer to the sample rate section for more details.

CLOCKING SCHEMES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. To allow WM8739 to be used in a centrally clocked system, the WM8739 is capable of either generating this 'system' clock itself or receiving it from an external source as will be discussed.

For applications where it is desirable that the WM8739 is the system clock source, then clock generation is achieved through the use of a suitable crystal connected between the XTI/MCLK input and XTO output pins (see CRYSTAL OSCILLATOR section).

For applications where a component other than the WM8739 will generate the reference clock, the external system can be applied directly through the XTI/MCLK input pin with no software configuration necessary. Note that in this situation, the oscillator circuit of the WM8739 can be safely powered down to conserve power (see POWER DOWN section)

CRYSTAL OSCILLATOR

The WM8739 includes a crystal oscillator circuit that allows the audio system's reference clock to be generated on the device. The crystal oscillator is a low radiation type, designed for low EMC. A typical application circuit is shown in Figure 12.

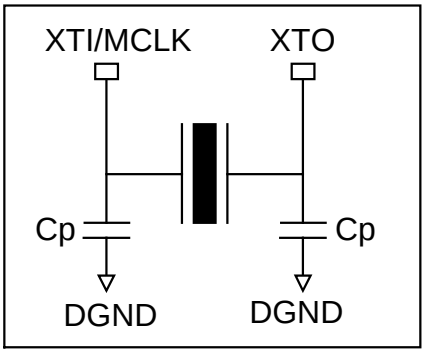


Figure 12 Crystal Oscillator Application Circuit

For crystals with a 30pF fundamental load capacitance, a value of 5pF for Cp is recommended.

The WM8739 crystal oscillator provides an extremely low jitter clock source. Low jitter clocks are a requirement for a high quality audio ADC, regardless of the converter architecture. The WM8739 architecture is less susceptible than most converter techniques but still requires clocks with less than approximately 1ns of jitter to maintain performance. In applications where there is more than one source for the master clock, it is recommended that the clock is generated by the WM8739 to minimise such problems.

CORE CLOCK

The WM8739 DSP core can be clocked either by MCLK or MCLK divided by 2. This is controlled by software as shown in Table 4 below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001000 Sampling Control	6	CLKIDIV2	0	Core Clock divider select 1 = Core Clock is MCLK divided by 2 0 = Core Clock is MCLK

Table 4 Software Control of Core Clock

Having a programmable MCLK divider allows the device to be used in applications where higher frequency master Clocks are available. For example the device can support 512fs master clocks whilst fundamentally operating in a 256fs mode.

DIGITAL AUDIO INTERFACES

WM8739 may be operated in either one of the 4 offered audio interface modes. These are:

- Right justified
- Left justified
- I^2S
- DSP mode

All four of these modes are MSB first.

The digital audio interface takes the data from the internal ADC digital filters and places it on ADCDAT and ADCLRC. ADCDAT is the formatted digital audio data stream output from the ADC digital filters with left and right channels multiplexed together. ADCLRC is an alignment clock that controls whether Left or Right channel data is present on the ADCDAT line. ADCDAT and ADCLRC are synchronous with the BCLK signal with each data bit transition signified by a BCLK high to low transition. ADCDAT is always an output. BCLK and ADCLRC maybe an input or an output depending whether the device is in master or slave mode. Refer to the MASTER/SLAVE OPERATION section.

There are four digital audio interface formats accommodated by the WM8739. These are shown in the figures below. Refer to the Electrical Characteristic section for timing information.

Left Justified mode is where the MSB is available on the first rising edge of BCLK following a LRCLK transition.

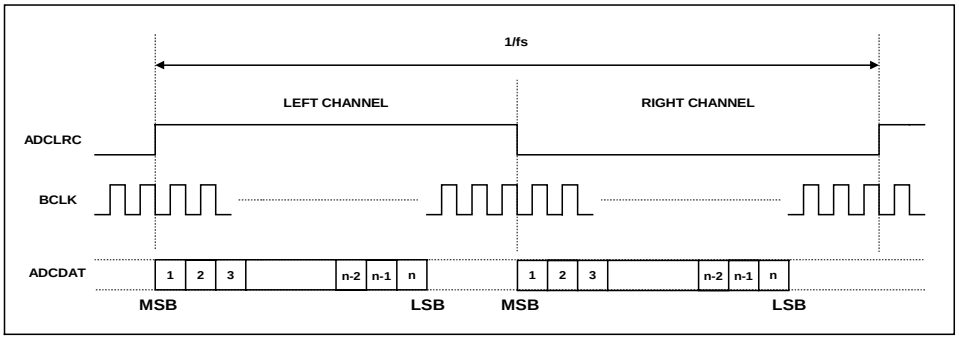


Figure 13 Left Justified Mode

I^{2}S mode is where the MSB is available on the 2nd rising edge of BCLK following a LRCLK transition.

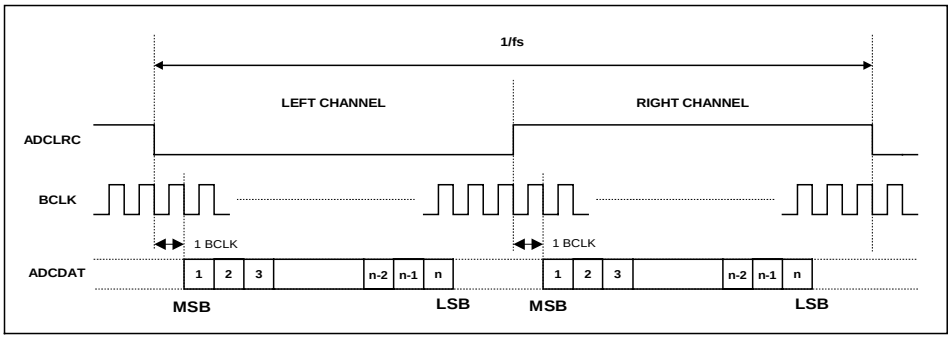


Figure 14 I^{2}S Mode

Right Justified mode is where the LSB is available on the rising edge of BCLK preceding a LRCLK transition, yet MSB is still transmitted first.

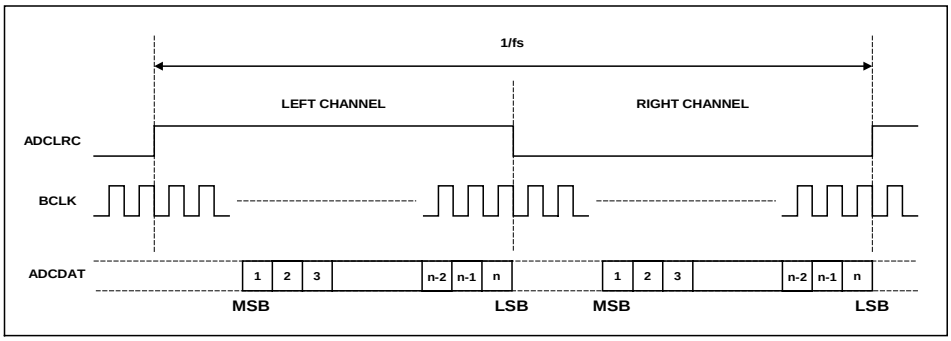


Figure 15 Right Justified Mode

DSP mode is where the left channel MSB is available on either the 1st or 2nd rising edge of BCLK (selectable by LRP) following a LRCLK transition high. Right channel data immediately follows left channel data.

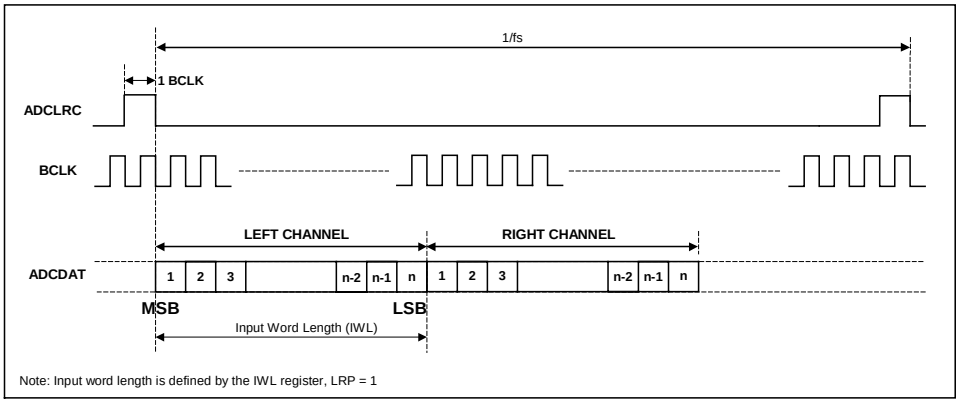


Figure 16 DSP Mode

The ADC digital audio interface modes are software configurable as indicated in Figure 16. Note that dynamically changing the software format may results in erroneous operation of the interfaces and is therefore not recommended.

The length of the digital audio data is programmable at 16/20/24 or 32 bits. Refer to the software control table below. The data is signed 2's complement. The ADC digital filters process data using 24 bits. If the ADC is programmed to output 16 or 20 bit data then it strips the LSBs from the 24 bit data. If the ADC is programmed to output 32 bits then it packs the LSBs with zeros.

ADCDAT is always an output. It powers up and returns from standby 'low'.

ADCLRC and BCLK can be either outputs or inputs depending on whether the device is configured as a master or slave. If the device is a master then the ADCLRC and BCLK signals are outputs that default low. If the device is a slave then the ADCLRC and BCLK are inputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000111 Digital Audio Interface Format	1:0	FORMAT[1:0]	10	Audio Data Format Select 11 = DSP Mode, frame sync + 2 data packed words 10 = I^2S Format, MSB-First left-1 justified 01 = MSB-First, left justified 00 = MSB-First, right justified
	3:2	IWL[1:0]	10	Input Audio Data Bit Length Select 11 = 32 bits 10 = 24 bits 01 = 20 bits 00 = 16 bits
	4	LRP	0	DSP mode A/B select (in DSP mode only) 1 = MSB is available on 2nd BCLK rising edge after LRC rising edge 0 = MSB is available on 1st BCLK rising edge after LRC rising edge
	6	MS	0	Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode

Table 5 Digital Audio Interface Control

Note:

Right justified 32 bit mode is not supported, but if selected, will put the WM8739 into 24 bit right justified mode.

MASTER AND SLAVE MODE OPERATION

The WM8739 can be configured as either a master or slave mode device. As a master mode device the WM8739 controls sequencing of the data and clocks on the digital audio interface. As a slave device the WM8739 responds with data to the clocks it receives over the digital audio interface. The mode is set with the MS bit of the control register as shown in Table 6.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000111 Digital Audio Interface Format	6	MS	0	Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode

Table 6 Programming Master/Slave Modes

As a master mode device the WM8739 controls the sequencing of data transfer (ADCDAT) and output of clocks (BCLK, ADCLRC) over the digital audio interface. It uses the timing generated from either its on-board crystal or the MCLK input as the reference for the clock and data transitions. This is illustrated in Figure 17. ADCDAT is always an output from the WM8739 independent of master or slave mode.

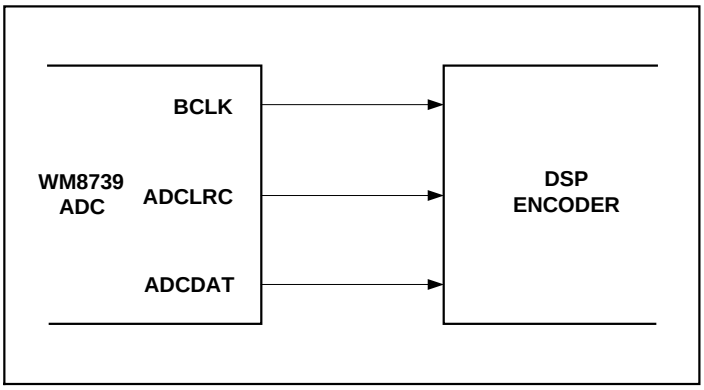


Figure 17 Master Mode

As a slave device the WM8739 sequences the data transfer (ADCDAT) over the digital audio interface in response to the external applied clocks (BCLK, ADCLRC). This is illustrated Figure 18.

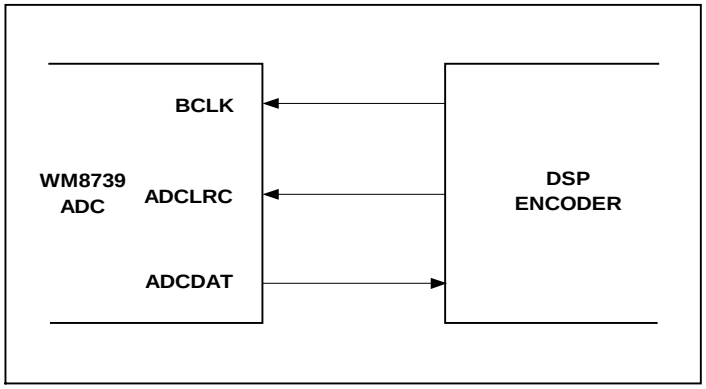


Figure 18 Slave Mode

AUDIO DATA SAMPLING RATES

The WM8739 provides for two modes of operation (normal and USB) to generate the required ADC sampling rate. Normal and USB modes are programmed under software control according to the table below.

In Normal mode, the user controls the sample rate by using an appropriate MCLK or crystal frequency and the sample rate control register setting. The WM8739 can support sample rates from 8ks/s up to 96ks/s.

In USB mode, the user must use a fixed MLCK or crystal frequency of 12MHz to generate sample rates from 8ks/s to 96ks/s. It is called USB mode since the common USB (Universal Serial Bus) clock is at 12MHz and the WM8739 can be directly used within such systems. WM8739 can generate all the normal audio sample rates from this one Master Clock frequency, removing the need for different master clocks or PLL circuits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	
0001000 Sampling Control	0	USB/ NORMAL	0	Mode Select 1 = USB mode (250/272fs) 0 = Normal mode (256/384fs)	
	1	BOSR	0	Base Over-Sampling Rate	
				USB Mode 0 = 250fs 1 = 272fs	Normal Mode 0 = 256fs 1 = 384fs
	5:2	SR[3:0]	0000	ADC sample rate control; See USB Mode and Normal Mode Sample Rate sections for operation	

Table 7 Sample Rate Control

NORMAL MODE SAMPLE RATES

In normal mode MCLK/crystal oscillator is set up according to the desired sample rate of the ADC. For ADC sampling rates of 8, 32, 48 or 96KHz, MCLK frequencies of either 12.288MHz (256fs) or 18.432MHz (384fs) can be used. For ADC sampling rates of 8, 44.1 or 88.2KHz from MCLK frequencies of either 11.2896MHz (256fs) or 16.9344MHz (384fs) can be used.

The table below should be used to set up the device to work with the various sample rate combinations. For example if the user wishes to use the WM8739 in normal mode with the ADC sample rate at 48KHz, then the device should be programmed with BOSR = 0, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0 with a 12.288MHz MCLK or with BOSR = 1, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0 with a 18.432MHz MCLK. The ADC will then operate with a Digital Filter of type 1, refer to Digital Filter Characteristics section for an explanation of the different filter types.

SAMPLING RATE	MCLK FREQUENCY	SAMPLE RATE REGISTER SETTINGS					DIGITAL FILTER TYPE
kHz	MHz	BOSR	SR3	SR2	SR1	SR0	
48	12.288	0	0	0	0	0	1
	18.432	1	0	0	0	0	
8	12.288	0	0	0	1	0	1
	18.432	1	0	0	1	0	
32	12.288	0	0	1	1	0	1
	18.432	1	0	1	1	0	
96	12.288	0	0	1	1	1	2
	18.432	1	0	1	1	1	
44.1	11.2896	0	1	0	0	0	1
	16.9344	1	1	0	0	0	
8 (Note 1)	11.2896	0	1	0	1	0	1
	16.9344	1	1	0	1	0	
88.2	11.2896	0	1	1	1	1	2
	16.9344	1	1	1	1	1	

Table 8 Normal Mode Sample Rate Look-up Table

Notes:

1. 8k not exact, actual = 8.018kHz

2. All other combinations of BOSR and SR[3:0] that are not in the truth table are invalid

The BOSR bit represents the base over-sampling rate. This is the rate that the WM8739 digital signal processing is carried out at. In Normal mode, with BOSR = 0, the base over-sampling rate is at 256fs, with BOSR = 1, the base over-sampling rate is at 384fs. This can be used to determine the actual audio data rate produced by the ADC.

Example scenarios are:

1. with a requirement that the ADC data rate is 8kHz, then choosing MCLK = 12.288MHz the device is programmed with BOSR = 0 (256fs), SR3 = 0, SR2 = 0, SR1 = 1, SR0 = 0.The ADC output data rate will then be exactly 8kHz (derived from 12.288MHz/256 x1/6)

2. with a requirement that ADC data rate is 8kHz, then choosing MCLK = 16.9344MHz the device is programmed with BOSR = 1 (384fs), SR3 = 1, SR2 = 0, SR1 = 0, SR0 = 1. The ADC will no longer output data at exactly 8.000KHz, instead it will be 8.018kHz (derived from 16.9344MHz/384 x 2/11). A slight (sub 0.5%) pitch shift will therefore result in the 8kHz audio data and (importantly) the user must ensure that the data across the digital interface is correctly synchronised at the 8.018kHz rate.

The exact sample rates achieved are defined by the relationships in Table 9.

TARGET SAMPLING RATE	ACTUAL SAMPLING RATE			
	BOSR=0 (256fs)		BOSR=1 (384fs)	
	MCLK=12.288	MCLK=11.2896	MCLK=18.432	MCLK=16.9344
kHz	kHz	kHz	kHz	kHz
8	8	8.018	8	8.018
	12.288MHz/256 x 1/6	11.2896MHz/256 x 2/11	18.432MHz/384 x 1/6	16.9344MHz/384 x 2/11
32	32	*not available*	32	*not available*
	12.288MHz/256 x 2/3		18.432MHz/384x 2/3	
44.1	*not available*	44.1	*not available*	44.1
		11.2896MHz/256		16.9344MHz /384
48	48	*not available*	48	*not available*
	12.288MHz/256		18.432MHz/384	
88.2	*not available*	88.2	*not available*	88.2
		11.2896MHz/384 x 2		16.9344MHz /384 x 2
96	96	*not available*	96	*not available*
	12.288MHz/256 x 2		18.432MHz/384 x 2	

Table 9 Normal Mode Actual Sample Rates

128/192fs NORMAL MODE

The Normal Mode sample rates are designed for standard 256fs and 384fs MCLK rates. However the WM8739 is also capable of being clocked from a 128/192fs MCLK for application over limited sampling rates as shown in the table below.

SAMPLING RATE	MCLK FREQUENCY	SAMPLE RATE REGISTER SETTINGS					DIGITAL FILTER TYPE
kHz	MHz	BOSR	SR3	SR2	SR1	SR0	
48	6.144	0	0	1	1	1	2
	9.216	1	0	1	1	1	
44.1	5.6448	0	1	1	1	1	2
	8.4672	1	1	1	1	1	

Table 10 128/192fs Normal Mode Sample Rate Look-up Table

512/768fs NORMAL MODE

512fs and 768fs MCLK rates can be accommodated by using the CLKIDIV2 bit. The core clock to the DSP will be divided by 2 so an external 512/768 MCLK will become 256/384fs internally and the device otherwise operates as in Table 8 but with MCLK at twice the specified rate. See Table 4 for software control.

USB MODE SAMPLE RATES

In USB mode the MCLK/crystal oscillator input is 12MHz only.

SAMPLING RATE	MCLK FREQUENCY	SAMPLE RATE REGISTER SETTINGS					DIGITAL FILTER TYPE
kHz	MHz	BOSR	SR3	SR2	SR1	SR0	
48	12.000	0	0	0	0	0	0
44.1 (Note 2)	12.000	1	1	0	0	0	1
8	12.000	0	0	0	1	0	0
8 (Note 1)	12.000	1	1	0	1	0	1
32	12.000	0	0	1	1	0	0
96	12.000	0	0	1	1	1	3
88.2 (Note 3)	12.000	1	1	1	1	1	2

Table 11 USB Mode Sample Rate Look-up Table

Notes:

1. 8k not exact, actual = 8.021kHz
2. 44.1k not exact, actual = 44.118kHz
3. 88.2k not exact, actual = 88.235kHz
4. All other combinations of BOSR and SR[3:0] that are not in the truth table are invalid

The table above can be used to set up the device to work with various sample rate combinations. For example if the user wishes to use the WM8739 in USB mode with the ADC sample rate at 48kHz, then the device should be programmed with BOSR = 0, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0. The ADC will then operate with a Digital Filter of type 0, refer to Digital Filter Characteristics section for an explanation of the different filter types.

The BOSR bit represents the base over-sampling rate. This is the rate that the WM8739 digital signal processing is carried out at and the sampling rate will always be a sub-multiple of this. In USB mode, with BOSR = 0, the base over-sampling rate is defined at 250fs, with BOSR = 1, the base over-sampling rate is defined at 272fs. This can be used to determine the actual audio sampling rate produced by the ADC.

Example scenarios are:

1. with a requirement that the ADC data sampling rate is 8KHz the device is programmed with BOSR = 0 (250fs), SR3 = 0, SR2 = 0, SR1 = 1, SR0 = 0.The ADC will then be exactly 8kHz (derived from 12MHz/250 x 1/6).
2. with a requirement that ADC data rate is 8KHz the device is programmed with BOSR = 1 (272fs), SR3 = 0, SR2 = 0, SR1 = 1, SR0 = 0. The ADC will not output data at exactly 8kHz, instead it will be 8.021kHz (derived from 12MHz/272 x 2/11). A slight (sub 0.5%) pitch shift will therefore result in the 8kHz audio data and (more importantly) the user must ensure that the data across the digital interface is correctly synchronised at the 8.021kHz rate.

The exact sample rates supported for all combinations are defined by the relationships in Table 12 below.

TARGET SAMPLING RATE	ACTUAL SAMPLING RATE	
	BOSR=0 (250fs)	BOSR=1 (272fs)
kHz	kHz	kHz
8	8	8.021
	12MHz/(250 x 48/8)	12MHz/(272 x 11/2)
32	32	*not available*
	12MHz/(250 x 48/32)	
44.1	*not available*	44.117
		12MHz/272
48	48	*not available*
	12MHz/250	
88.2	*not available*	88.235
		12MHz/136
96	96	*not available*
	12MHz/125	

Table 12 USB Mode Actual Sample Rates

ACTIVATING DSP AND DIGITAL AUDIO INTERFACE

To prevent any communication problems from arising across the Digital Audio Interface the Audio Interface is disabled (tristate). Once the Audio Interface and the Sampling Control has been programmed it is activated by setting the ACTIVE bit under Software Control.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001001 Active Control	0	ACTIVE	0	Activate Interface 1 = Active 0 = Inactive

Table 13 Activating DSP and Digital Audio Interface

It is recommended that between changing any content of Digital Audio Interface or Sampling Control Register that the active bit is reset then set.

SOFTWARE CONTROL INTERFACE

The software control interface may be operated using either a 3-wire or 2-wire MPU interface. Selection of interface format is achieved by setting the state of the MODE pin.

In 3-wire mode, SDIN is used for the program data, SCLK is used to clock in the program data and CSB is used to latch in the program data. In 2-wire mode, SDIN is used for serial data and SCLK is used for the serial clock. In 2-wire mode, the state of the CSB pin allows the user to select one of two addresses.

SELECTION OF SERIAL CONTROL MODE

The serial control interface may be selected to operate in either 2 or 3-wire mode. This is achieved by setting the state of the MODE pin.

MODE	INTERFACE FORMAT
0	2 wire
1	3 wire

Table 14 Control Interface Mode Selection

3-WIRE SERIAL CONTROL MODE

The WM8739 can be controlled using a 3-wire serial interface. SDIN is used for the program data, SCLK is used to clock in the program data and CSB is used to latch in the program data. The 3-wire interface protocol is shown in Figure 19.

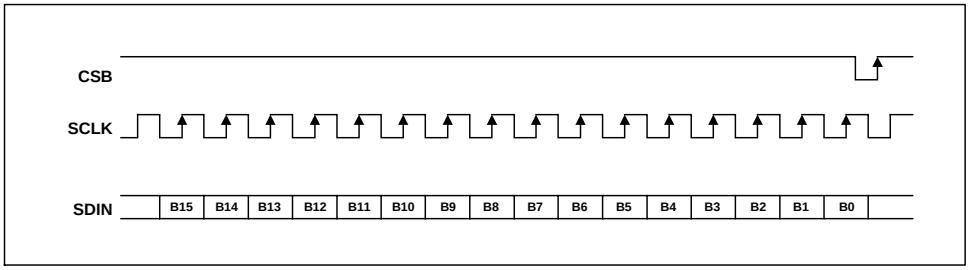


Figure 19 3-Wire Serial Interface

Notes:

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits

2-WIRE SERIAL CONTROL MODE

The WM8739 supports a 2-wire MPU serial interface. The device operates as a slave device only. The WM8739 has one of two slave addresses that are selected by setting the state of pin 20, (CSB).

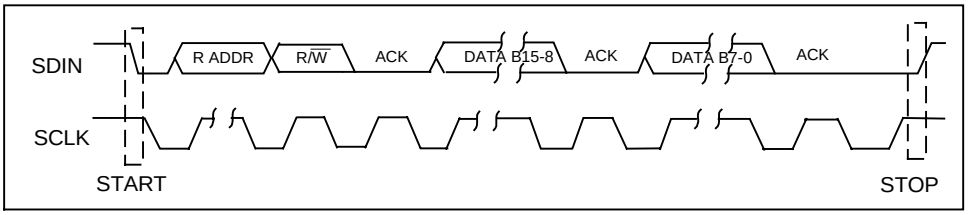


Figure 20 2-Wire Serial Interface

Notes:

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits

CSB STATE (DEFAULT = LOW)	ADDRESS
0	0011010
1	0011011

Table 15 2-Wire MPU Interface Address Selection

To control the WM8739 on the 2-wire bus the master control device must initiate a data transfer by establishing a start condition, defined by a high to low transition on SDIN while SCLK remains high. This indicates that an address and data transfer will follow. All peripherals on the 2-wire bus respond to the start condition and shift in the next eight bits (7-bit address + R/W bit). The transfer is MSB first. The 7-bit address consists of a 6-bit base address + a single programmable bit to select one of two available addresses for this device (see Table 15). If the correct address is received and the R/W bit is '0', indicating a write, then the WM8739 will respond by pulling SDIN low on the next clock pulse (ACK). The WM8739 is a write only device and will only respond to the R/W bit indicating a write. If the address is not recognised the device will return to the idle condition and wait for a new start condition and valid address.

Once the WM8739 has acknowledged a correct address, the controller will send eight data bits (bits B[15]-B[8]). WM8739 will then acknowledge the sent data by pulling SDIN low for one clock pulse. The controller will then send the remaining eight data bits (bits B[7]-B[0]) and the WM8739 will then acknowledge again by pulling SDIN low.

A stop condition is defined when there is a low to high transition on SDIN while SCLK is high. If a start or stop condition is detected out of sequence at any point in the data transfer then the device will jump to the idle condition.

After receiving a complete address and data sequence the WM8739 returns to the idle state and waits for another start condition. Each write to a register requires the complete sequence of start condition, device address and R/W bit followed by the 16 register address and data bits.

POWER DOWN MODES

The WM8739 contains power conservation modes in which various circuit blocks may be safely powered down in order to conserve power. This is software programmable as shown in the table below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000110 Power Down Control	0	LINEINPD	1	Line Input Power Down 1 = Enable Power Down 0 = Disable Power Down
	2	ADCPD	1	ADC Power Down 1 = Enable Power Down 0 = Disable Power Down
	5	OSCPD	0	Oscillator Power Down 1 = Enable Power Down 0 = Disable Power Down
	7	POWEROFF	1	Power Off Device 1 = Device Power Off 0 = Device Power On

Table 16 Power Conservation Modes Software Control

Unused register bits 1,3,4,6 should be set to '1' when writing to this register. The power down control can be used to either a) permanently disable functions when not required in certain applications or b) to dynamically power up and down functions depending on the operating mode, e.g.: during playback or record. Please follow the special instructions below if dynamic implementations are being used.

OSCPD: Powers off the on board crystal oscillator. The MCLK input will function independently of the Oscillator being powered down.

The device can be put into a standby mode (STANDBY) by powering down all the audio circuitry under software control as shown in Table 17.

POWEROFF	OSCPD	ADCPD	LINEINPD	DESCRIPTION
0	0	1	1	STANDBY, but with Crystal Oscillator
0	1	1	1	STANDBY, Crystal oscillator not-available.

Table 17 Standby Mode

In STANDBY mode the Control Interface, a small portion of the digital and areas of the analogue circuitry remain active. The active analogue includes the analogue VMID reference so that the analogue line inputs remain biased to VMID. This reduces any audible effects caused by DC glitches when entering or leaving STANDBY mode.

The device can be powered off by writing to the POWEROFF bit of the Power Down register. In POWEROFF mode the Control Interface and a small portion of the digital remain active. The analogue VMID reference is disabled. As in STANDBY mode the crystal oscillator pin can be independently controlled. Refer to Table 18.

POWEROFF	OSCPD	ADCPD	LINEINPD	DESCRIPTION
1	0	X	X	POWEROFF, but with Crystal Oscillator OSC available
1	1	X	X	POWEROFF, Crystal oscillator not-available

Table 18 Power Off Mode

DEVICE RESETTING

The WM8739 contains a power on reset circuit that resets the internal state of the device to a known condition. The power on reset is applied as DCVDD powers on and released only after the voltage level of DCVDD crosses a minimum turn off threshold. If DCVDD later falls below a minimum turn on threshold voltage then the power on reset is re-applied. The threshold voltages and associated hysteresis are shown in the Electrical Characteristics table.

The user also has the ability to reset the device to a known state under software control as shown in the table below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001111 Reset Register	8:0	RESET	not reset	Reset Register Writing 00000000 to register resets device

Table 19 Software Control of Reset

When using the software reset. In 3-wire mode the reset is applied on the rising edge of CSB and released on the next rising edge of SCLK. In 2-wire mode the reset is applied for the duration of the ACK signal (approximately 1 SCLK period, refer to Figure 20).

REGISTER MAP

The complete register map is shown in Table 20. The detailed description can be found in the relevant text of the device description. There are 8 registers with 9 bits per register. These can be controlled using either the 2 wire or 3 wire MPU interface.

REGISTER	B 15	B 14	B 13	B 12	B 11	B 10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
R0 (00h)	0	0	0	0	0	0	0	LRIN BOTH	LIN MUTE	0	0	LINVOL				
R1 (02h)	0	0	0	0	0	0	1	RLIN BOTH	RIN MUTE	0	0	RINVOL				
R5 (0Ah)	0	0	0	0	1	0	1	0	0	0	0	HPOR	0	0	0	ADC HPD
R6 (0Ch)	0	0	0	0	1	1	0	0	PWR OFF	1	OSCPD	1	1	ADCPD	1	LINEIN PD
R7 (0Eh)	0	0	0	0	1	1	1	0	0	MS	0	LRP	IWL		FORMAT	
R8 (10h)	0	0	0	1	0	0	0	0	0	CLKI DIV2	SR				BOSR	USB/ NORM
R9 (12h)	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	ACTIVE
R15(1Eh)	0	0	0	1	1	1	1	RESET								
	ADDRESS							DATA								

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000000 Left Line In	4:0	LINVOL[0:4]	10111 (0dB)	Left Channel Line Input Volume Control 11111 = +12dB . . 1.5dB steps down to 00000 = -34.5dB
	7	LINMUTE	1	Left Channel Line Input Mute 1 = Enable Mute 0 = Disable Mute
	8	LRINBOTH	0	Left to Right Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of LINVOL[0:4] and LINMUTE to RINVOL[0:4] and RINMUTE 0 = Disable Simultaneous Load
0000001 Right Line In	4:0	RINVOL[0:4]	10111 (0dB)	Right Channel Line Input Volume Control 11111 = +12dB . .1.5dB steps down to 00000 = -34.5dB
	7	RINMUTE	1	Left Channel Line Input Mute 1 = Enable Mute 0 = Disable Mute
	8	RLINBOTH	0	Right to Left Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of RINVOL[0:4] and RINMUTE to LINVOL[0:4] and LINMUTE 0 = Disable Simultaneous Load

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000101 Digital Audio Path Control	0	ADCHPD	0	ADC High Pass Filter Enable (Digital) 1 = Disable High Pass Filter 0 = Enable High Pass Filter
	4	HPOR	0	Store dc offset when High Pass Filter disabled 1 = store offset 0 = clear offset
0000110 Power Down Control	0	LINEINPD	1	Line Input Power Down 1 = Enable Power Down 0 = Disable Power Down
	2	ADCPD	1	ADC Power Down 1 = Enable Power Down 0 = Disable Power Down
	5	OSCPD	0	Oscillator Power Down 1 = Enable Power Down 0 = Disable Power Down
	7	POWEROFF	1	POWEROFF mode 1 = Enable POWEROFF 0 = Disable POWEROFF
0000111 Digital Audio Interface Format	1:0	FORMAT[1:0]	10	Audio Data Format Select 11 = DSP Mode, frame sync + 2 data packed words 10 = I^2S Format, MSB-First left-1 justified 01 = MSB-First, left justified 00 = MSB-First, right justified
	3:2	IWL[1:0]	10	Input Audio Data Bit Length Select 11 = 32 bits 10 = 24 bits 01 = 20 bits 00 = 16 bits
	4	LRP	0	DSP mode A/B select (in DSP mode only) 1 = MSB is available on 2nd BCLK rising edge after LRC rising edge 0 = MSB is available on 1st BCLK rising edge after LRC rising edge
	6	MS	0	Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode
0001000 Sampling Control	0	USB/ NORMAL	0	Mode Select 1 = USB mode (250/272fs) 0 = Normal mode (256/384fs)
	1	BOSR	0	Base Over-Sampling Rate USB Mode: 0 = 250fs, 1 = 272fs Normal Mode: 0 = 256fs, 1 = 384fs
	5:2	SR[3:0]	0000 (fs)	ADC sample rate control; See USB Mode and Normal Mode Sample Rate sections for operation
	6	CLKIDIV2	0	Core Clock divider select 1 = Core Clock is MCLK divided by 2 0 = Core Clock is MCLK

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001001 Active Control	0	ACTIVE	0	Activate Interface 1 = Active 0 = Inactive
0001111 Reset Register	8:0	RESET	not reset	Reset Register Write 000000000 to register triggers reset

Table 20 Register Map Description

Note

1. All other bits not explicitly defined in the register table should be set to zero, unless specified otherwise (see Powerdown section).

DIGITAL FILTER CHARACTERISTICS

The ADC employs different digital filters. There are 4 types of digital filter, called Type 0, 1, 2 and 3. The performance of Types 0 and 1 is listed in the table below, the responses of all filters is shown in the proceeding pages.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter Type 0 (USB Mode, 250fs operation)					
Passband	+/- 0.05dB	0		0.416fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.584fs			
Stopband Attenuation	f > 0.584fs	-60			dB
ADC Filter Type 1 (USB mode, 272fs or Normal mode operation)					
Passband	+/- 0.05dB	0		0.4535fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-60			dB
High Pass Filter Corner Frequency	-3dB -0.5dB -0.1dB		3.7 10.4 21.6		Hz

Table 21 Digital Filter Characteristics

TERMINOLOGY

1. Stop Band Attenuation (dB) - the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

ADC FILTER RESPONSES

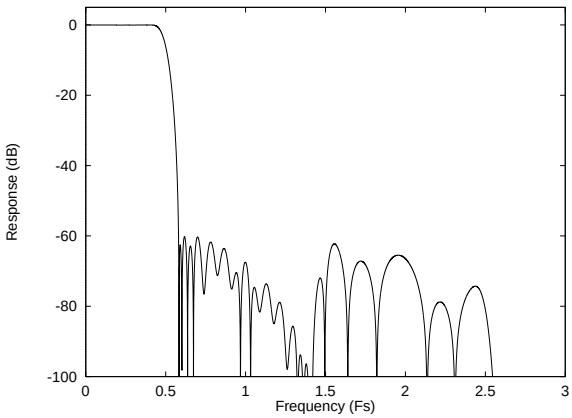


Figure 21 ADC Digital Filter Frequency Response –Type 0

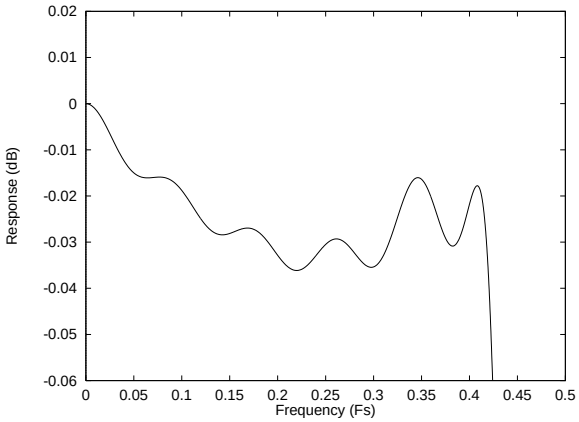


Figure 22 ADC Digital Filter Ripple –Type 0

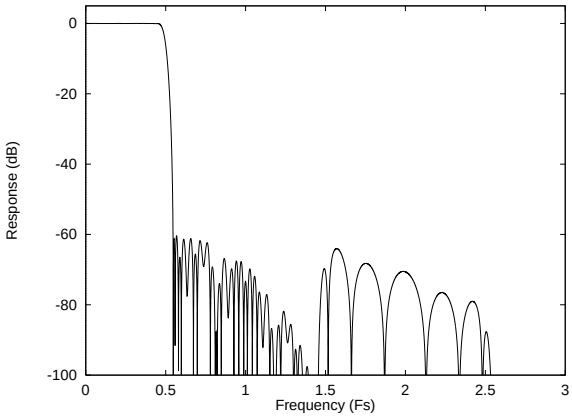


Figure 23 ADC Digital Filter Frequency Response –Type 1

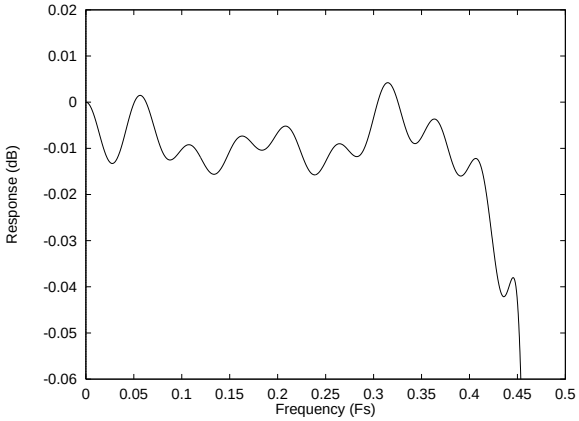


Figure 24 ADC Digital Filter Ripple –Type 1

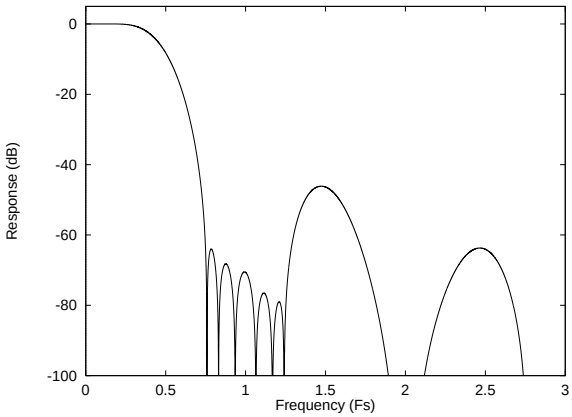


Figure 25 ADC Digital Filter Frequency Response –Type 2

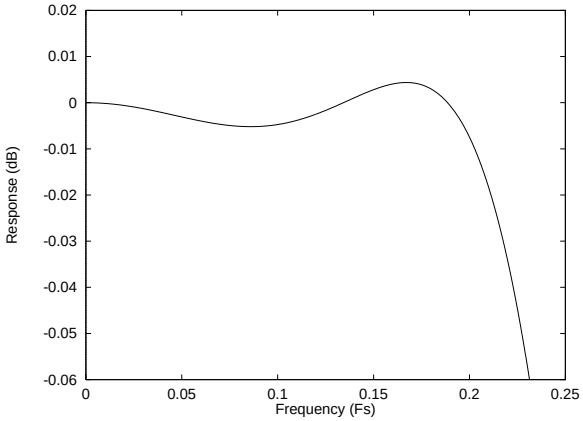


Figure 26 ADC Digital Filter Ripple –Type 2

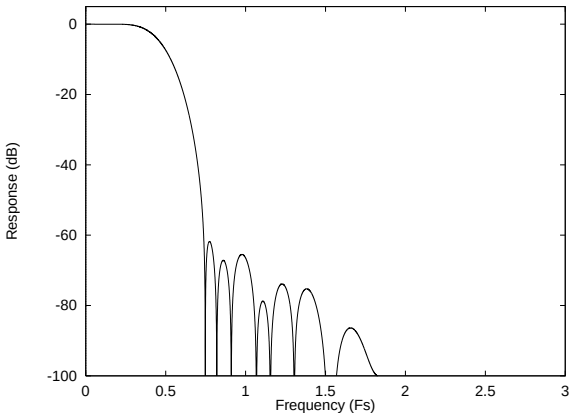


Figure 27 ADC Digital Filter Frequency Response –Type 3

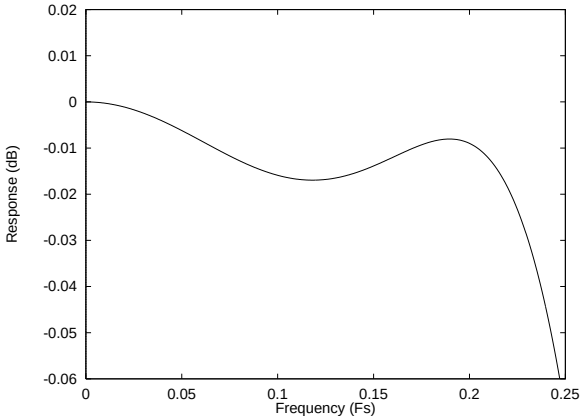


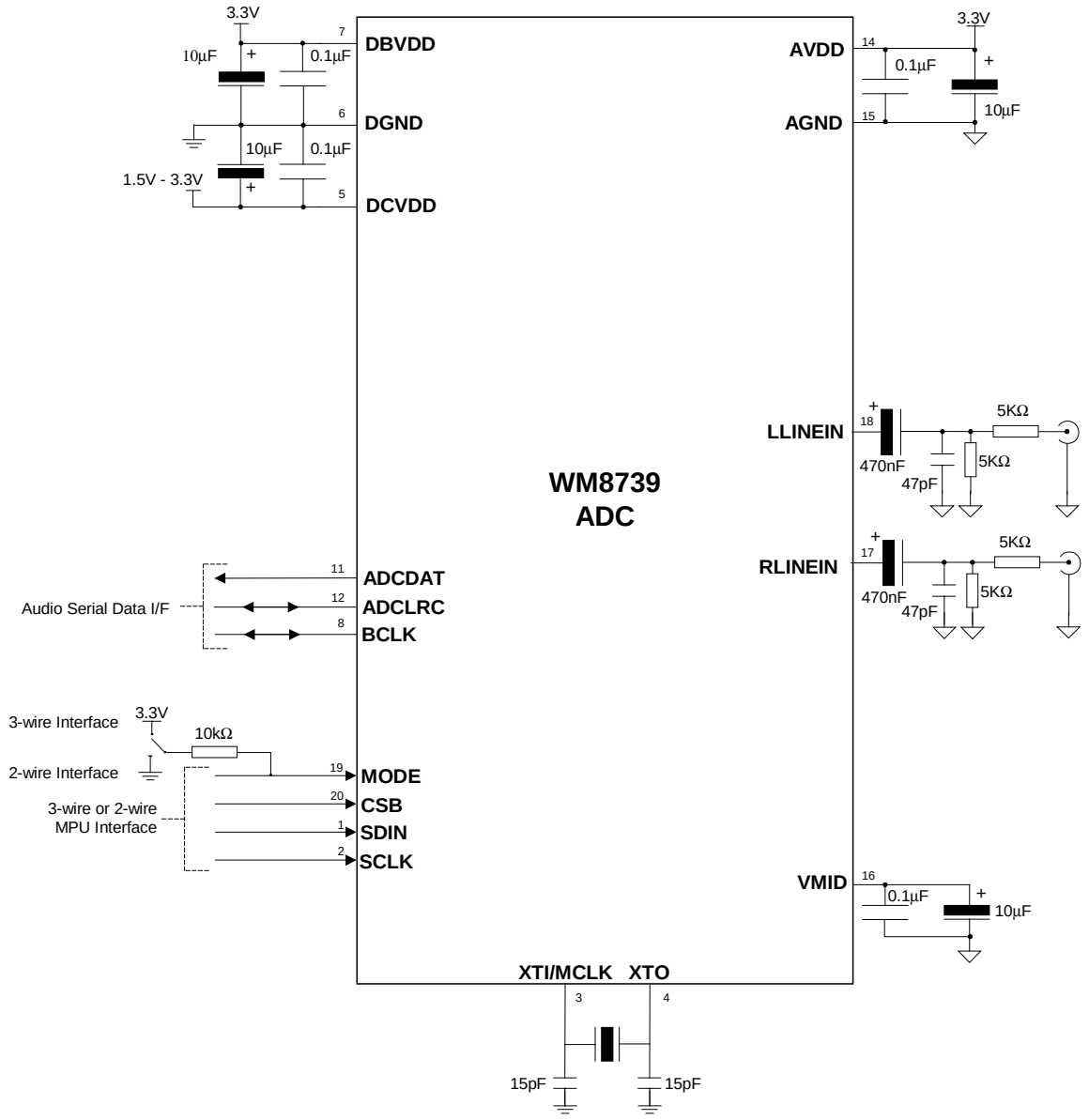
Figure 28 ADC Digital Filter Ripple –Type 3

ADC HIGH PASS FILTER

The WM8739 has a selectable digital high pass filter to remove DC offsets. The filter response is characterised by the following polynomial.

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995\, z^{-1}}$$

RECOMMENDED EXTERNAL COMPONENTS

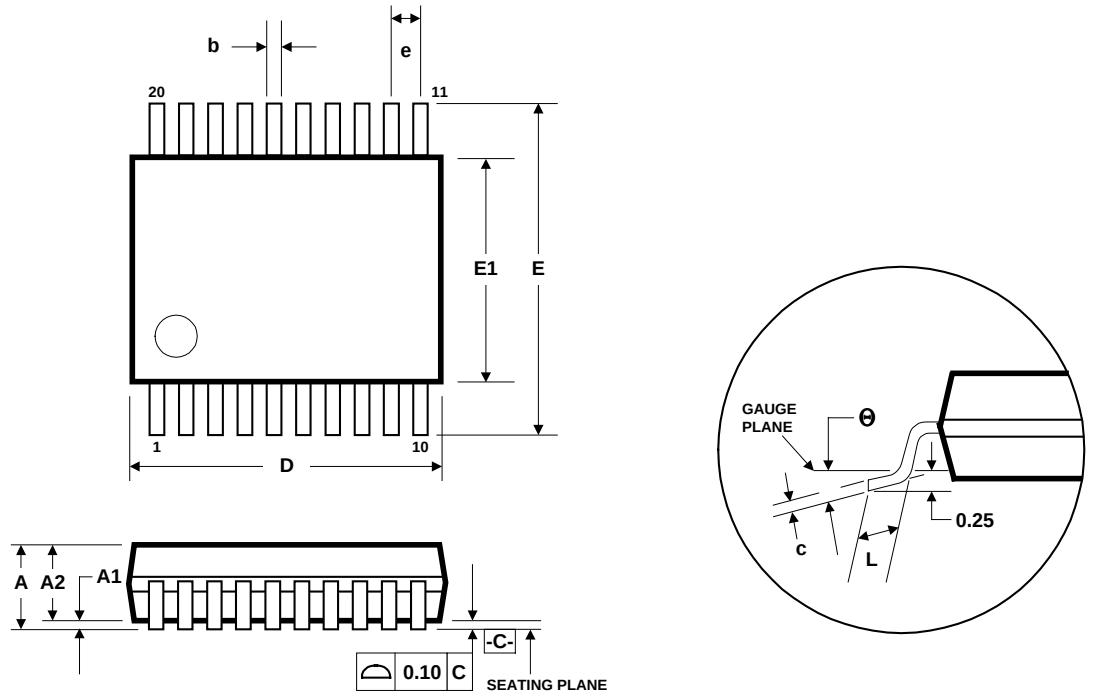


Notes:
1. AGND and DGND should be connected as close to the WM8739 as possible.
2. 0.1µF capacitors should be positioned as close the the WM8739 as possible.
3. Capacitor types should be carefully chosen. Capacitors with very low ESR are recommended for optimum performance.

Figure 29 External Components Diagram

PACKAGE DIMENSIONS (SSOP)

DS: 20 PIN SSOP (7.2 x 5.3 x 1.75 mm) **DM0015.A**

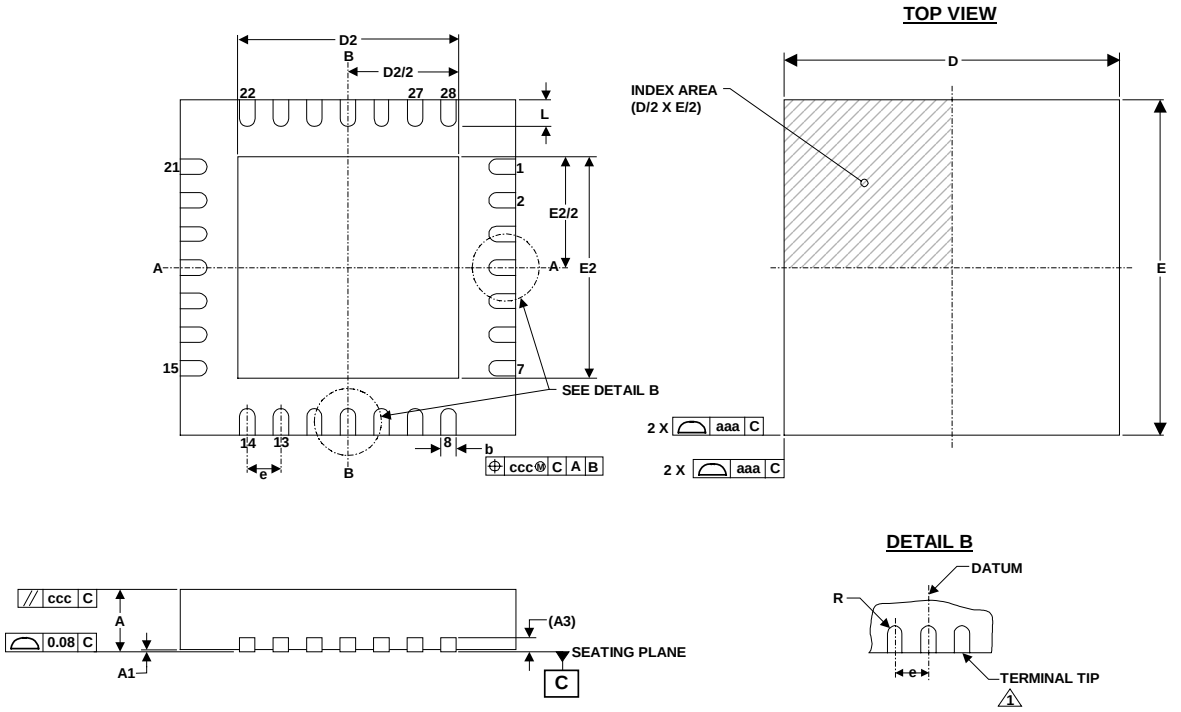


Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	-----
A_2	1.65	1.75	1.85
b	0.22	-----	0.38
c	0.09	-----	0.25
D	6.90	7.20	7.50
e	0.65 BSC		
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
θ	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

PACKAGE DIMENSIONS (QFN)

FL: 28 PIN QFN PLASTIC PACKAGE 5 X 5 X 1 mm BODY, 0.50 mm LEAD PITCH **DM023.B**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0	0.02	0.05	
A3		0.2 REF		2
b	0.18	0.23	0.30	1
D		5.00 BSC		
D2	3.2	3.3	3.4	2
E		5.00 BSC		
E2	3.2	3.3	3.4	2
e		0.5 BSC		
L	0.35	0.4	0.45	
R	b(min)/2			
Tolerances of Form and Position				
aaa		0.15		
ccc		0.10		
REF:	JEDEC.95, MO-220, VARIATION VHHD-1			

NOTES:
1. **DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.**
2. **FALLS WITHIN JEDEC.95, MO-220 WITH THE EXCEPTION OF D2, E2, A3:**
   D2,E2: LARGER PAD SIZE CHOSEN WHICH IS JUST OUTSIDE JEDEC SPECIFICATION
   A3: NOMINAL VALUE LESS THAN JEDEC
3. **ALL DIMENSIONS ARE IN MILLIMETRES**
4. **THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.**

IMPORTANT NOTICE

Wolfson Microelectronics Ltd (WM) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current. All products are sold subject to the WM terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

WM warrants performance of its products to the specifications applicable at the time of sale in accordance with WM's standard warranty. Testing and other quality control techniques are utilised to the extent WM deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

In order to minimise risks associated with customer applications, adequate design and operating safeguards must be used by the customer to minimise inherent or procedural hazards.

WM assumes no liability for applications assistance or customer product design. WM does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of WM covering or relating to any combination, machine, or process in which such products or services might be or are used. WM's publication of information regarding any third party's products or services does not constitute WM's approval, license, warranty or endorsement thereof.

Reproduction of information from the WM web site or datasheets is permissable only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated WM product or service, is an unfair and deceptive business practice, and WM is not responsible nor liable for any such use.

Resale of WM's products or services with statements different from or beyond the parameters stated by WM for that product or service voids all express and any implied warranties for the associated WM product or service, is an unfair and deceptive business practice, and WM is not responsible nor liable for any such use.

ADDRESS:

Wolfson Microelectronics Ltd

20 Bernard Terrace

Edinburgh

EH8 9NX

United Kingdom

Tel :: +44 (0)131 667 9386

Fax :: +44 (0)131 667 5176

Email :: sales@wolfsonmicro.com