YAMAHA LSI

YTD439

ISTU

ISDN BRI controller for Terminal Equipment with built-in DSU

❑ *Abstract*

YTD439 is a LSI that integrates in a single chip all the communication functions that are necessary for constructing an ISDN terminal with a built-in DSU. The functions of both the DSU (U reference point) and terminal (S/T reference point) are packed into the 100-pin SQFP chip allowing miniaturization of the terminal equipment.

YTD439 has a built-in TD switch function that is necessary for controlling the connection of the B-channel data. By connecting an external CPU, memory, and CODEC, a terminal with a built-in DSU can be configured. In addition, YTD439 has a function that reduces the power consumption by stopping the functions of unused blocks. This is effective for battery-driven terminals.

❍ *Features*

DSU block

- Conforms to TTC Standards JT-I430 and JT-G961.
- LT (line termination) function and CT (circuit termination) function.
- DSU can be disconnected.

S/T reference point driver/receiver block

- Transition to the sleep state possible by setting an I/O register.

CPU interface block

- 8-bit or 16-bit data bus selectable.
- I/O access through registers.

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YTD439 CATALOG
CATALOG No.:4TD439A2
2001.1

Layer 1 control block

- Frame assembling and disassembling function.
- I430 TTL output pin

Layer 2 control block

- Built-in LAPD protocol (supports four links).
- Call control and D-channel packet function.

Layer 3 interface block

- Message exchange through I/O access (large 1088-byte FIFO).

B channel HDLC controller

- Supports CRC-CCITT and CRC-32.
- 128k/64k/56k rate adaption

B channel transparent

- Supports PIAFS 64k/32k.
- Flexible rate adaption function.

B channel DATA FIFO

- Transmission and reception: 128-byte FIFO × 2 channels.

TD switch

- Switch circuit for 8 channels of B channel data.
- 512 k to 2,048 kHz PCM highway.

Others

- Terminal block can be disconnected. Power can be cut off.
- Terminal block sleep mode.
- Power supply to the analog block: +5 V.
  Power supply to the digital block: +5 V or 3.3 V.
- 5 V tolerant I/O pin
- 100-pin SQFP.

❍ *Applications*

- Terminal adapter
- Remote router
- ISDN telephone
- ISDN home telephone
- ISDN Facsimile

❍ *Functional Comparison of YAMAHA ISDN LSIs*

Function			YTD421	YTD428	YTD423	YTD436	YTD439
DSU Function	TTC Standard	JT-G961		1997 edition			1997 edition
Layer 1	TTC Standard	JT-I430	1993 edition	1993 edition	1993 edition	1997 edition	1997 edition
Layer 2	TTC Standard	JT-Q920 JT-Q921			1993 edition	1993 edition 1998 edition	1993 edition 1998 edition
ETSI ETS 300 012, ETS 300 125					√	√	
North American Switches National ISDN-1/2, AT&T 5ESS, Nortel DMS-100					√	√	
S/T Ref. Point Analog Driver/Receiver			√	√	External [YTD421]	√	√
Maximum D Channel Links	Circuit switching				2	2	2
	Dch Packet Switching (Teleaction communication)				2	2 (2)	2 (2)
D Channel Layer 3 Data Transfer Method					DMA Transfer or I/O Transfer	DMA Transfer or I/O Transfer	I/O Transfer
HDLC Controller for B Channel Data					√	External	√
B Channel Data Transfer Method					DMA Transfer or I/O Transfer	DMA Transfer or I/O Transfer (**Note 1**)	I/O Transfer
B Channel Internal Clock Mode (kHz)					32, 56, 64	32, 56, 64	
B Channel External Clock Mode					√	√	√
TD Switch							√
Clock Output Function for CPU					√	√	√
Signal Output Function for Testing					√	√	√
Power Supply (V)			+5 or +3.3 (**Note 2**)	+5	+5	+5 or +3.3 (**Note 2**)	+5 or +3.3 (**Note 2**)
5-V Tolerant I/O pin							√
Package			20-pin SSOP	100-pin SQFP	100-pin SQFP	100-pin SQFP	100-pin SQFP

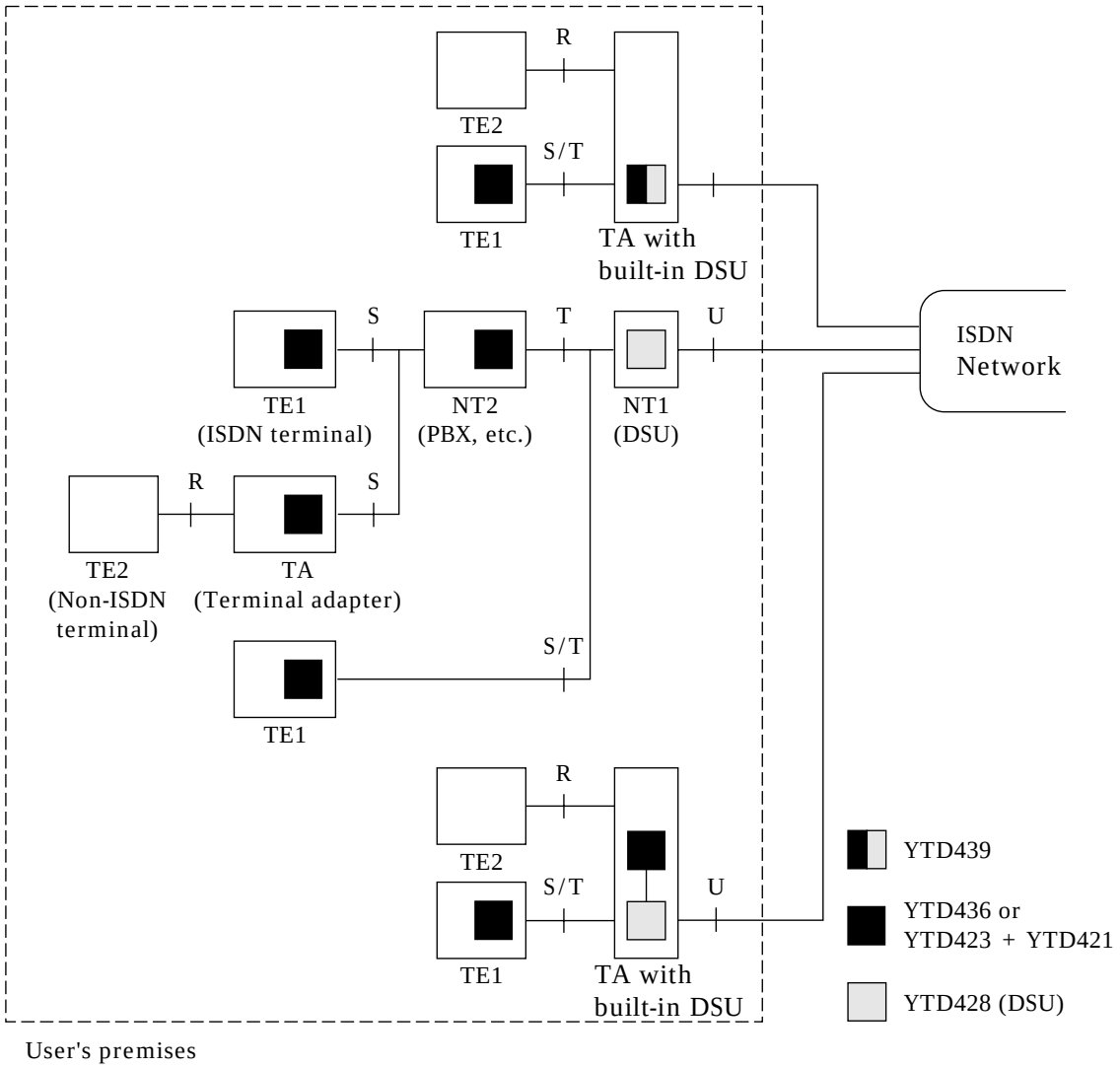
Note 1: DMA transfer: Request function only
I/O transfer: 4-byte FIFO
Note 2: Digital power supply only

❑ Block Diagram

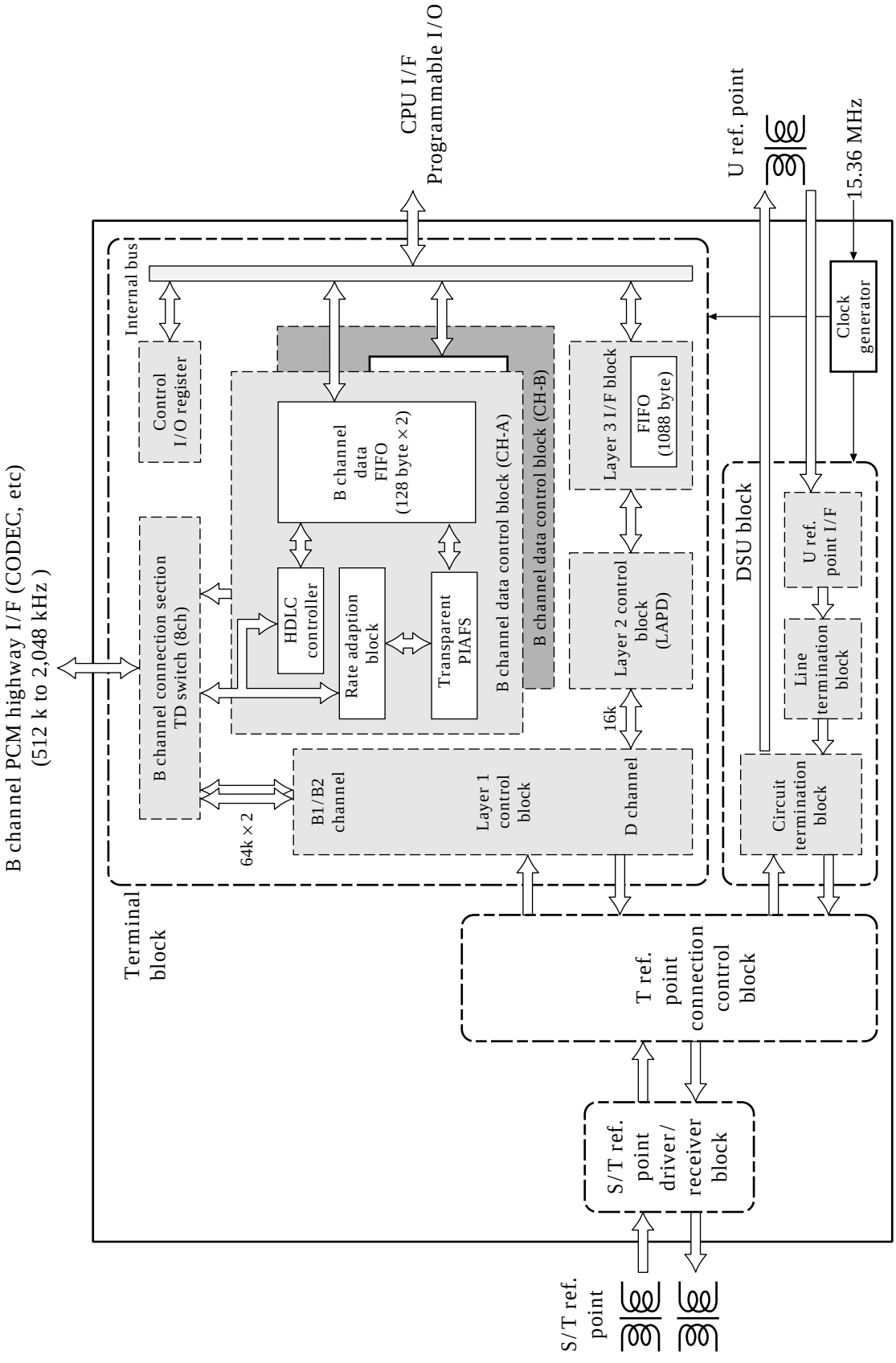
❍ User-Network Interface Block Diagram

YTD439 is best-suited for applications in terminal equipment with built-in DSU (TA, TE1) such as terminal adapters and remote routers with built-in DSUs.

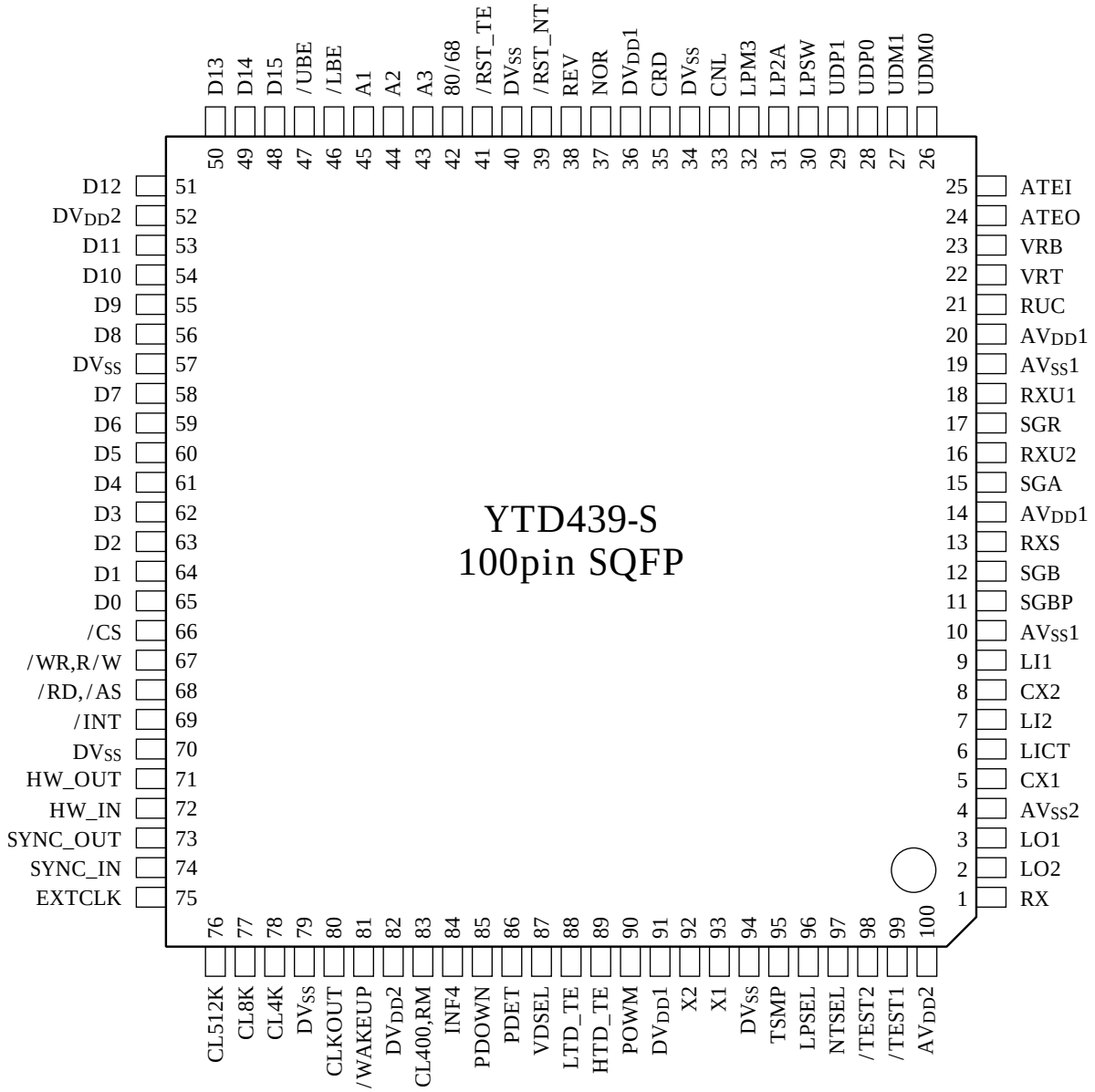
YTD439 contains a DSU function, which is necessary between the ISDN switch and the user-network interface, and layer 1 and layer 2 functions, which are required of ISDN system equipment. By adding minimal peripheral parts such as microprocessor and CODEC, terminal equipment can be optimally configured.



❍ *Internal Block Diagram*



❑ *Pin Assignments*



❑ Overview of Functions

❍ DSU Block

The DSU section achieves DSU functions of subscriber line interface (two-wire time compression multiplexing operation) and the user-network interface (digital four-wire time division full-duplex operation) for ISDN. The electrical characteristics conforming to TTC Standard JT-G961 is achieved.

Line Termination Block (LT Block)

The line termination section provides the $\sqrt{f}$ equalization that compensates for the line loss and amplitude distortion and the bridged tap equalization that compensates for signal distortion.

Circuit Termination Block (CT Block)

The circuit termination provides the following functions:

- U/T reference point rate adaption and frame assembling and disassembling
- State transition control
- U reference point driver circuit control
- T reference point reception timing control
- Loopback control (loopback 2 and loopback C for maintenance and testing)

❍ S/T Reference Point Driver/Receiver Block

By connecting S/T reference point transformers, the electrical characteristics conforming to TTC Standard JT-I430 is achieved. YTD439 normally operates in the DSU mode. However, if the DSU function is disconnected, YTD439 switches to the terminal mode and operates as a S/T reference point terminal LSI.

❍ T Reference Point Connection Control Block

When the DSU block is disconnected or when the driver/receiver functions are disabled, the input/output signal of JT-I430 is switched within this control block. In addition, when disconnecting the power to the terminal block or the S/T reference point driver/receiver block, this block disconnects the signal between the DSU block and the block that is disabled.

❍ Terminal Block

Layer 1 control block

The Layer 1 control block provides the Layer 1 functions conforming to JT-I430.
It automatically controls the Layer 1 state according to (1) the phantom power detection from the network, (2) the instruction from the host processor and (3) the transaction of INFO signals and notifies the state change to the host processor. The priority/collision control block monitors the collision conditions and puts priority on D channel data access so that each terminal can access the data fairly.

Layer 2 control block

The Layer 2 control block provides the Layer 2 functions (LAP-D protocol) conforming to JT-Q920 and JT-Q921.
YTD439 can establish total of four data links, two data links for circuit switching and two data links for D channel packet switching/teleaction communications. It supports the LAP-D frame assembly and disassembly, the SAPI and TEI address control, the LAP-D sequence control and flow control for each data link. More specifically, when the YTD439 accepts the data link establishment request from the host processor (Layer 3) in order to initiate a call or accept an incoming call, the YTD439 activates Layer 1, initiates the TEI assignment procedure (if necessary), and establishes the data link, thereby enabling the exchange of layer 3 messages. Later, the YTD439 releases the data link according to the data link release request from the host processor or the network.
Since both automatic and non-automatic TEI assignment are supported, VC/PVC can be implemented for packet switching.

Layer 3 Interface Block

The interface between Layer 2 (YTD439) and Layer 3 (host processor) is a logic interface supporting primitives. The command/status primitives consisting of data up to 8 bytes are exchanged by writing to or reading from the YTD439 I/O registers to control the data link.
I frames or UI frames containing Layer 3 messages are transferred using I/O transfer through the large dedicated FIFO.

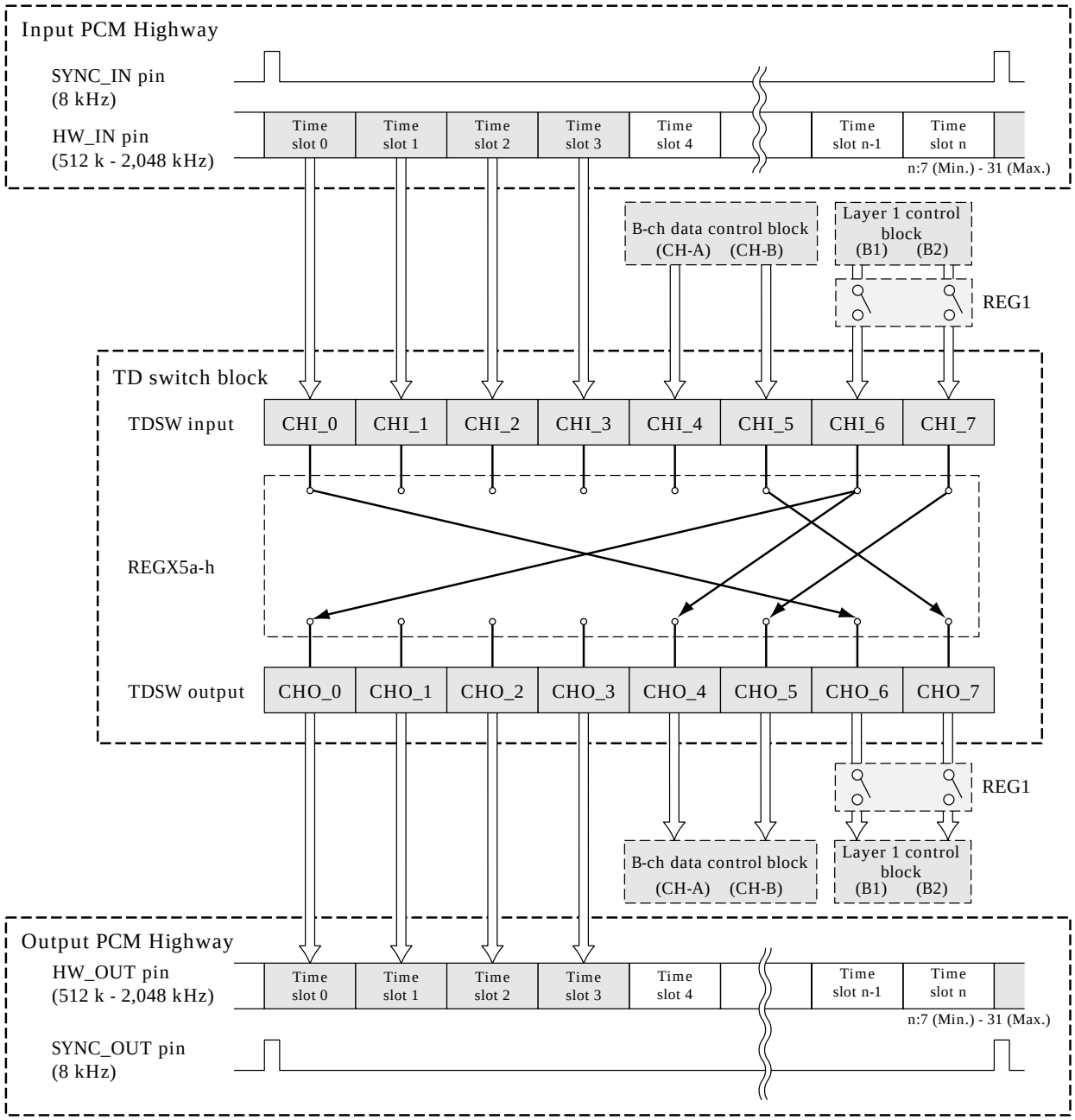
B Channel Data Control Block

The B channel data control block consists of two control blocks with the same functionality for CH-A and CH-B to support the two B channels, B1 and B2. Each B channel data control block has a HDLC controller block and a transparent block, and the B channel data FIFO connects to one of the blocks.
You can select the speeds of 128 k, 64 k, or 56 kHz for the HDLC controller block. The HDLC block supports CRC-CCITT, CRC-32, and no CRC. By activating the HDLC controller block, protocols such as PPP is also supported.
The transparent block carries out serial-to-parallel conversion on the B channel data and expands the data in the FIFO. This allows the host processor to check the B channel data that is received from the line. It also allows transmission of DTMF signals, voice messages, and other signals to the line by the host processor writing parallel data to the FIFO. This block also has a flexible rate adaption function that allows the use of protocols such as V110.
In addition, the transparent block also supports PIAFS64k and PIAFS32k. By following the commands from the host processor, this block carries out necessary tasks for PIAFS such as I460 rate adaption, SYNC pattern detection, automatic bit adjustment of 8-bit boundaries.

TD Switch Block

The TD switch block consists of the time-division switch. It allows the replacement of data of each channel on the PCM highway. By using the TD switch, the switch control of B channel data can be facilitated on terminals with multi-functionality such as extensions, three-way calls, and holding tone.

YTD439 supports 512 kHz to 2,048 kHz PCM highway and can perform switching on 8 channels. You can specify which output channels to connect the 8 channels of input through the I/O register. One-to-one connection and one-to-multi-point connections are supported.
The B channel data control block and the layer 1 control block (B channel data) are connected to the PCM highway internally in the YTD439, and two channels are used by each. The remaining four channels are connected to the PCM highway pins and allows connection to arbitrary channels such as an external CODEC.



The data path in the TD Switch Block diagram is set assuming the following application example.

Voice call and voice monitor using the B1 channel

B1 channel (downward)	→	Output PCM highway time slot 0	: CHI_6 → CHO_0
	→	B channel data control block (CH-A)	: CHI_6 → CHO_4
B1 channel (upward)	←	Input PCM highway time slot 0	: CHO_6 ← CHI_0

Data communication using the B2 channel

B2 channel (downward)	→	B channel data control block (CH-B)	: CHI_7 → CHO_5
B2 channel (upward)	←	B channel data control block (CH-B)	: CHO_7 ← CHI_5

❑ Electrical Characteristics

❍ Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply voltage	$AV_{DD}1$	- 0.3	6.0	V
	$AV_{DD}2$	- 0.3	6.0	V
	$DV_{DD}1$	- 0.3	5.7	V
	$DV_{DD}2$	- 0.3	5.7	V
Input voltage	$AV_{IN}1$	- 0.3	$AV_{DD}1$ + 0.3	V
	$AV_{IN}2$	- 0.3	$AV_{DD}2$ + 0.3	V
	$DV_{IN}1$	- 0.3	5.75	V
	$DV_{IN}2$	- 0.3	5.75	V
Storage temperature	T_{stg}	- 50	125	°C

(Based on $AV_{SS}1$ = $AV_{SS}2$ = DV_{SS} = 0.0 V)

❍ Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Max.	Unit
Supply voltage	$AV_{DD}1$		4.75	5.25	V
	$AV_{DD}2$		4.75	5.25	V
	$DV_{DD}1$	**Note**	3.0	3.6	V
		Note	4.75	5.25	V
	$DV_{DD}2$	VDSEL = "H"	4.75	5.25	V
	$DV_{DD}2$	VDSEL = "L"	3.0	3.6	V
Operating Temperature	T_{op}		0	70	°C

(Based on $AV_{SS}1$ = $AV_{SS}2$ = DV_{SS} = 0.0 V)

Note: Select either a 5 V system or a 3.3 V system.

❍ DC Characteristics

U Reference Point Receiver (AVDD1= 5.0 V, Top = 25 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Allowable load impedance at output	Z_O	**Note 1**	30			kΩ
Receive buffer input impedance	Z_{i1}	**Note 2**	10			MΩ
Analog signal reference voltage	V_{SG}	**Note 3**	2.45	2.50	2.55	V
ADC self-bias	V_{RT}	**Note 4**	0.7AV_{DD1} - 0.1	0.7AV_{DD1}	0.7AV_{DD1} + 0.1	V
	V_{RB}	**Note 5**	0.3AV_{DD1} - 0.1	0.3AV_{DD1}	0.3AV_{DD1} + 0.1	V

Note 1: Applies to the SGR pin.

Note 2: Applies to the RXU1 and RXU2 pins.

Note 3: Applies to the SGR pin (open).

Note 4: Applies to the VRT pin.

Note 5: Applies to the VRB pin.

DSU Digital Block (DVDD1 = 3.3 ± 0.3 V or 5 V ± 5%, Top = 0 to 70 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH}	**Note 1**	0.8DV_{DD1}			V
		Note 2	0.9DV_{DD1}			V
Low-level input voltage	V_{IL}	**Note 1**			0.2DV_{DD1}	V
		Note 2			0.1DV_{DD1}	V
High-level output voltage	V_{OH}	**Note 3**	DV_{DD1} - 0.4			V
		Note 4	AV_{DD1} - 0.4			V
Low-level output voltage	V_{OL}	**Note 3**			0.4	V
		Note 4			0.4	V
Leakage current	I_L		- 10		10	µA
Off-state leak current	I_{LZ}		- 10		10	µA

Note 1: Applies to NOR, REV, /RST_NT, POWM, TSMP, LPSEL, NTSEL, /TEST1, /TEST2 pins.

Note 2: Applies to the X1 pin.

Note 3: Applies to LPSW, LP2A, LPM3, CNL, and CRD pins.

Condition: I_{OH} = - 0.4 mA, I_{OL} = 1.2 mA

Note 4: Applies to UDM0, UDM1, UDP0, and UDP1 pins.

Condition: AV_{DD1} = 4.75 to 5.25 V, Top = 25 °C, I_{OH} = - 0.4 mA, and I_{OL} = 1.2 mA

Terminal Digital Block

a. When DVDD2 = 5 V ± 5% (VDSEL pin = "H" and Top = 0 to 70 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level TTL input	V_{IH}	**Note 1**	2.2			V
Low-level TTL input	V_{IL}	**Note 1**			0.8	V
High-level CMOS input	V_{IH}	**Note 2**	0.8$DV_{DD}2$			V
Low-level CMOS input	V_{IL}	**Note 2**			0.2$DV_{DD}2$	V
High-level output	V_{OH}	**Note 3**	2.7			V
Low-level output	V_{OL}	**Note 3**			0.4	V
Open drain output	V_{OL}	**Note 4**			0.4	V
Leakage current	I_L		- 10		10	µA
Off-state leakage current	I_{LZ}	**Note 5**	- 10		10	µA

Note 1: Applies to EXTCLK, SYNC_IN, SYNC_OUT, HW_IN, /RD, /WR, /CS, D15 to D0, /UBE, /LBE, A3 to A1 pins.

Note 2: Applies to /RST_TE, 80/68, /WAKEUP, PDET, and VDSEL pins.

Note 3: I_{OH} = -0.4 mA, I_{OL} = 1.2 mA

Note 4: When HW_OUT pin is set to open drain. Condition: R_L = 500 Ω

Note 5: When pins D15 to D0 are in the input condition (when word access (16 bits) is specified) and when pins D7 to D0 are in the input condition (before issuing the **SYSTEM–CONFIGURATION–REQUEST** command or when byte access is (8 bits) is specified).

b. When DVDD2 = 3.3 V ± 0.3 V (VDSEL pin = "L", Top = 0 to 70 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level input	V_{IH}	**Note 1**	0.8$DV_{DD}2$			V
Low-level input	V_{IL}	**Note 1**			0.2$DV_{DD}2$	V
High-level output	V_{OH}	**Note 2**	$DV_{DD}2$- 0.4			V
Low-level output	V_{OL}	**Note 2**			0.4	V
Open drain output	V_{OL}	**Note 3**			0.4	V
Leakage current	I_L		- 10		10	µA
Off-state leakage current	I_{LZ}	**Note 4**	- 10		10	µA

Note 1: Applies to EXTCLK, SYNC_IN, SYNC_OUT, HW_IN, /RD, /WR, /CS, D15 to D0, /UBE, /LBE, A3 to A1, /RST_TE, 80/68, /WAKEUP, PDET, and VDSEL pins.

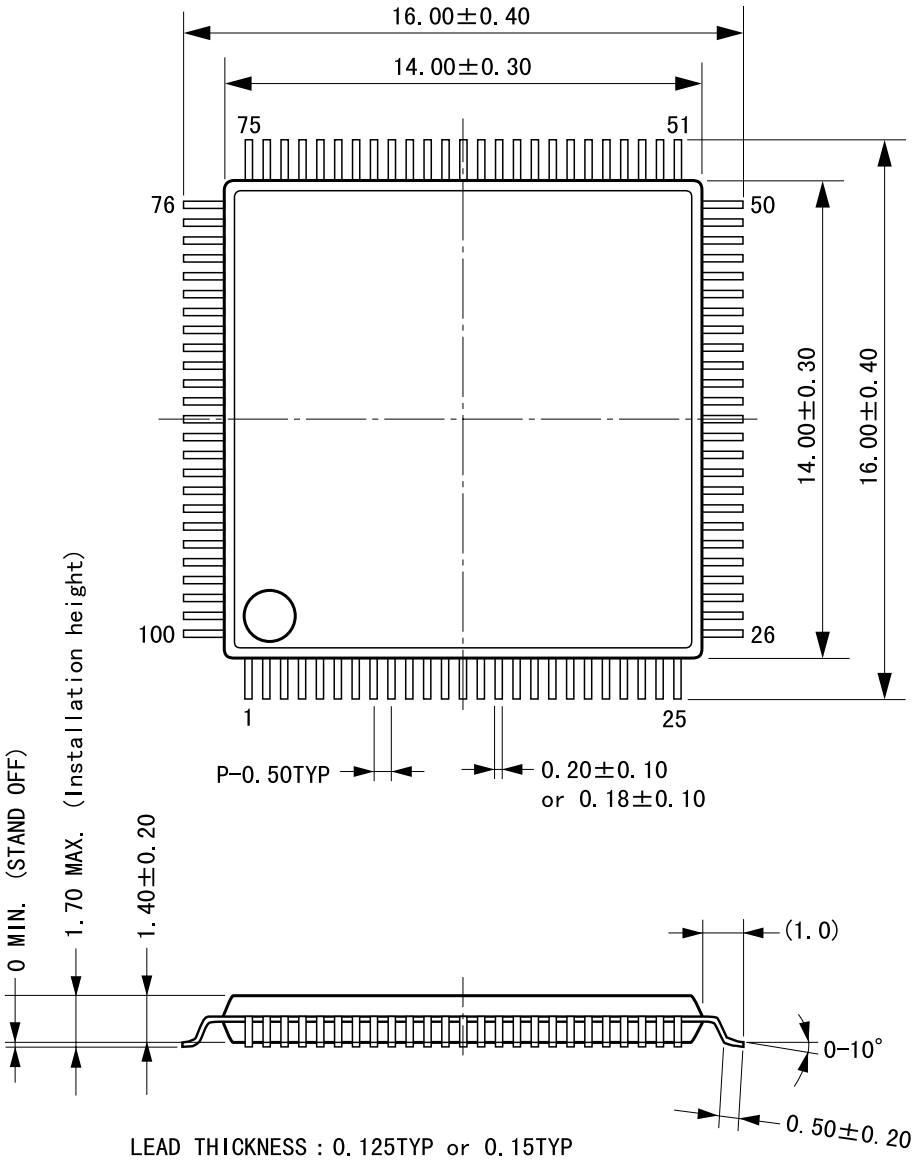
Note 2: I_{OH} = -0.4 mA, I_{OL} = 1.2 mA

Note 3: When HW_OUT pin is set to open drain. Condition: R_L = 500 Ω

Note 4: When pins D15 to D0 are in the input condition (when word access (16 bits) is specified) and when pins D7 to D0 are in the input condition (before issuing the **SYSTEM–CONFIGURATION–REQUEST** command or when byte access is (8 bits) is specified).

❑ *Package Outline*

C-PK100SP-1



(UNIT) : mm (millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

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