FAIRCHILD

SEMICONDUCTOR ™

74VHCT00A
Quad 2-Input NAND Gate

General Description

The VHCT00A is an advanced high-speed CMOS 2-Input NAND Gate fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages, including buffer output, which provide high noise immunity and stable output.

Protection circuits ensure that 0V to 7V can be applied to the input pins without regard to the supply voltage and to the output pins with V_{CC} = 0V. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 3V to 5V systems and two supply systems such as battery backup.

Features

- High speed: t_{PD} = 5.0 ns (typ) at T_A = 25°C
- High noise immunity: V_{IH} = 2.0V, V_{IL} = 0.8V
- Power down protection is provided on all inputs and outputs
- Low noise: V_{OLP} = 0.8V (max)
- Low power dissipation:
  I_{CC} = 2 μA (max) at T_A = 25°C
- Pin and function compatible with 74HCT00

Ordering Code:

Order Number	Package Number	Package Description
74VHCT00AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74VHCT00ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHCT00AMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHCT00AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol
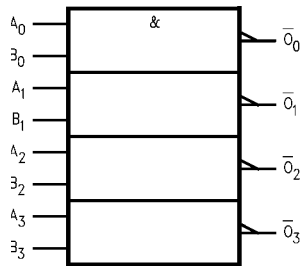
Connection Diagram
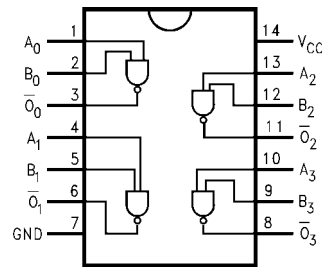
Pin Descriptions

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

Truth Table

A	B	$\overline{O}$
L	L	H
L	H	H
H	L	H
H	H	L

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74VHCT00A

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	
(Note 2)	−0.5V to V_{CC} + 0.5V
(Note 3)	−0.5V to 7.0V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	
(Note 4)	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 5)

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	
(Note 2)	0V to V_{CC}
(Note 3)	0V to 5.5V
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
$V_{CC} = 5.0V \pm 0.5V$	0 ns/V ~ 20 ns/V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: HIGH or LOW state. I_{OUT} absolute maximum rating must be observed.

Note 3: V_{CC} = 0V.

Note 4: V_{OUT} < GND, V_{OUT} > V_{CC} (Outputs Active)

Note 5: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	4.5	2.0			2.0		V		
		5.5	2.0			2.0				
V_{IL}	LOW Level Input Voltage	4.5			0.8		0.8	V		
		5.5			0.8		0.8			
V_{OH}	HIGH Level Output Voltage	4.5	4.40	4.50		4.40		V	$V_{IN} = V_{IH}$	$I_{OH} = -50$ μA
		4.5	3.94			3.80		V	or V_{IL}	$I_{OH} = -8$ mA
V_{OL}	LOW Level Output Voltage	4.5		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$	$I_{OL} = 50$ μA
		4.5			0.36		0.44	V	or V_{IL}	$I_{OL} = 8$ mA
I_{IN}	Input Leakage Current	0 – 5.5			±0.1		±1.0	μA	$V_{IN} = 5.5V$ or GND	
I_{CC}	Quiescent Supply Current	5.5			2.0		20.0	μA	$V_{IN} = V_{CC}$ or GND	
I_{CCT}	Maximum I_{CC}/ Input	5.5			1.35		1.50	mA	$V_{IN} = 3.4V$ Other Inputs = V_{CC} or GND	
I_{OFF}	Output Leakage Current (Power Down State)	0.0			0.5		5.0	μA	$V_{OUT} = 5.5V$	

Noise Characteristics

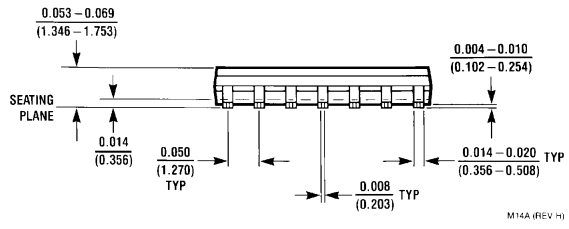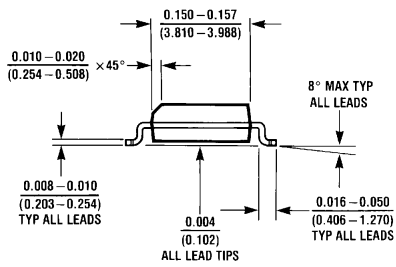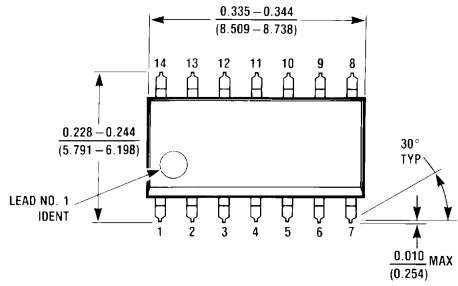| Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$		Units	Conditions
			Typ	Limit		
V_{OLP} (Note 6)	Quiet Output Maximum Dynamic V_{OL}	5.0	0.4	0.8	V	$C_L = 50$ pF
V_{OLV} (Note 6)	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.4	−0.8	V	$C_L = 50$ pF
V_{IHD} (Note 6)	Minimum HIGH Level Dynamic Input Voltage	5.0		2.0	V	$C_L = 50$ pF
V_{ILD} (Note 6)	Maximum LOW Level Dynamic Input Voltage	5.0		0.8	V	$C_L = 50$ pF

Note 6: Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0 ± 0.5		5.0	6.9	1.0	8.0	ns	$C_L = 15$ pF
t_{PHL}				5.5	7.9	1.0	9.0		$C_L = 50$ pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			17				pF	(Note 7)

Note 7: C_{PD} is defined as the value of the internal equivalent capacitance, which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr.) = $C_{PD} * V_{CC} * f_{IN} + I_{CC}/4$ (per gate)

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Physical Dimensions inches (millimeters) unless otherwise noted

0.335 − 0.344
(8.509 − 8.738)

14 13 12 11 10 9 8

0.228 − 0.244
(5.791 − 6.198)

LEAD NO. 1
IDENT

30°
TYP

1 2 3 4 5 6 7

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203)
TYP

0.014 − 0.020
(0.356 − 0.508) TYP

M14A (REV H)

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

14   8

0.295 − 0.319
(7.5 − 8.1)

0.205 − 0.213
(5.2 − 5.4)

1   7

0.394 − 0.402
(10.0 − 10.2)

(0.71)
(1.8)

0.067 − 0.083
(1.7 − 2.1)

0.006 − 0.010
(0.15 − 0.25) TYP

0° − 8° TYP

0.006 (0.15)

SEATING PLANE

0.050 TYP
(1.27)

0.000 − 0.010
(0 − 0.25)

0.014 − 0.020
(0.35 − 0.50) TYP

(0.049 TYP)
(1.25)

0.016 − 0.031
(0.4 − 0.8) TYP

M14D (REV B)
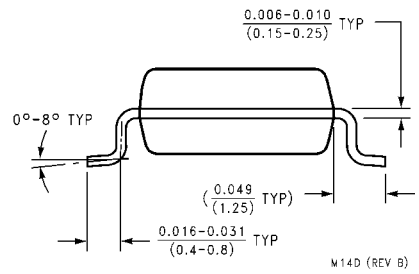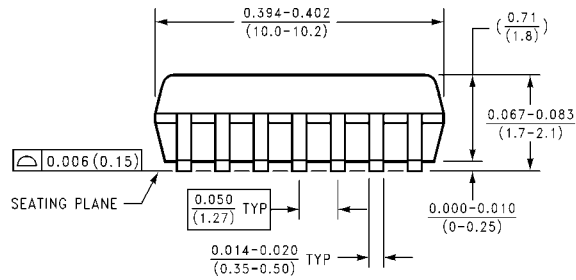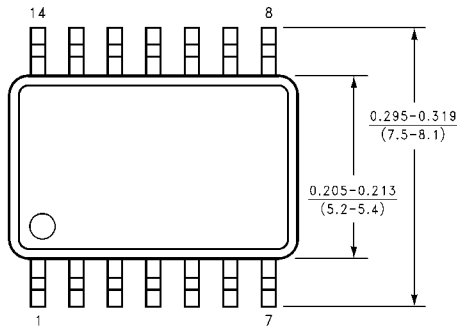
14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

74VHCT00A

5.0±0.1
-A-
0.43 TYP
14   8
6.4
3.2   4.4±0.1
-B-
1   7
PIN #1 IDENT.

0.2 C B A
ALL LEAD TIPS

7.72
4.16
1.78
0.65   0.42
LAND PATTERN RECOMMENDATION

ALL LEAD TIPS
0.1 C
1.2 MAX
-C-
0.65
0.19 - 0.30
0.13 M A B S C S

0.90 +0.15 -0.10
0.10±0.05

SEE DETAIL A
0.09-0.20

12.00° TOP & BOTTOM
R0.16
R0.31
0°-8°
0.6±0.1
1.00
DETAIL A
GAGE PLANE
0.25
SEATING PLANE
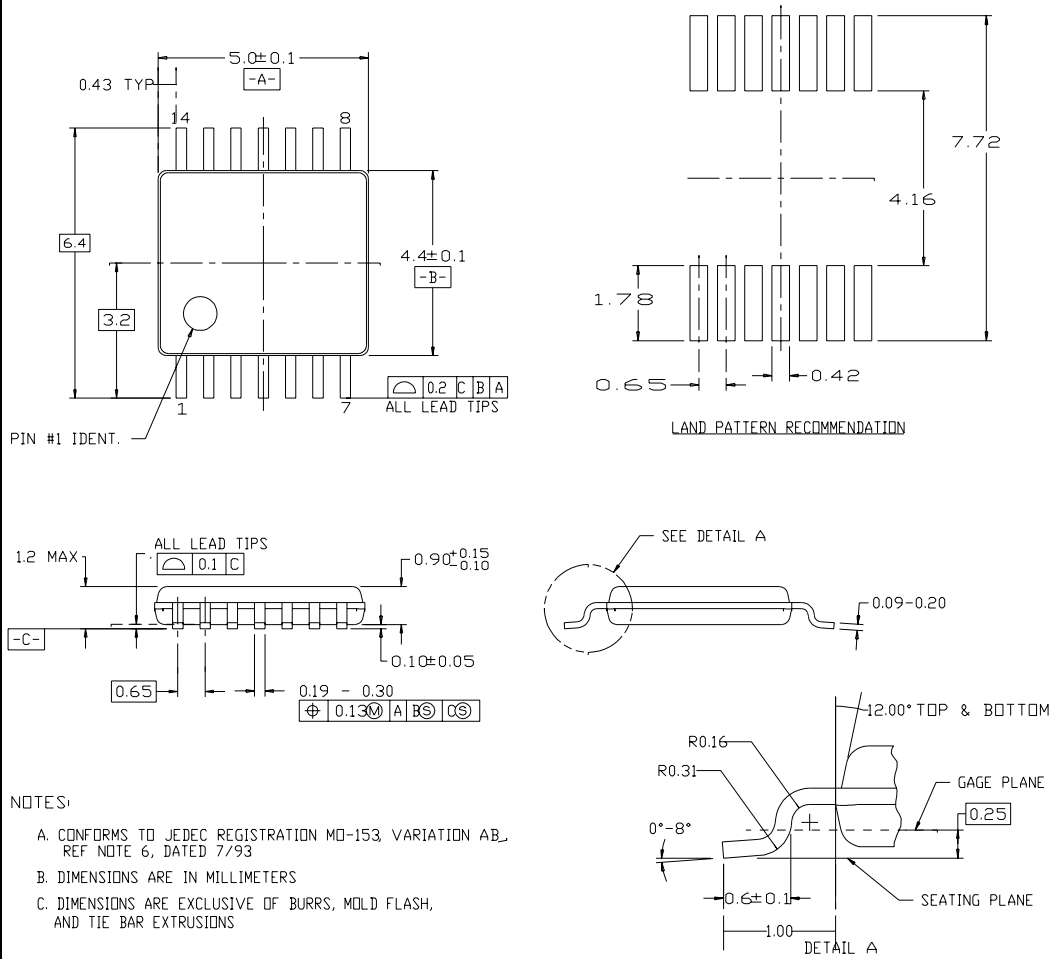
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.740 — 0.770
(18.80 — 19.56)

0.090
(2.286)

14 13 12 11 10 9 8

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1
IDENT

1 2 3 4 5 6 7

0.092 DIA   0.030 MAX
(2.337)   (0.762) DEPTH

OPTION 1

INDEX
AREA

14 13 12

PIN NO. 1
IDENT

1 2 3

OPTION 02

0.135 ± 0.005
(3.429 ± 0.127)

0.145 — 0.200
(3.683 — 5.080)

0.060 TYP
(1.524)

4° TYP
OPTIONAL

0.020
(0.508)
MIN

0.125 — 0.150
(3.175 — 3.810)

90° ± 4° TYP

0.075 ± 0.015
(1.905 ± 0.381)

0.014 — 0.023 TYP
(0.356 — 0.584)

0.100 ± 0.010 TYP
(2.540 ± 0.254)

0.050 ± 0.010 TYP
(1.270 — 0.254)

0.300 — 0.320
(7.620 — 8.128)

0.065
(1.651)

95° ± 5°

0.008 — 0.016 TYP
(0.203 — 0.406)

0.280
(7.112)
MIN

0.325 +0.040 −0.015

(8.255 +1.016 −0.381)

N14A (REV F)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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