Features

- Pulse-width Modulation up to 2 kHz Clock Frequency
- Protection against Short-circuit, Load-dump Overvoltage and Reverse V_S
- Duty-cycle 0 to 100% Continuously
- Output Stage for Power MOSFET
- Interference and Damage Protection According to VDE 0839 and ISO/TR 7637/1
- Charge-pump Noise Suppressed
- Ground-wire Breakage Protection

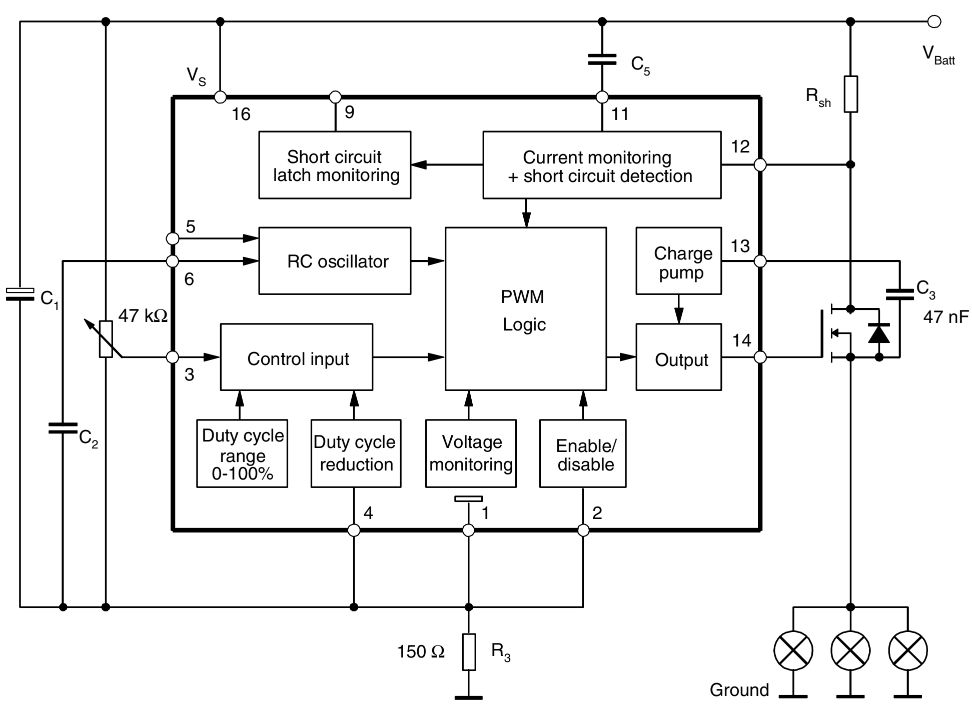
PWM Power Control with Automatic Duty-cycle Reduction

U6084B

Description

The U6084B is a PWM-IC with bipolar technology designed for the control of an N-channel power MOSFET used as a high-side switch. The IC is ideal for use in the brightness control (dimming) of lamps such as in dashboard applications. For constant brightness, the preselected duty-cycle can be reduced automatically as a function of the supply voltage.

Figure 1. Block Diagram with External Circuit



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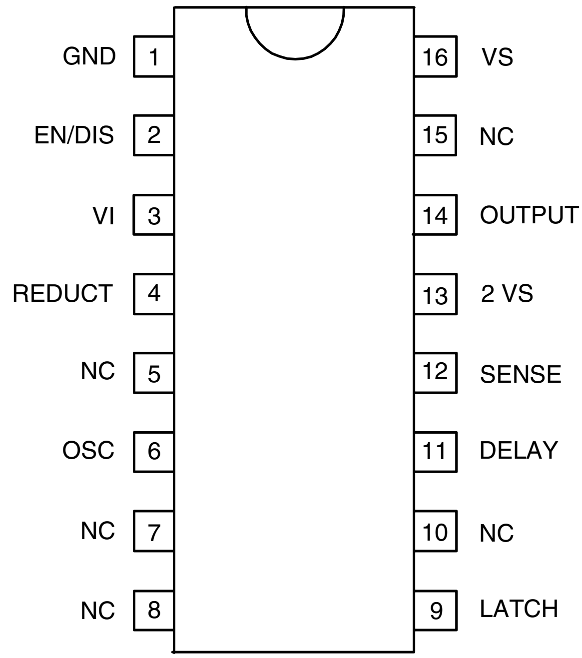
Pin Configuration

Figure 2. Pinning



Pin Description

Pin	Symbol	Function
1	GND	IC ground
2	EN/DIS	Enable/disable
3	VI	Control input (duty cycle)
4	REDUCT	Duty cycle reduction
5	NC	Attenuation
6	OSC	Oscillator
7	NC	Not connected
8	NC	Not connected
9	LATCH	Status short-circuit latch
10	NC	Not connected
11	DELAY	Short-circuit protection delay
12	SENSE	Current sensing
13	2VS	Voltage doubler
14	OUTPUT	Output
15	NC	Not connected
16	VS	Supply voltage V_S

Functional Description

Pin1 – GND

Ground-wire Breakage

To protect the FET in case of ground-wire breakage, a 820 kΩ resistor between gate and source is recommended to provide proper switch-off conditions.

Pin 2 – Enable/Disable

The dimmer can be switched on or off, with pin 2, independently of the set duty cycle.

Table 1. Pin 2 Function

V_2	Function
Approximately > 0.7 V or open	Disable
< 0.7 V or connected to pin 1	Enable

Pin 3 – Control Input

The pulse width is controlled by means of an external potentiometer (47 kΩ). The characteristic (angle of rotation/duty cycle) is linear. The duty cycle be varied from 0 to 100%. It is possible to further restrict the duty cycle with resistors R_1 and R_2 (see Figure 3 on page 8).

Pin 3 is protected against short-circuit to V_{Batt} and ground GND ($V_{Batt} \leq 16.5$ V).

Pin 4 – Duty Cycle Reduction

With pin 4 connected according to Figure 3 on page 8, the set duty cycle is reduced to $V_{Batt} \approx$ 12.5 V. This causes a power reduction in the FET and in the lamps. In addition, the brightness of the lamps is largely independent of the supply voltage range, V_{Batt} = 12.5 to 16 V.

Output Slope Control

The rise and fall time (t_r, t_f) of the lamp voltage can be limited to reduce radio interference. This is done with an integrator which controls a power MOSFET as source follower. The slope time is controlled by an external capacitor C_4 and the oscillator current (see Figure 3 on page 8).

Calculation:

$$t_f = t_r = V_{Batt} \times \frac{C_4}{I_{osc}}$$

With V_{Batt} = 12 V, C_4 = 470 pF and I_{osc} = 40 µA, we thus obtain a controlled slope of

$$t_f = t_r = 12\ \text{V} \times \frac{470\ \text{pF}}{40\ \mu\text{A}} \times 141\ \mu\text{s}$$

Pin 5 – Attenuation

Capacitor C_4 connected to pin 5 damps oscillation tendencies.

Pin 6 – Oscillator

The oscillator determines the frequency of the output voltage. This is defined by an external capacitor, C_2. It is charged with a constant current, I, until the upper switching threshold is reached. A second current source is then activated which taps a double current, 2 × I, from the charging current. The capacitor, C_2, is thus discharged by the current, I, until the lower switching threshold is reached. The second source is then switched off again and the procedure starts once more.

Example for Oscillator Frequency Calculation

$$V_{T100} = V_S \times \alpha_1 = (V_{Batt} - I_S \times R_3) \times \alpha_1$$

$$V_{T<100} = V_S \times \alpha_2 = (V_{Batt} - I_S \times R_3) \times \alpha_2$$

$$V_{TL} = V_S \times \alpha_3 = (V_{Batt} - I_S \times R_3) \times \alpha_3$$

where

V_{T100} = High switching threshold 100% duty cycle

$V_{T<100}$ = High switching threshold < 100% duty cycle

V_{TL} = Low switching threshold

α_1, α_2 and α_3 are fixed values

The above mentioned threshold voltages are calculated for the following values given in the datasheet.

V_{Batt} = 12 V, I_S = 4 mA, R_3 = 150 Ω,

α_1 = 0.7, α_2 = 0.67 and α_3 = 0.28.

V_{T100} = (12 V - 4 mA × 150 Ω) × 0.7 ≈ 8 V

$V_{T<100}$ = 11.4 V × 0.67 = 7.6 V

V_{TL} = 11.4 V × 0.28 = 3.2 V

For a duty cycle of 100%, the oscillator frequency, f, is as follows:

$$f = \frac{I_{osc}}{2 \times (V_{T100} - V_{TL}) \times C_2} \quad \text{where } C_2 = 22\text{ nF and } I_{osc} = 40\ \mu\text{A}$$

Therefore:

$$f = \frac{40\ \mu\text{A}}{2 \times (8\text{ V} - 3.2\text{ V}) \times 22\text{ nF}} = 189\text{ Hz}$$

For a duty cycle of less than 100%, the oscillator frequency, f, is as follows:

$$f = \frac{I_{osc}}{2 \times (V_{T<100} - V_{TL}) \times C_2 + 4 \times V_{Batt} \times C_4}$$

where C_4 = 470 pF

$$f = \frac{40\ \mu\text{A}}{2 \times (7.6\text{ V} - 3.2\text{ V}) \times 22\text{ nF} + 4 \times 12\text{ V} \times 470\text{ pF}} = 185\text{ Hz}$$

A selection of different values of C_2 and C_4 provides a range of oscillator frequencies from 10 to 2000 Hz.

Pins 7, 8, 10 and 15

Not connected.

Pin 9 – Status Short Circuit Latch

The status of the short-circuit latch can be monitored via pin 9 (open collector output).

Table 2. Pin 9 Function

Pin 9	Function
L	Short-circuit detected
H	Not short-circuit detected

Pins 11 and 12 – Short-circuit Protection and Current Sensing

Short-circuit Detection and Time Delay t_d

The lamp current is monitored by means of an external shunt resistor. If the lamp current exceeds the threshold for the short-circuit detection circuit ($V_{T2} \approx$ 90 mV), the duty cycle is switched over to 100% and capacitor C_5 is charged by a current source of 20 µA (I_{ch} - I_{dis}). The external FET is switched off after the cut-off threshold (V_{T11}) is reached. Renewed switching on the FET is possible only after a power-on reset. The current source, I_{dis}, ensures that capacitor C_5 is not charged by parasitic currents. Capacitor C_5 is discharged by I_{dis} to typ. 0.7 V.

Time delay, t_d, is as follows:

$$t_d = C_5 \times \frac{(V_{11} - 0.7\ V)}{(I_{ch} - I_{dis})}$$

With C_5 = 330 nF and V_{Batt} = 12 V, we have

$$t_d = 330\ nF \times \frac{(9.8\ V - 0.7\ V)}{20\ \mu A} = 150\ ms$$

Current Limitation

The lamp current is limited by a control amplifier that protects the external power transistor. The voltage drop across an external shunt resistor acts as the measured variable. Current limitation takes place for a voltage drop of $V_{T1} \approx$ 100 mV. Owing to the difference V_T - $V_{T2} \approx$ 10 mV, current limitation occurs only when the short-circuit detection circuit has responded.

After a power-on reset, the output is inactive for half an oscillator cycle. During this time, the supply voltage capacitor can be charged so that current limitation is guaranteed in the event of a short-circuit when the IC is switched on for the first time.

Pins 13 and 14 – Charge Pump and Output

Pin 14 (output) is suitable for controlling a power MOSFET. During the active integration phase, the supply current of the operational amplifier is mainly supplied by capacitor C_3 (bootstrapping). Additionally, a trickle charge is generated by an integrated oscillator ($f_{13} \approx$ 400 kHz) and a voltage doubler circuit. This permits a gate voltage supply at a duty cycle of 100%.

Pin 16 – Supply Voltage, V_s or V_{Batt}

Undervoltage Detection

In the event of voltages of approximately V_{Batt} < 5.0 V, the external FET is switched off and the latch for short-circuit detection is reset.

A hysteresis ensures that the FET is switched on again at approximately $V_{Batt} \geq$ 5.4 V.

Overvoltage Detection

Stage 1

If overvoltages of V_{Batt} > 20 V (typically) occur, the external transistor is switched off and switched on again at V_{Batt} < 18.5 V (hysteresis).

Stage 2

If V_{Batt} > 28.5 V (typically), the voltage limitation of the IC is reduced from 26 V to 20 V. The gate of the external transistor remains at the potential of the IC ground, thus producing voltage sharing between the FET and lamps in the event of overvoltage pulses (e.g., load-dump). The short-circuit protection is not in operation. At V_{Batt} < 23 V, the overvoltage detection stage 2 is switched off.

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Parameters	Symbol	Value	Unit
Junction temperature	T_j	150	°C
Ambient temperature range	T_{amb}	-40 to +110	°C
Storage temperature range	T_{stg}	-55 to +125	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	120	K/W

Electrical Characteristics

T_{amb} = -40 to +110°C, V_{Batt} = 9 to 16.5 V, (basic function is guaranteed between 6.0 V to 9.0 V) reference point ground, unless otherwise specified (see Figure 1 on page 1). All other values refer to pin GND (pin 1).

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Current consumption	Pin 16	I_S			6.8	mA
Supply voltage	Overvoltage detection, stage 1	V_{Batt}			25	V
Stabilized voltage	I_S = 10 mA, pin 16	V_S	24.5		27.0	V
Battery undervoltage detection	- on - off	V_{Batt}	4.4 4.8	5.0 5.4	5.6 6.0	V
Battery Overvoltage Detection	**Pin 2**					
Stage 1:	- on - off	V_{Batt}	18.3 16.7	20.0 18.5	21.7 20.3	V
Stage 2:	- on - off	V_{Batt}	25.5 19.5	28.5 23.0	32.5 26.5	V
Stabilized voltage	I_S = 30 mA, pin 16	V_Z	18.5	20.0	21.5	V
Short-circuit Protection	**Pin 12**					
Short-circuit current limitation	$V_{T1} = V_S - V_{12}$	V_{T1}	85	100	120	mV
Short-circuit detection	$V_{T2} = V_S - V_{12}$	V_{T2}	75	90	105	mV
		$V_{T1} - V_{T2}$	3	10	30	mV
Delay Timer Short-circuit Detection	**Pin 11**					
Switched off threshold	$V_{T11} = V_S - V_{11}$	V_{T11}	9.5	9.8	10.1	V
Charge current		I_{ch}		23		µA
Discharge current		I_{dis}		3		µA
Capacitance current	$I_5 = I_{ch} - I_{dis}$	I_5	13	20	27	mA
Output short-circuit latch	Pin 9					
Saturation voltage	I_9 = 100 µA	V_{sat}		150	350	mV

Notes: 1. Reference point is battery ground

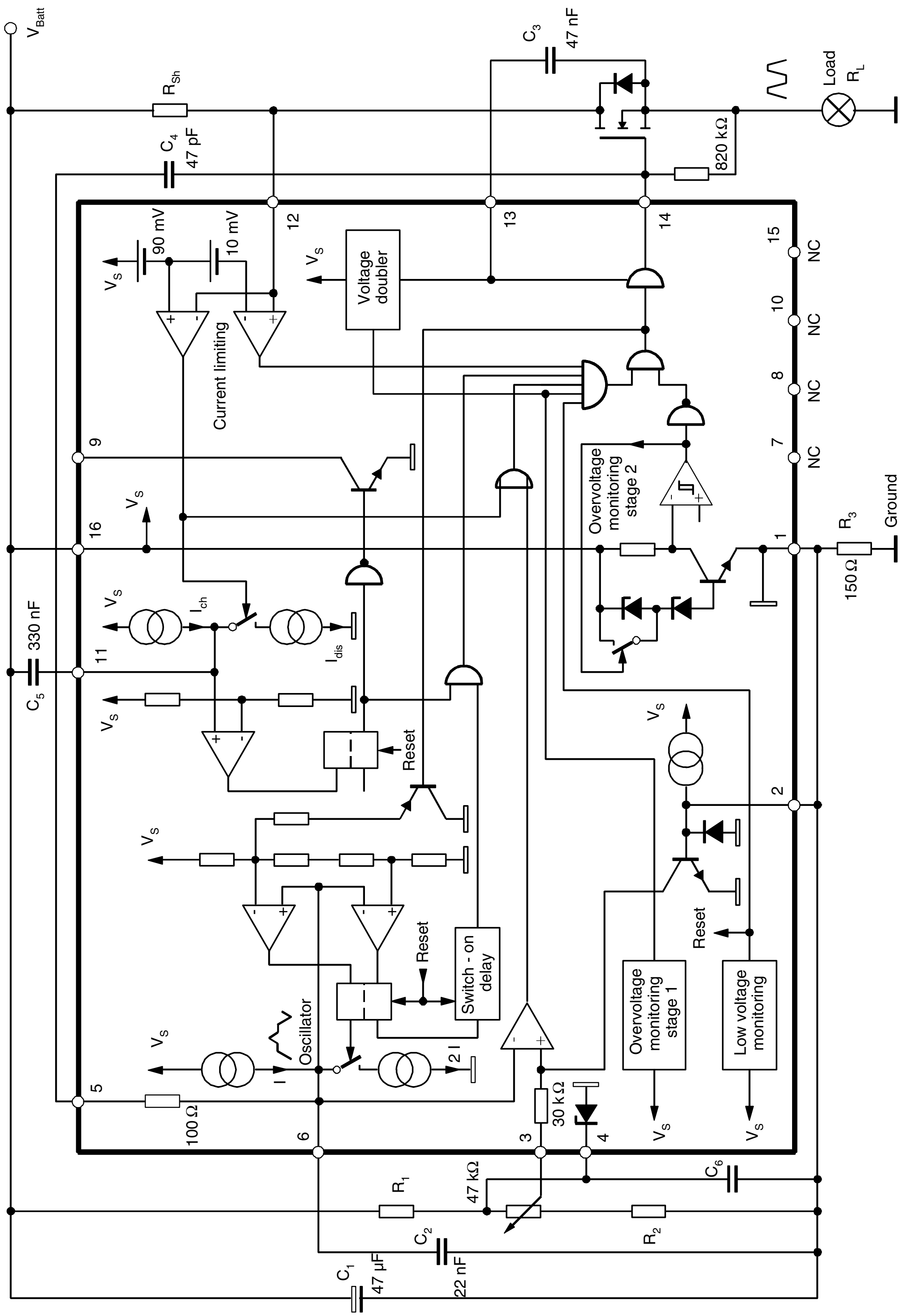
Electrical Characteristics (Continued)

T_{amb} = -40 to +110°C, V_{Batt} = 9 to 16.5 V, (basic function is guaranteed between 6.0 V to 9.0 V) reference point ground, unless otherwise specified (see Figure 1 on page 1). All other values refer to pin GND (pin 1).

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Voltage Doubler	**Pin 13**					
Voltage	Duty cycle 100%	V_{13}	2 V_S			
Oscillator frequency		f_{13}	280	400	520	kHz
Internal voltage limitation	I_{13} = 5 mA	V_{13}	26	27.5	30.0	V
	(whichever is lower)	V_{13}	(V_{S+14})	(V_{S+15})	(V_{S+16})	
Gate Output	**Pin 14**					
Voltage	Low level	V_{14}	0.35	0.70	0.95	V
	V_{Batt} = 16.5 V, T_{amb} = 110°C, R_3 = 150 Ω				1.5[1]	
	High level, duty cycle 100%	V_{14}		V_{13}		
Current	V_{14} = Low level	I_{14}	1.0			mA
	V_{14} = High level, $I_{13} > \lvert I_{14} \rvert$		-1.0			
Enable/Disable	**Pin 2**					
Current	V_2 = 0 V	I_2	-20	-40	-60	µA
Duty Cycle Reduction	**Pin 4**					
Z-voltage	I_4 = 500 µA	V_4	6.9	7.4	8.0	V
Oscillator						
Frequency	Pin6	f	10		2000	Hz
Threshold cycle Upper	$V_{14} = \text{High}, \alpha_1 = \frac{V_{T100}}{V_S}$	α_1	0.68	0.7	0.72	
Lower	$V_{14} = \text{Low}, \alpha_2 = \frac{V_{T<100}}{V_S}$	α_2	0.65	0.67	0.69	
	$\alpha_3 = \frac{V_{TL}}{V_S}$	α_3	0.26	0.28	0.3	
Oscillator current	V_{Batt} = 12 V	$\pm I_{osc}$	26	40	54	µA
Frequency tolerance	C_4 open, C_2 = 470 nF, duty cycle = 50%	f	6.0	9.9	13.5	Hz

Notes: 1. Reference point is battery ground

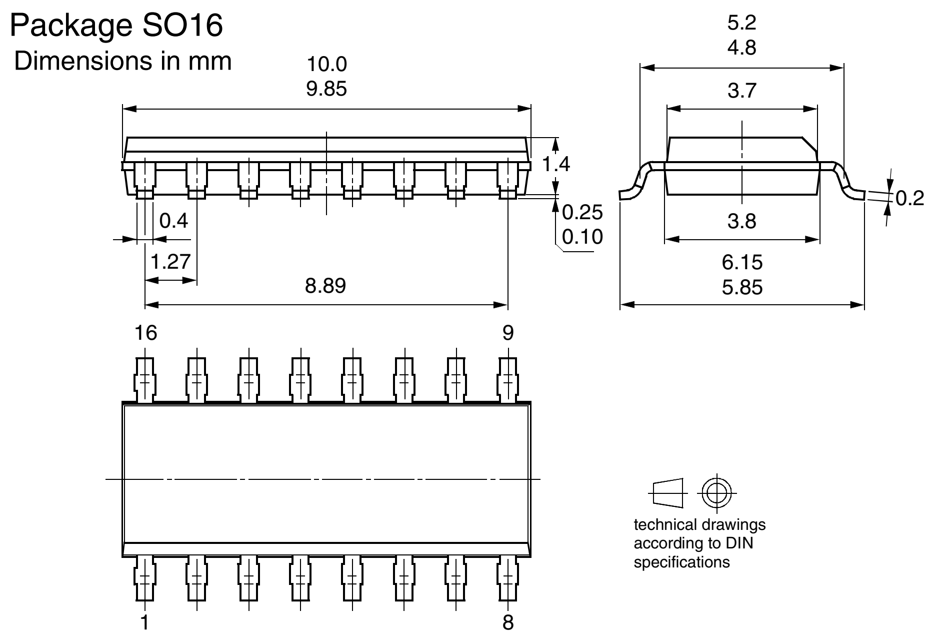
Figure 3. Application



Ordering Information

Extended Type Number	Package	Remarks
U6084B-FP	SO16	–

Package Information



Revision History

Please note that the referring page numbers in this section are referred to the specific revision mentioned, not to this document.

Changes from Rev. 4677A - 02/03 to Rev. 4677B - 02/04

1. Block Diagram on page 1 changed.
2. New heading rows at Table "Absolute Maximum Ratings" on page 6 added.

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