Description

The 256Mb DDR SDRAM is a high-speed COMS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM.

The 256Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb DDR SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

The 256Mb DDR SDRAM operates from a differential clock (CLK and CLK#; the crossing of CLK going HIGH and CLK# going LOW will be referred to as the postive edge of CLK). Commands (address and control signals) are registered at verey positive edge of CLK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CLK.

Read and Write assesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0,BA1 select the bank; A0-A12 select the row). The address bits registered coincident with sthe READ or WRITE command are used to select the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2,4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a selftimed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

The 256Mb DDR SDRAM is designed to operate in either low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Initial devices will have a VDD supply of 3.3V (nominal). Eventually, all devices will migrate to a VDD supply of 2.5V(nominal). During this initial period of product availability. this split will be vendor and device specific.

This data sheet includes all features and functionality required for JEDEC DDR devices; options not required but listed, are noted as such. Certain vendors may elect to offer a superset of this specification by offering improved timing and/or including optional features. Users benefit from knowing that any system design based on the required aspects of this specification are supported by all DDR SDRAM vendors; conversely, users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

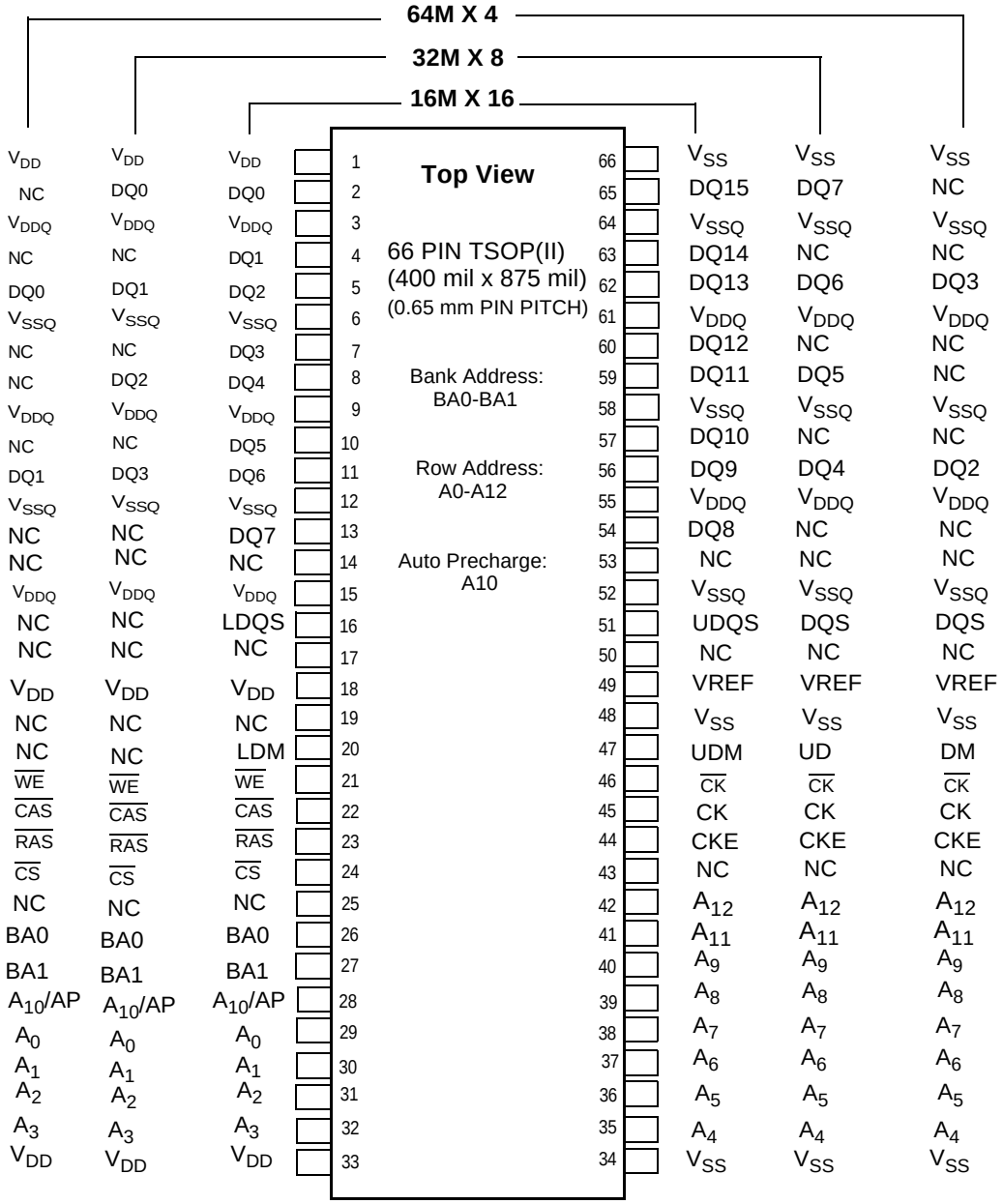
Note: The functionality described in, and the timing specifications included in this data sheet are for the DLL Enabled mode of operation. This is the only normal operating mode for these DDR devices.

Features

- Double-data-rate architecture: two data transfers per clock cycle
- Bidirectional, intermittent data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for READs: center-aligned with data for WRITEs
- Differential clock inputs (CLK and CLK#)
- DLL aligns DQ and DQS transitions with CLK transitions
- Commands entered on each positive CLK edge; data referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths:2,4, or 8
- CAS Latency: 2 or 2.5
- AUTO PRECHARGE option for each burst access
- Auto Refresh and Self Refresh Modes
- 7.81us Auto Refresh Interval
- 2.5V (SSTL_2 compatible) I/O
- VDDQ=+2.5V ±0.2V
- VDD=+3.3V ±0.3V

Pin Configuration

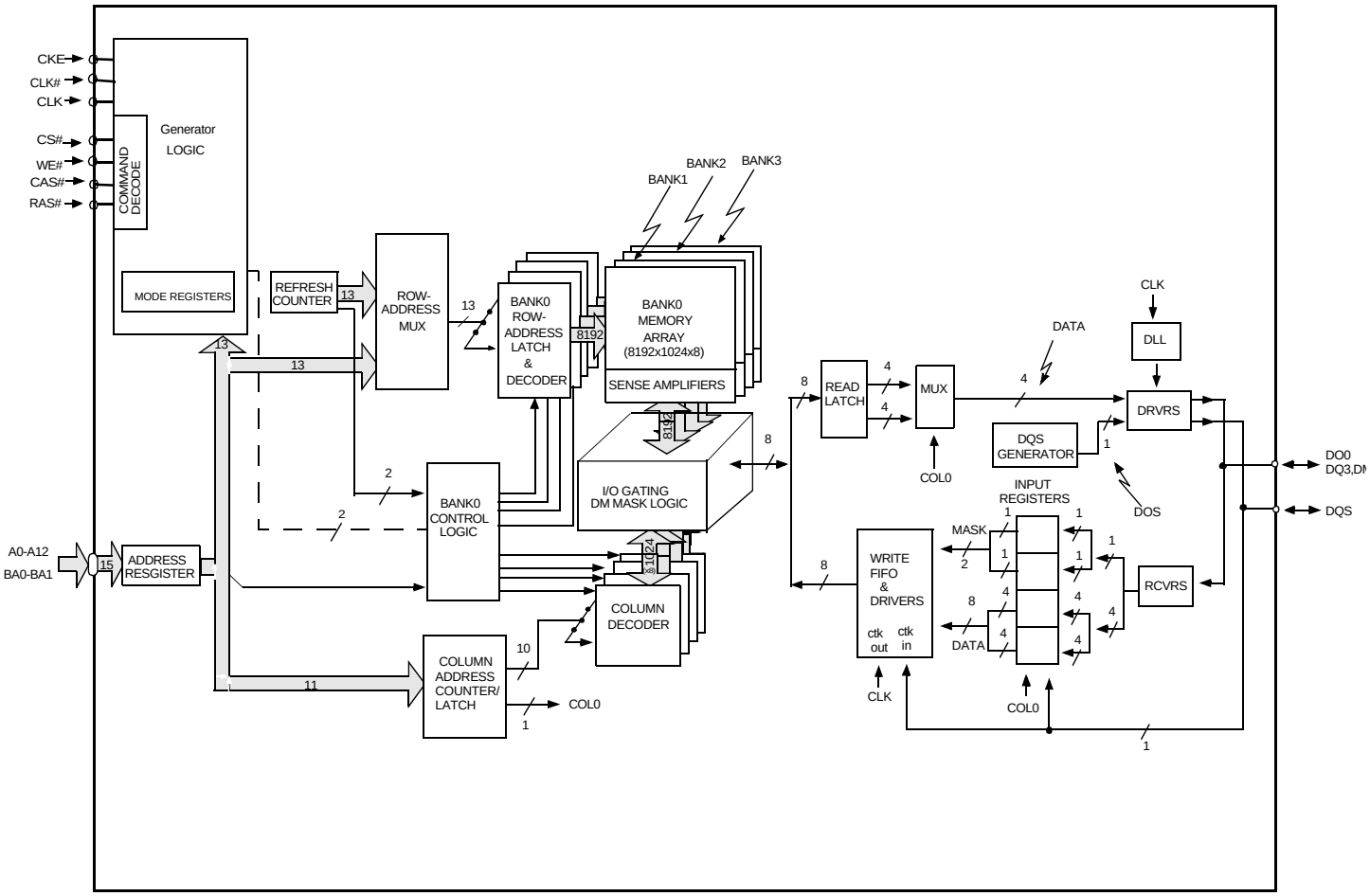
256M DDR SDRAM (x4/x8/x16) Pin-out



Column Address Table

Organization	Column Address
64Mx4	A0-A9,A11
32Mx8	A0-A9
16Mx16	A0-A8

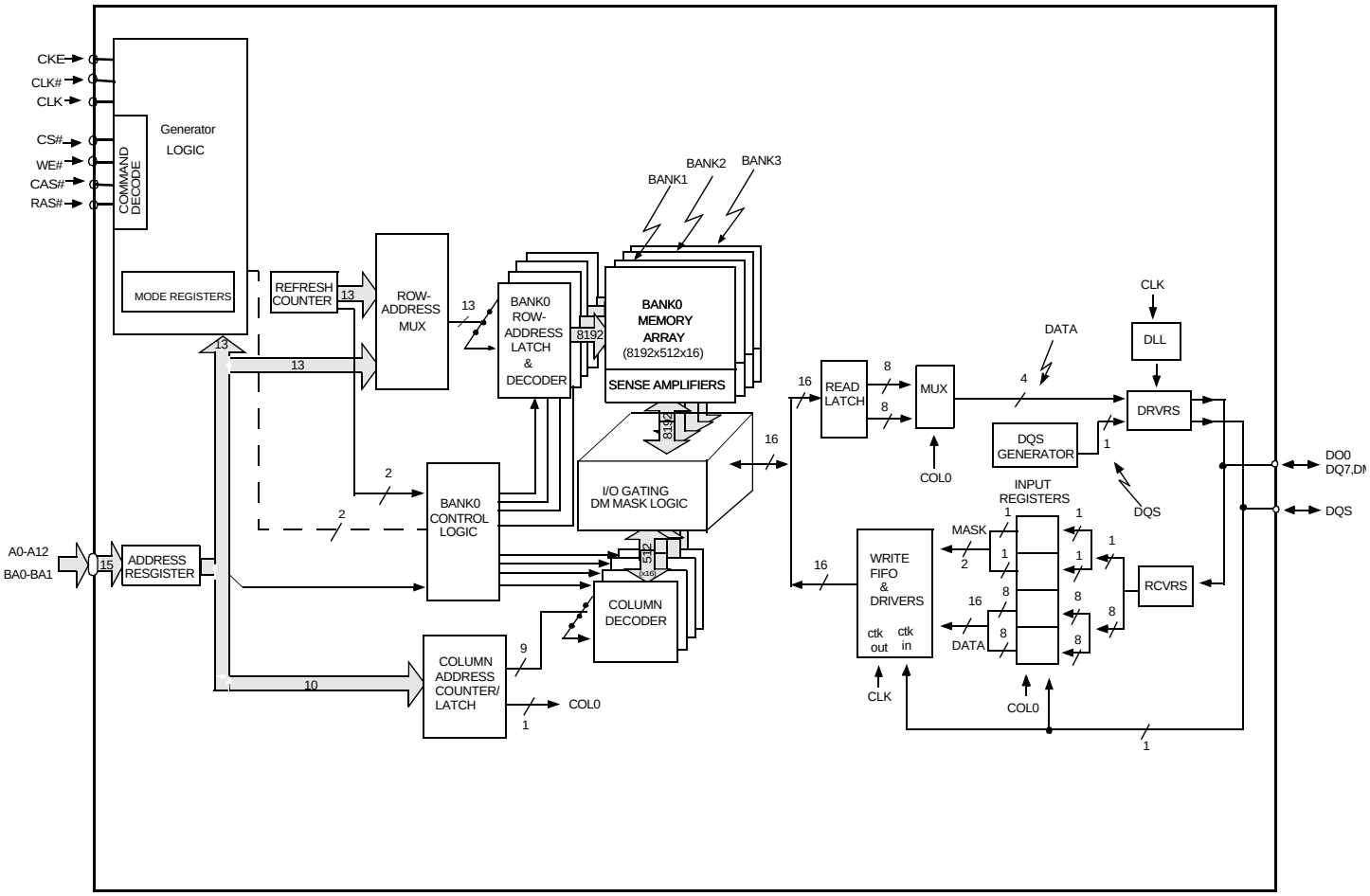
FUNCTIONAL BLOCK DIAGRAM- X4 CONFIGURATION



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not necessarily represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

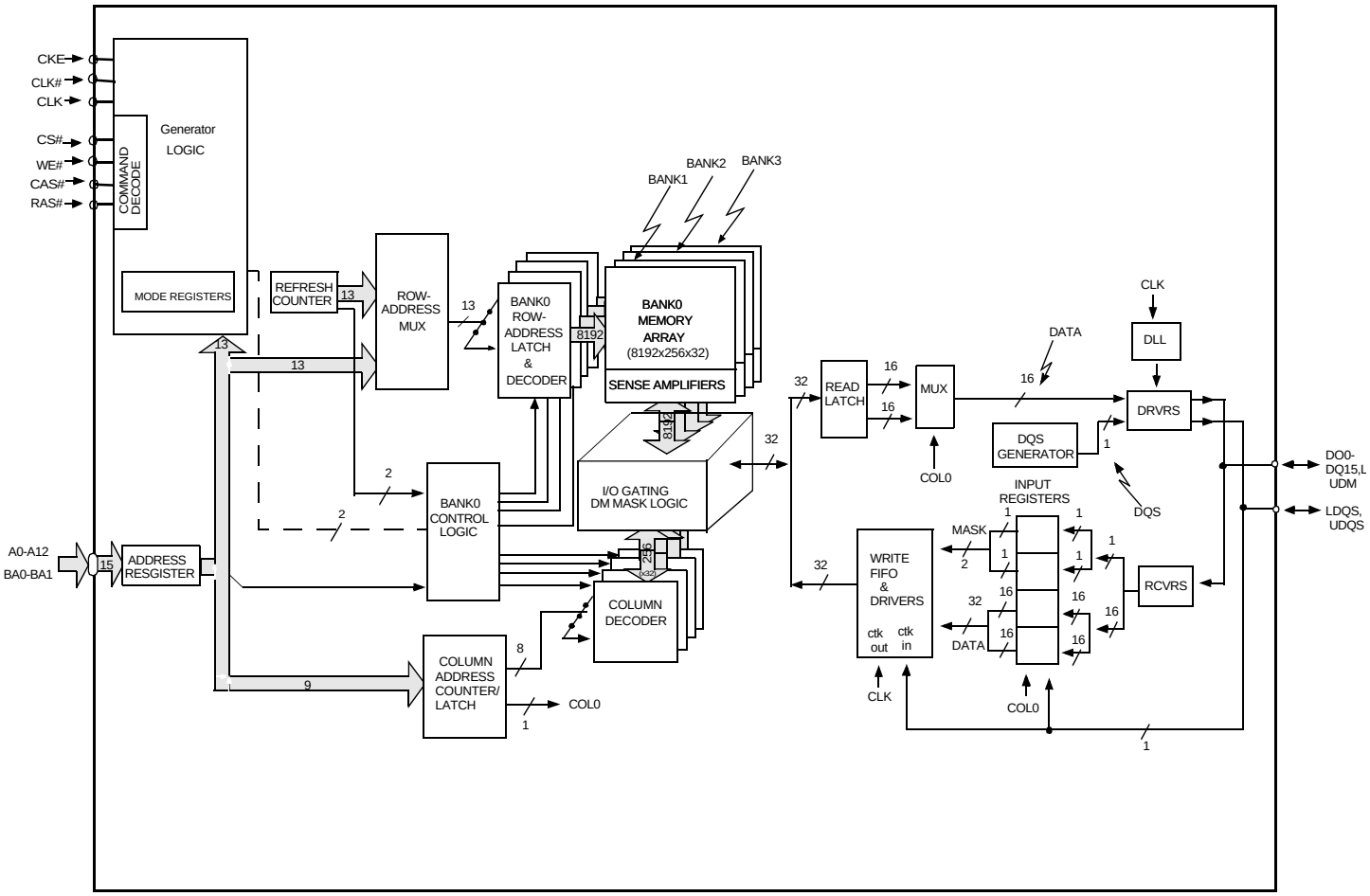
FUNCTIONAL BLOCK DIAGRAM- X8 CONFIGURATION



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not necessarily represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only)m but is internally loaded to match the load of the bidirectional DQ and DQS signals.

FUNCTIONAL BLOCK DIAGRAM- X16 CONFIGURATION



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not necessarily represent an actual circuit implementation.

Note 2: LDM and VDM are unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

PIN DESCRIPTIONS

Symbol	Type	Description
CLIK,CLK#	Input	Clock: CLK and CLK# are differential clock inputs. All address and control input signals are sampled on the positive edge of CLK/negative edge of CLK#. Ouptut(read) data is referenced to both edges of CLK. Internal clock signals are dervied from CLK/CLK#.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CLK, CLK# and CKE are disabled during power-down and self refresh modes, providing low standby power. CKE will recognize an LVCMOS LOW level prior to VREF being stable on power-up.
CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
RAS#,CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
DM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. DM pins include dummy loading internally, to match the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-DQ7; UDM corresponds to the data on DQ8-DQ15.
BA0,BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A0-A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0,BA1. The address inputs also provide the op-code durinbg a LOAD MODE REGISTER command.
DQ	I/O	Data Input/Output: Data bus
DQS	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15.
NC	-	No Connect: these pins should be left unconnected.
V_{DDQ}	Supply	DQ Power Supply:+2.5V ±0.2V .
V_{SSQ}	Supply	DQ Ground.
V_{DD}	Supply	Power Supply: +3.3V ±0.3V .
V_{SS}	Supply	Ground.
V_{REF}	Input	SSTL_2 reference voltage.

Description

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The 256Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb DDR SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command. which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0,BA1 select the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. the following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to V_{DD}, then to V_{DDQ}, and finally to V_{REF} (and to the system V_{TT}). V_{TT} must be applied after V_{DDQ} to avoid device latch-up, which may cause permanent damage to the device. V_{REF} can be applied any time after V_{DDQ}, but is expected to be nominally coincident with V_{TT}. Except for CKE, inputs are not recognized as valid until after V_{REF} is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after V_{DD} is applied. Maintaining an LVCMOS LOW level on CKE during power-up will put the DQ and DQS outputs in the High-Z stage, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200μs delay prior to applying an executable a command.

Once the 200μs delay has been satisfied, a COMMAND INHIBIT or NOP comand should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a LOAD MODE REGISTER command should be issued for the Extended Mode Register to enable the DLL, then a LOAD MODE REGISTER comand should be issued for the base mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any read command. A PRECHARGE ALL command should be applied, placing the device in the "all banks idle" stage.

Once in the idle state, two AUTO REFRESH cycles must be performed. Additionally, a LOAD MODE REGISTER command for the base Mode Register, with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

Register Definition

Base Mode Register

The base mode register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in Figure 1. The base mode register is programmed via the LOAD MODE REGISTER command (with BA0=0 and BA1=0) and will retain the stored information unitil it is programmed again or the device loses power.

Base mode register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4-M6 specify the CAS latency, and M7-M11 specify the operating mode.

The base mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

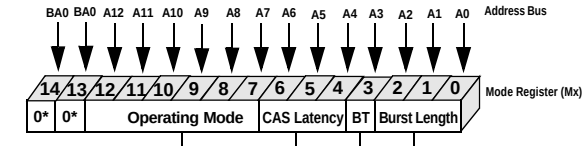
Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 1. the burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two, by A2-Ai when the burst length is set to four and by A3-Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type



M2 M1 M0	Burst Length	
	M3=0	M3=1
0 0 0	Reserved	Reserved
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3(optional)
1 0 0	Reserved
1 0 1	1.5(optional)
1 1 0	2.5
1 1 1	Reserved

M12	M11	M10	M9	M8	M7	M6-10	Operating Mode
0	0	0	0	0	0	Valid	Normal Operation
0	0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	-	All other states reserved

Figure 1

BASE MODE REGISTER DEFINITION

Table 1

BURST DEFINITION

Burst Length	Starting Column Address:	Order of Accesses Within a Burst	
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1-A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

NOTE:

1. For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-Ai selects the eight-data-element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to 2 or 2.5 clocks (latencies of 1.5 or 3 are optional, and one or both of these optional latencies might be supported by some vendors).

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available nominally coincident with clock edge n + m. Table 2 below indicated the operating frequencies at which each CAS latency setting can be used.

Reserved stated should not be used as unknown operation, or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by setting M7-M12 to zero; to reset the DLL and select normal operation , program M7, M9-M12 to 0 and M8 to 1. All other combinations of values for M7-M12 are reserved for future use and/ or test modes.

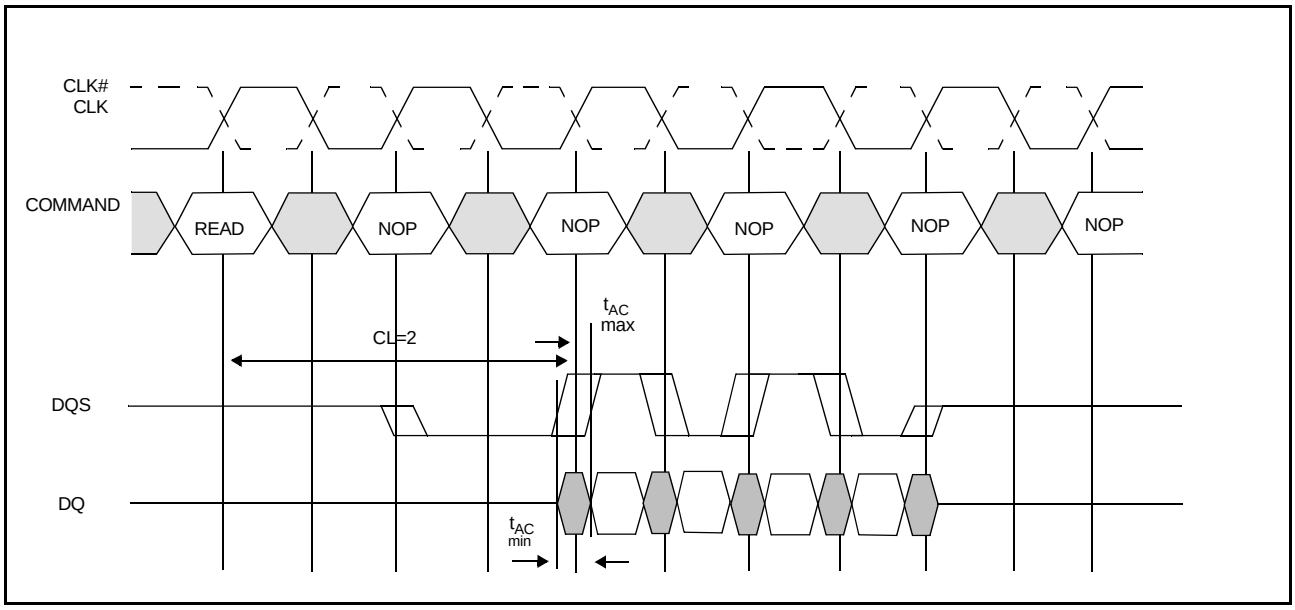
Test Modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

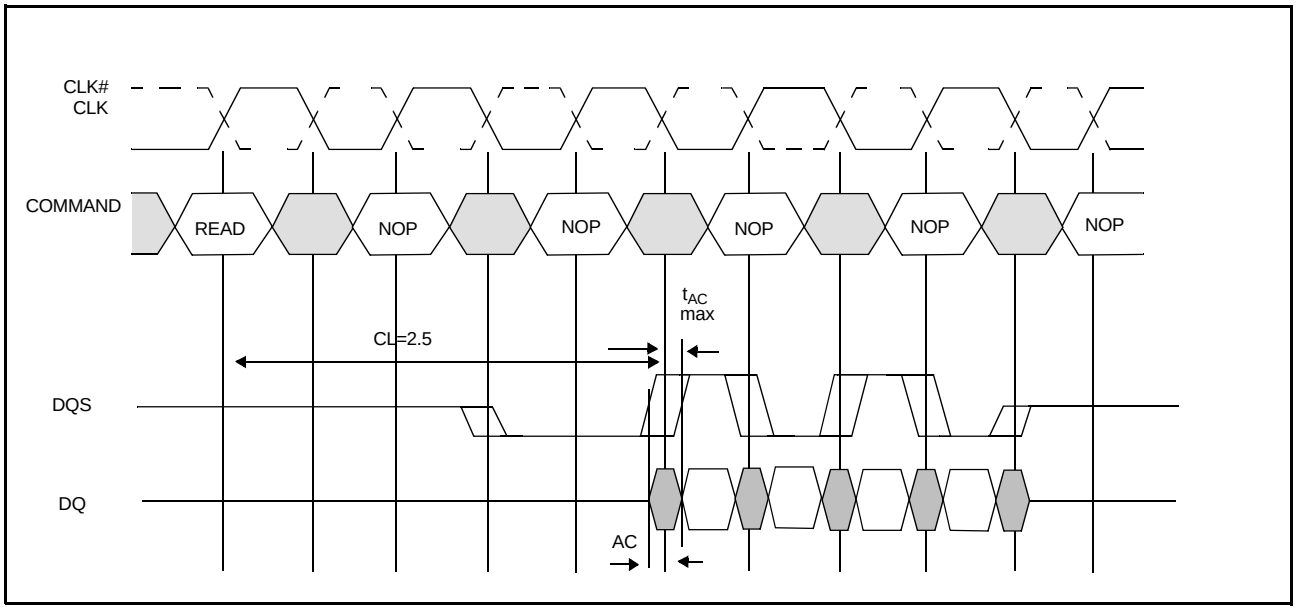
Table 2

CAS LATENCY

SPEED GRADE	MAXIMUM OPERATING			
	CAS LATENCY =1.5	CAS LATENCY =2	CAS LATENCY =2.5	CAS LATENCY =3
-75	100	133	150	200
-8	100	125	143	166

* Values are nominal (i.e. may have been rounded off; exact tCK should be used)

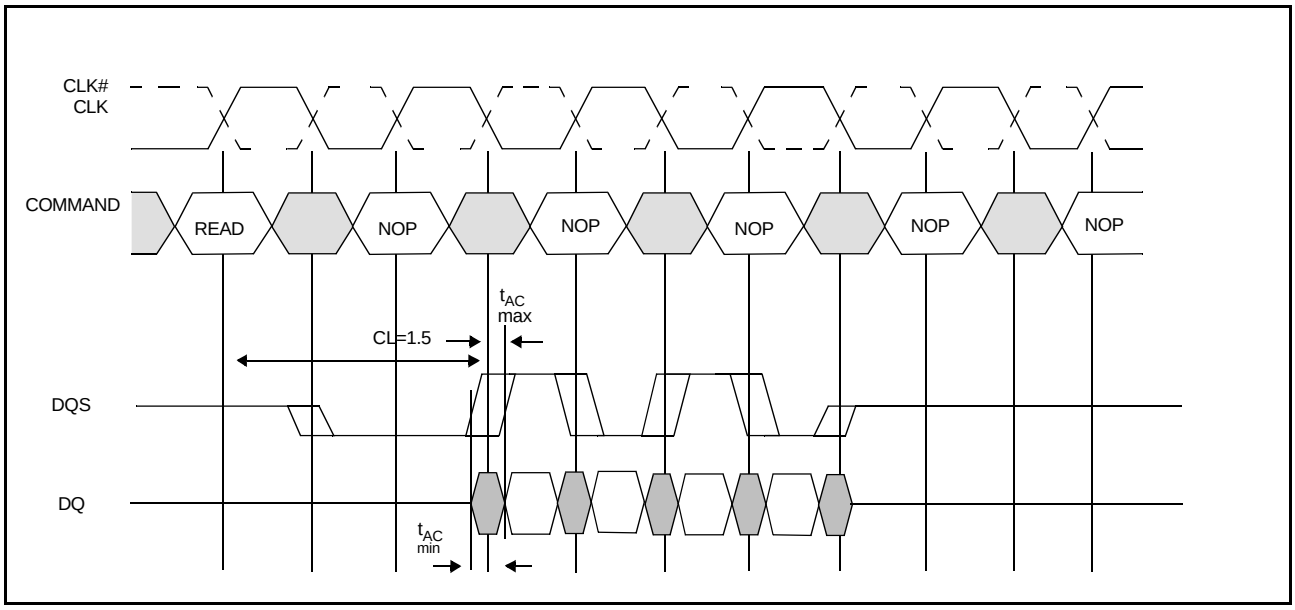


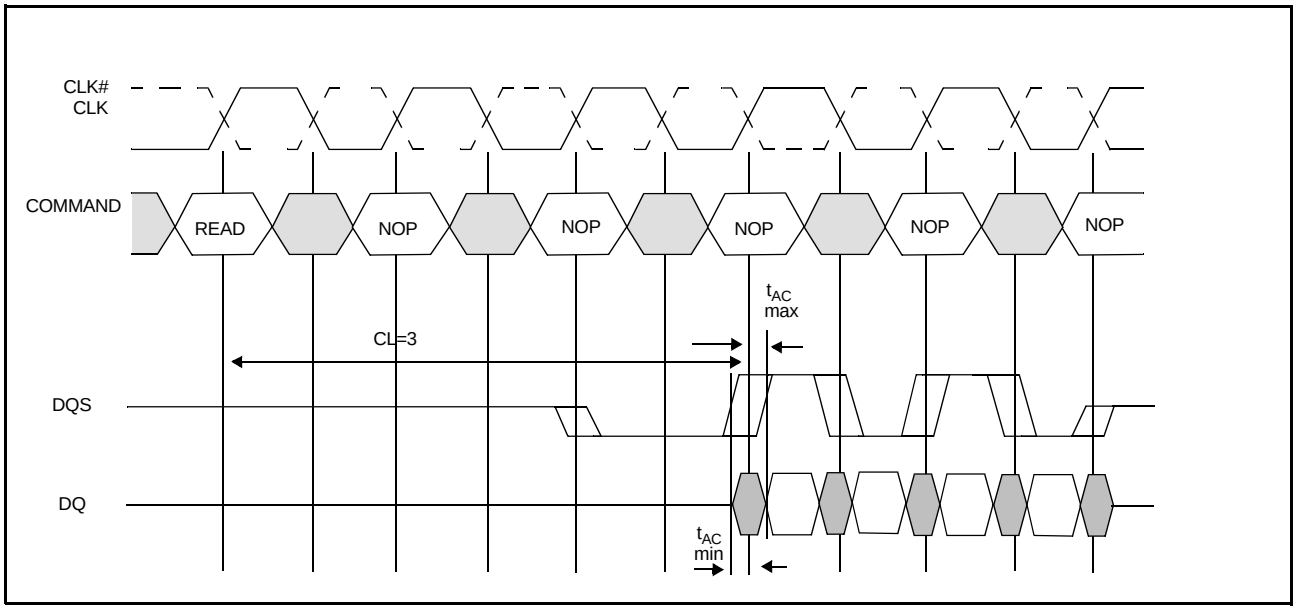


DONT CARE
UNDEFINED

Burst Length=4 in the cases shown

Figure 2a
REQUIRED CAS LATENCIES





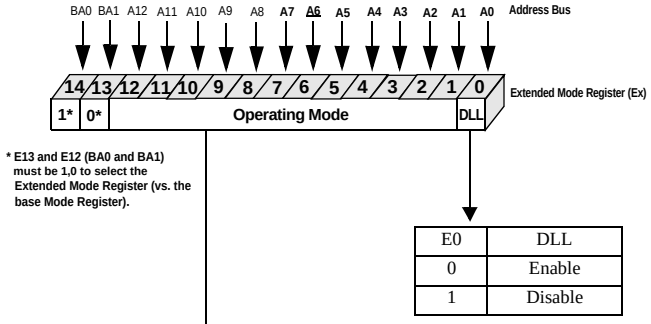
Burst Length=4 in the cases shown

Figure 2b
OPTIONAL CAS LATENCIES

EXTENDED MODE REGISTER

The Extended Mode Resister is used to enable or disable the DLL of the DDR SDRAM, as shown in Figure 3. The Extended Mode Register is programmed via the LOAD MODE REGISTER command (with BA0=1 and BA1=0) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Voolating either of these requirements will result in unspecified operaiton.



E0	DLL
0	Enable
1	Disable

E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	Operating Mode
0	0	0	0	0	0	0	0	0	0	0	0	Valid	Normal Operation
-	-	-	-	-	-	-	-	-	-	-	-	-	All other stateds reserved

Figure 3

EXTENDED MODE REGISTER DEFINITION

COMMANDS

Truth Table 1 provides a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables appear following the Operation section; these tables provide current state/next state information.

TRUTH TABLE 1-Commands and DM Operation

(Notes:1)

Burst Length	CS#	RAS#	CAS#	WE#	DM	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	X	Bank/col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	X	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	9
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6,7
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	2
Write Enable	-	-	-	-	L	-	Active	8
Write Inhibit	-	-	-	-	H	-	High-Z	8

NOTE: 1. CKE is HIGH for all commands shown except SELF REFRESH.

2. BA0-BA1 select either the Base or the Extended Mode Register (BA0=0, BA=1 selects Base Mode Register; BA0=1, BA1=0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A12 provide the op-code to be written to the selected mode Register.
3. BA0-BA1 provide bank address and A0-A12 provide row address.
4. BA0-BA1 provide bank address; A0-Ai provide column address (where i=8 for x16, 9 for x8 and 11 for x4 except A10); A10 HIGH enables the auto precharge feature (nonpersistent), A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0-BA1 determine which bank is precharged.
   A10 HIGH: all banks are precharged and BA0-BA1 are "Dont Care."
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Dont Care" except for CKE.
8. Used to mask write data; provided conicident with the corresponding data.
9. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an DDR SDRAM which is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode registers are loaded via inputs A0-A12 See mode register descriptions in the Register Definition section. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank . A PRECHARGE command must be issued befor opening a different row in the same bank.

READ

The READ command is used to initaiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai(where i=8 for x 16, 9 for x8 or 11 for x 4, except A10) selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the READ burst; if AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initaiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai(where i=8 for x 16, 9 for 8 or 11 for x 4, except A10) selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the WRITE burst; if AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident whith the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with autoprecharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analagous to CAS# BEFORE-RAS# (CBR) REFRESH in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command. The 256Mb DDR SDRAM requires AUTO REFRESH cycles at an average interval of 7.81μs(maximum).

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode,the DDr SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon exiting SELF REFRESH (200 clock cycles must then occur befor a READ command can be issued). Input signals except CKE are "Dont Care" during SELF REFRESH.

Once self refresh mode is engaged, the DDR SDRAM provides its own internal clocking, causing it to perform its own AUTO REFRESH cycles. The DDR SDRAM must remain in self refresh mode for a minimum period equal to ^{t}RAS and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for ^{t}XSR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

OPERATIONS

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the DDR SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

After opening a row (issuing an ACTIVE command). a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

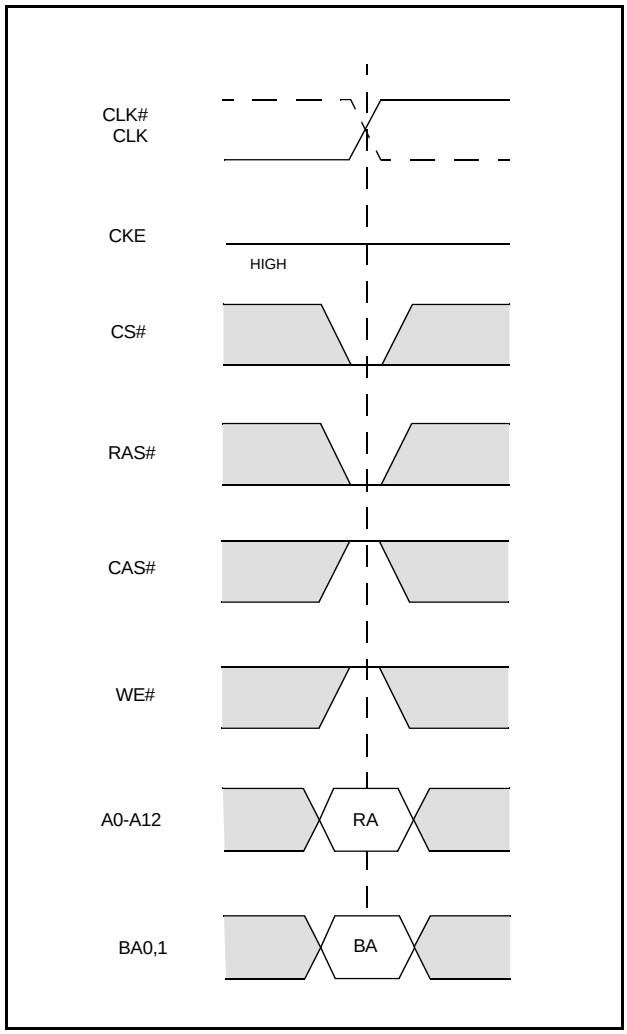


Figure 4
ACTIVATING A SPECIFIC ROW IN A SPECIFIC BANK

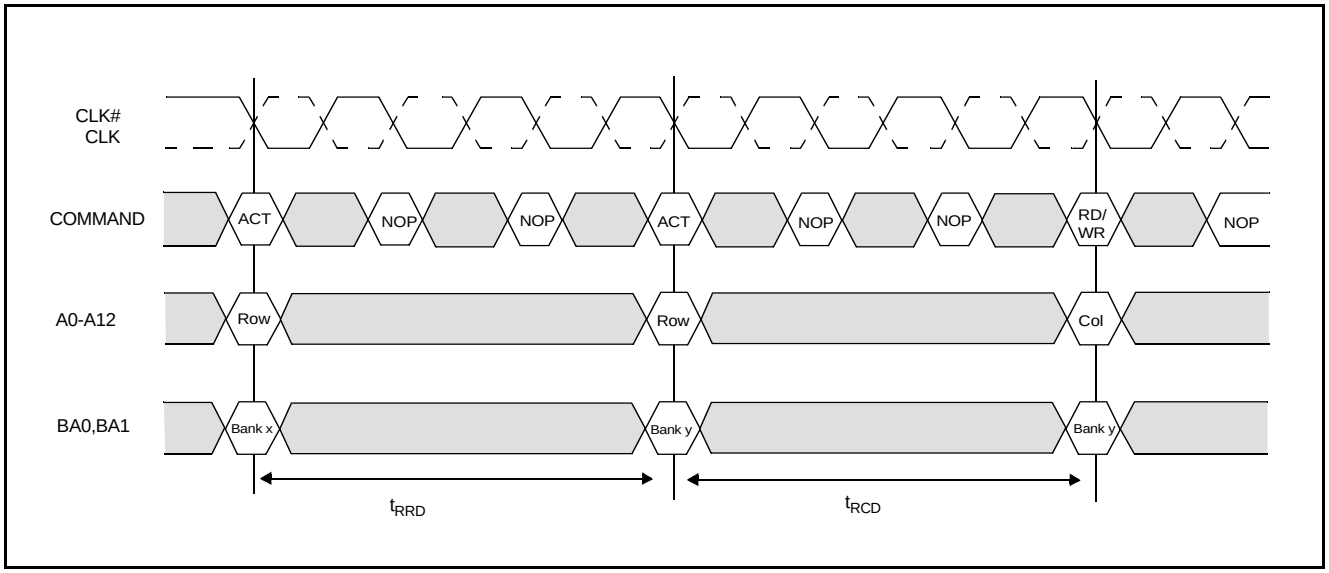


Figure 5
t_{RCD} AND t_{RRD} Definition

READs

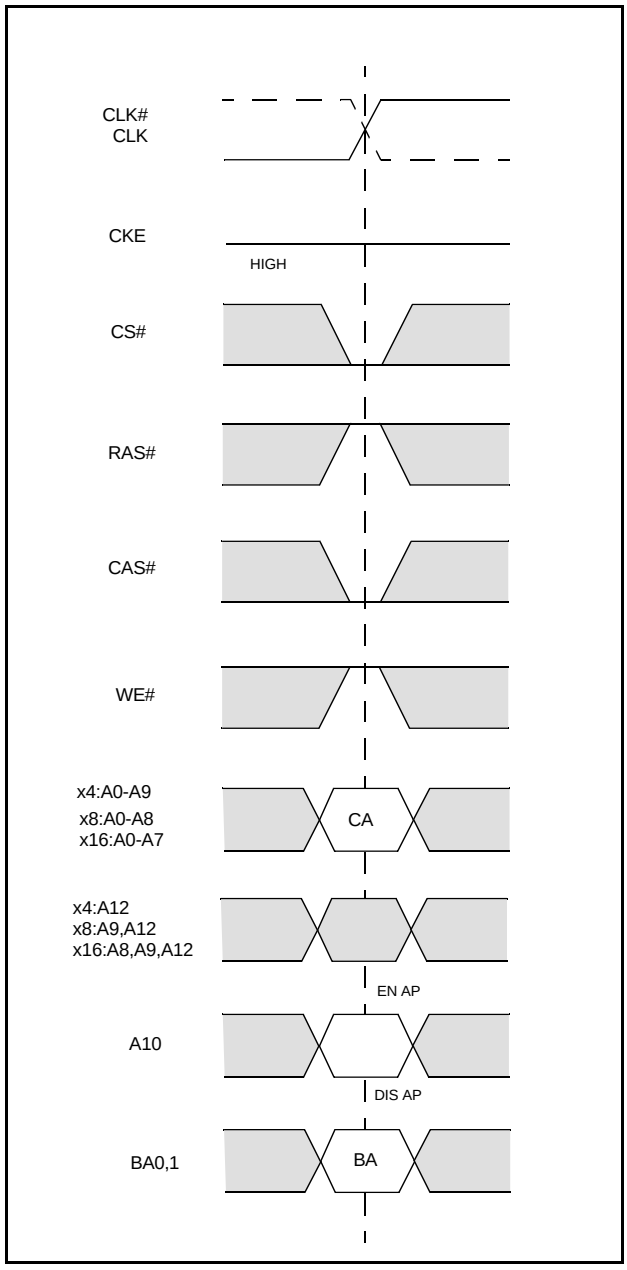
READ bursts are initiated with a READ command, as shown in Figure 6.

The starting column and bank addresses are provided with the READ command and AUTO PRECHARGE is either enabled or disabled for that burst access. If AUTO PRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, AUTO PRECHARGE is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e. at the next crossing of CLK and CLK#). Figure 7 shows general timing for each posible CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z.

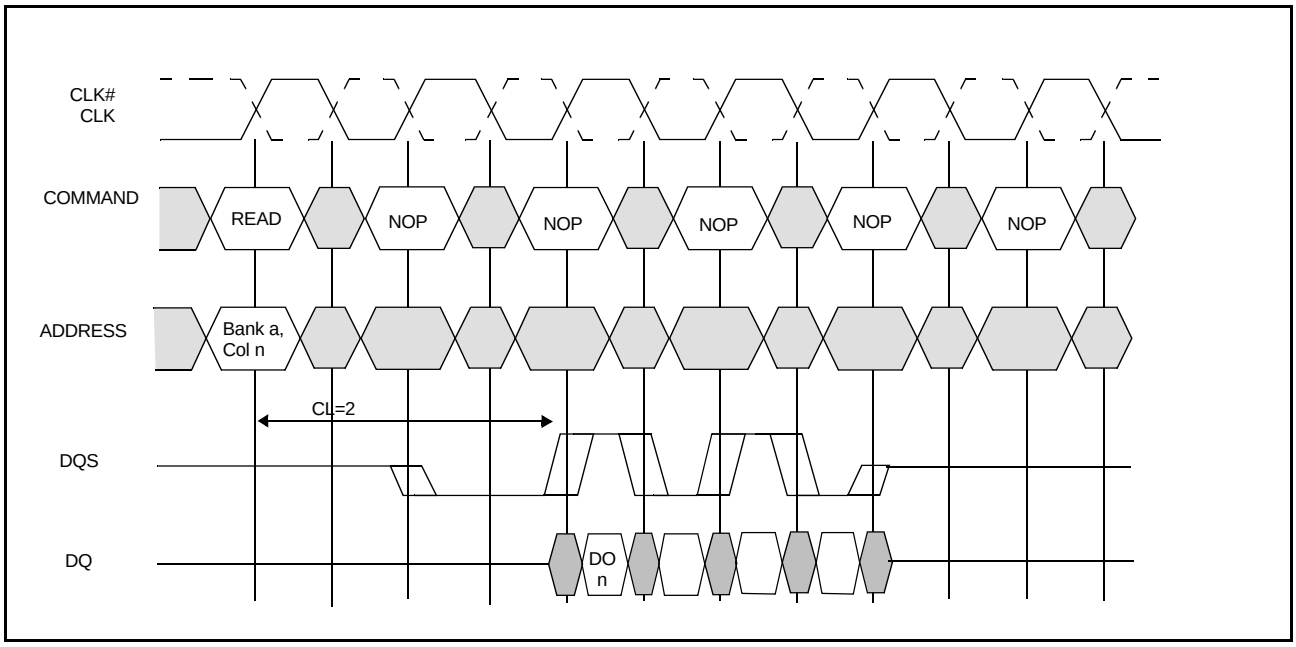
Data fom any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follow either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued x cycles after the first READ command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in Figure 8. A READ command can be initiated on any clock cycle following a previous READ command. Non consecutive READ data is shown for illustration in figure 9. Full-speed random read accesses within a page (or pages) can be performed as shown in Figure 10.

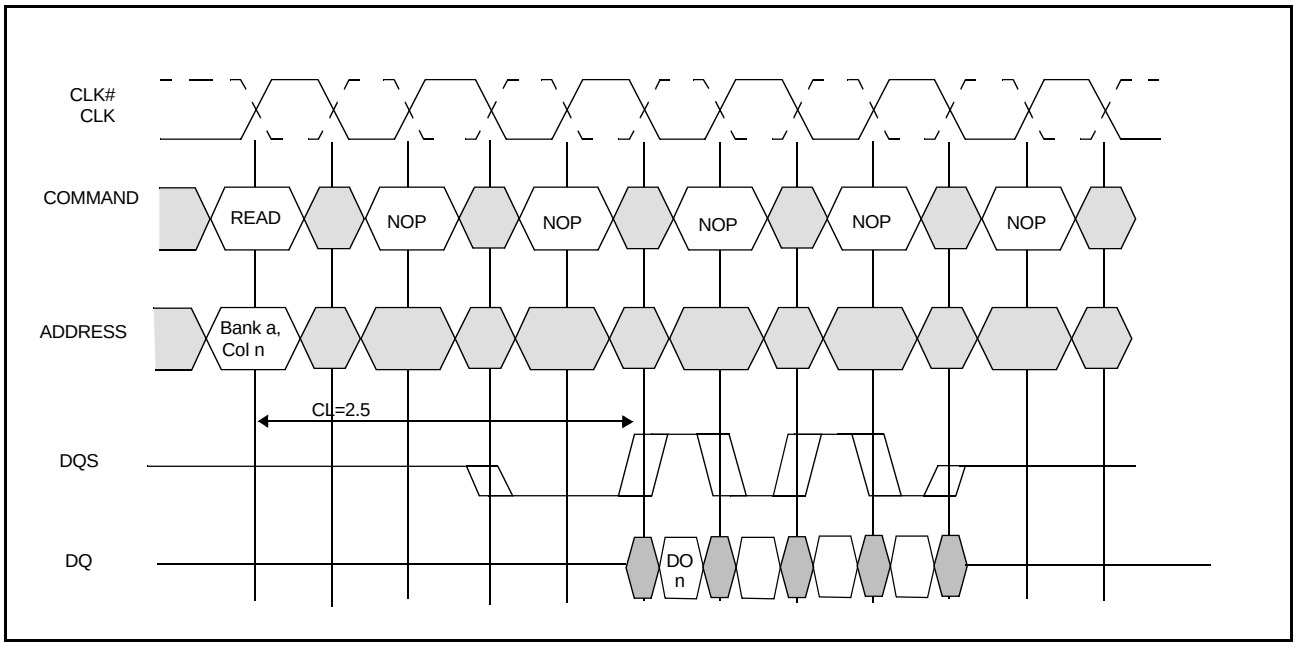


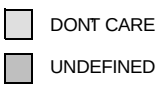
=DONT CARE

CA = Column Address
BA = Bank Address
EN AP = Enable Autoprecharge
DIS AP = Disable Autoprecharge

Figure 6
READ COMMAND

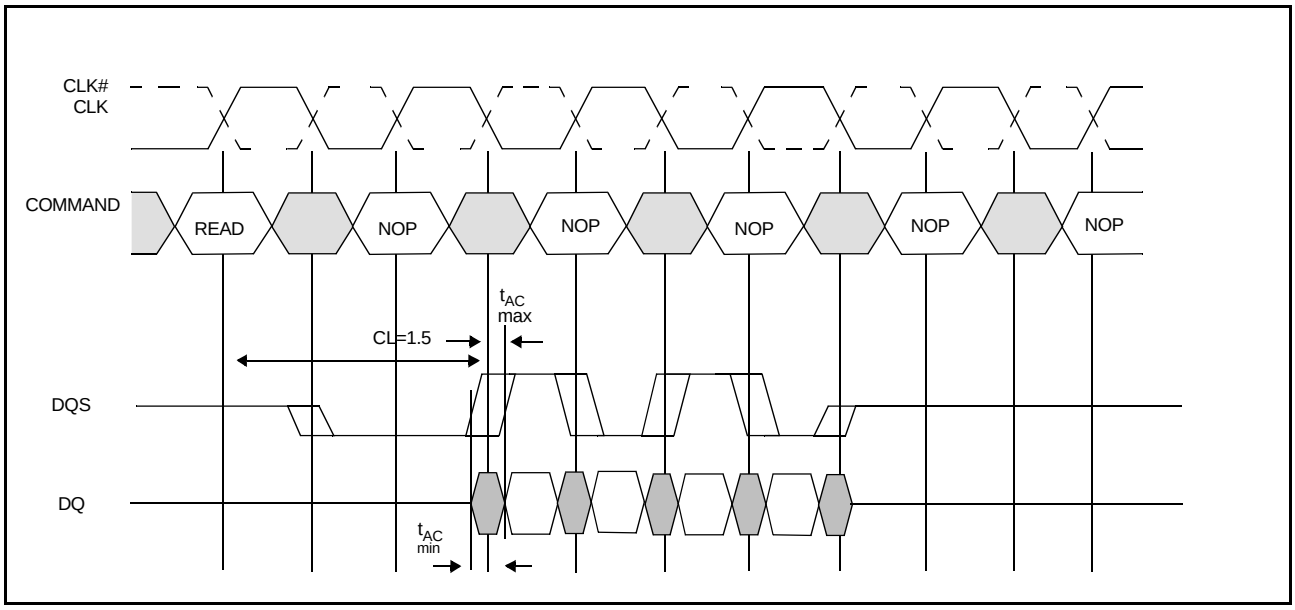


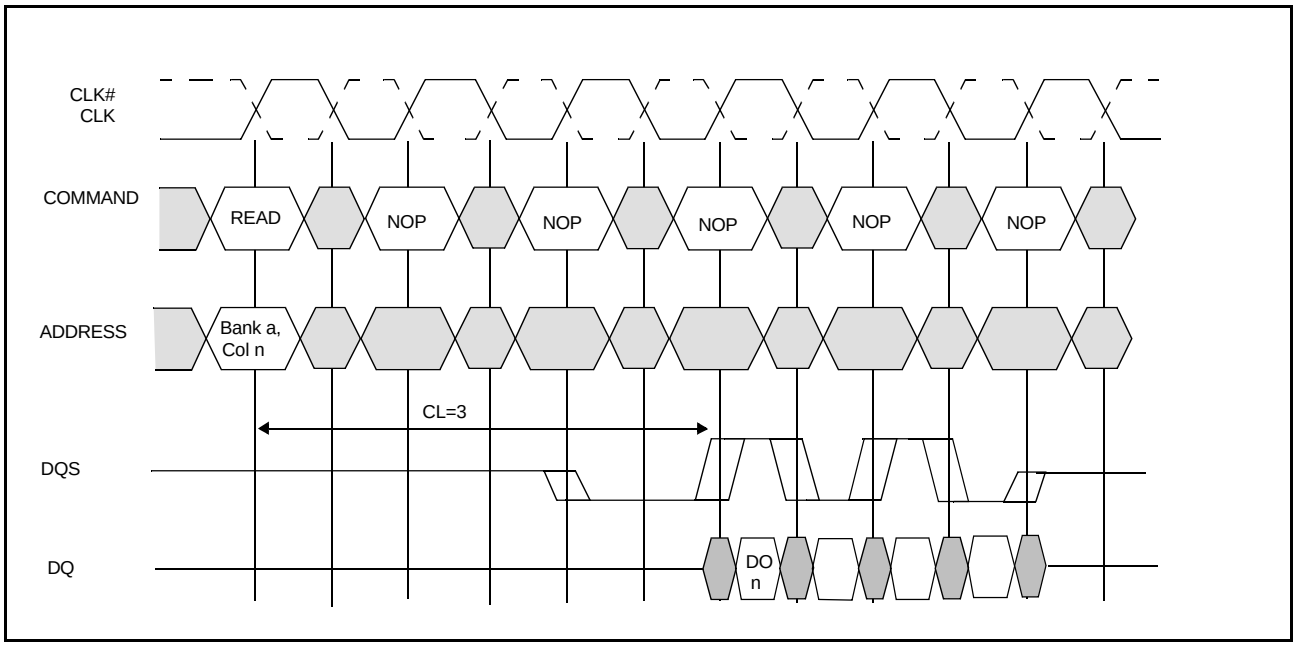




DO n=Data Out from column n
Burst Length=4
3 subsequent elements of Data Out appear in the programmed order following DO n

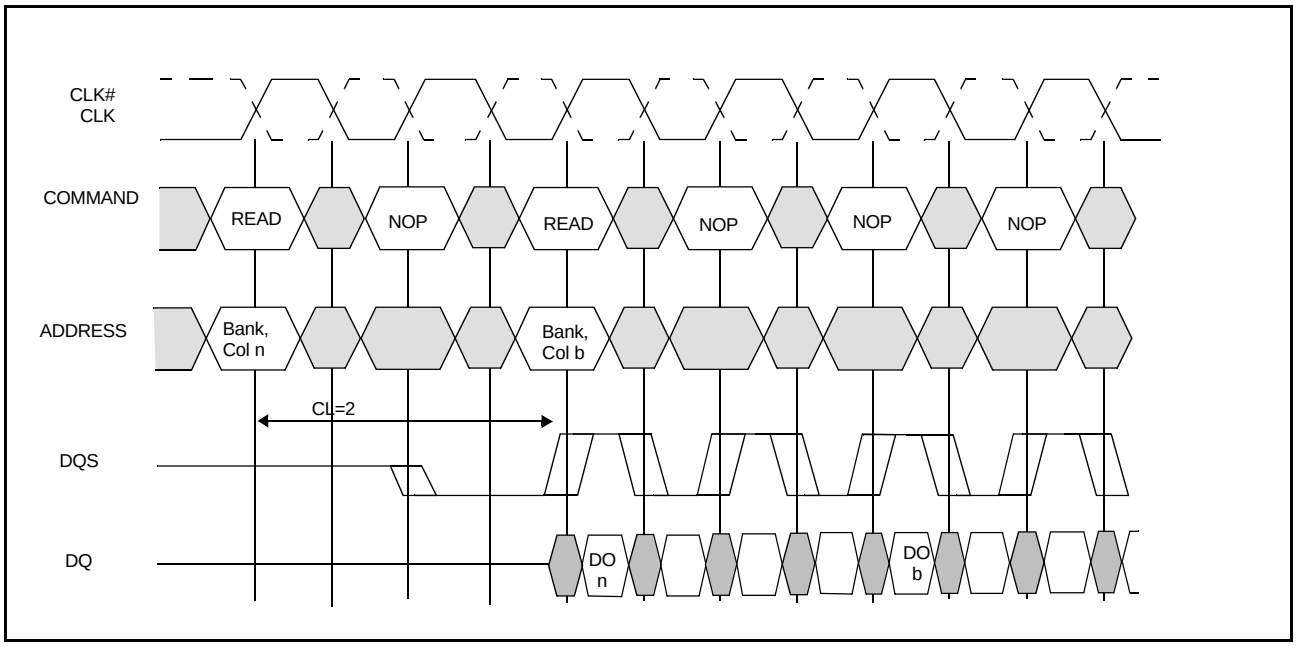
Figure 7a
READ BURST - REQUIRED CAS LATENCIES

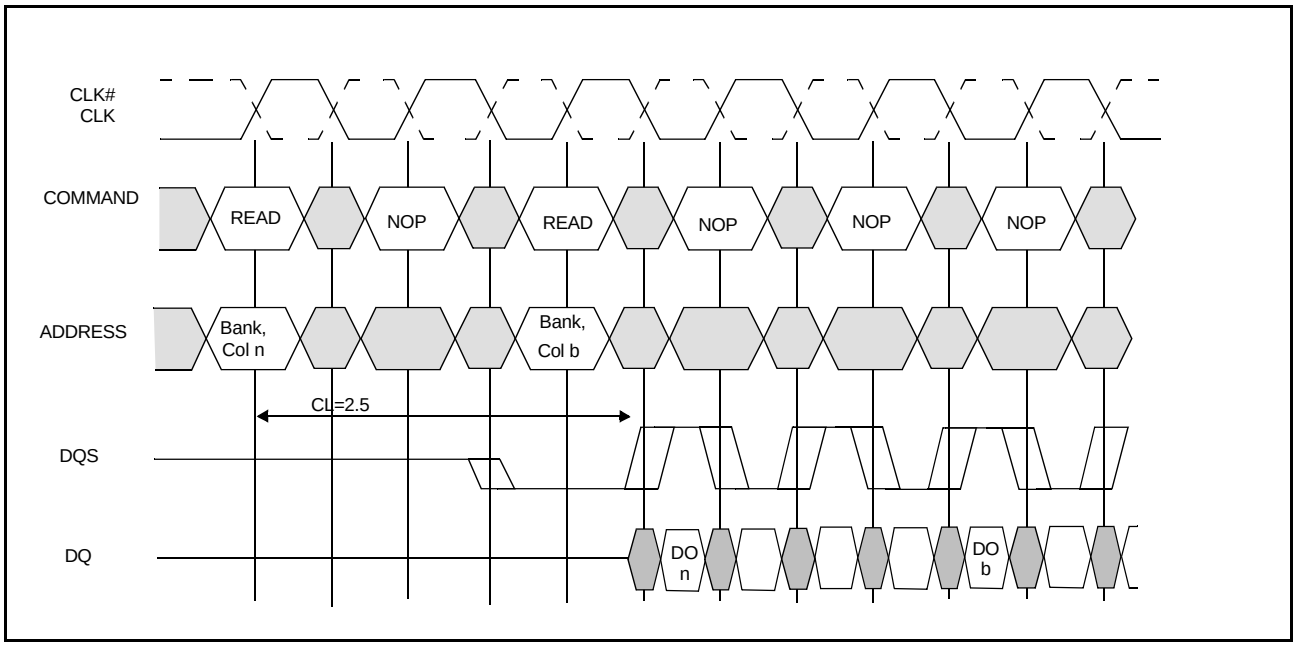


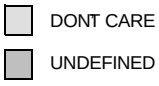


DO n=Data Out from column n
Burst Length=4
3 subsequent elements of Data Out appear in the programmed order following DO n

Figure 7b
READ BURST - OPTIONAL CAS LATENCIES

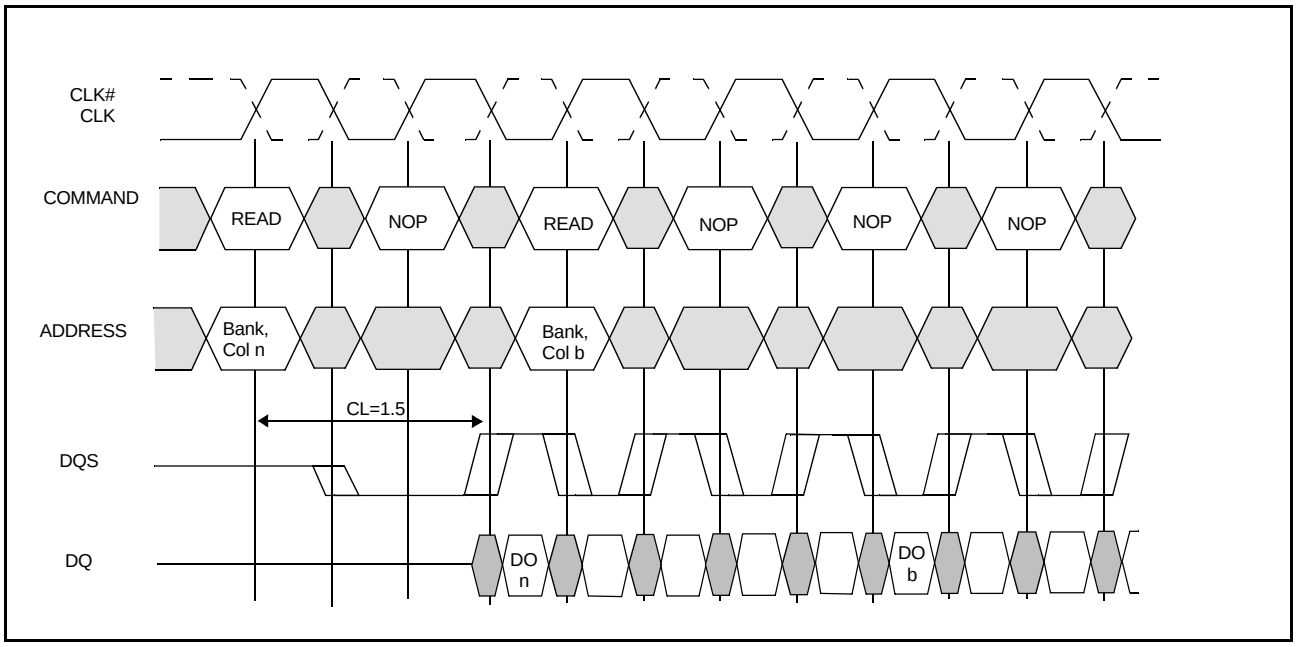


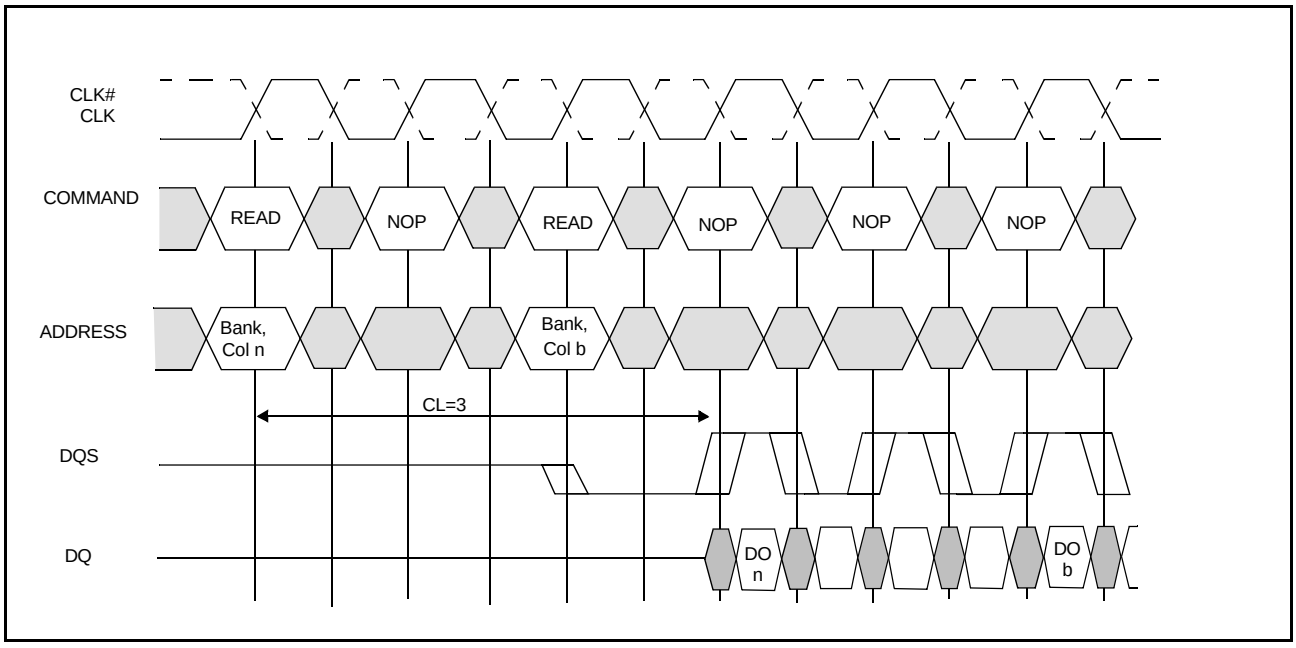


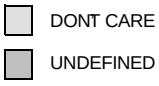


Do n(or b)= Data Out from column n (or column b)
Burst Length= 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO b

Figure 8a
CONSECUTIVE READ BURSTS - REQUIRED CAS LATENCIES

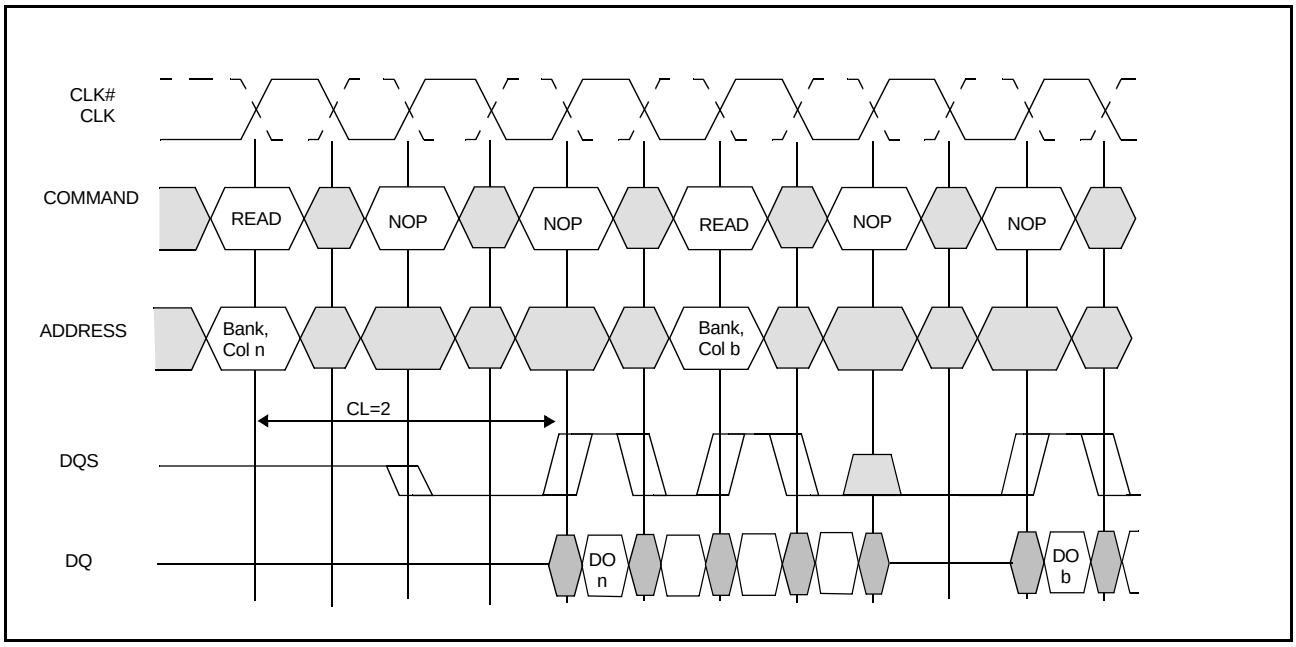


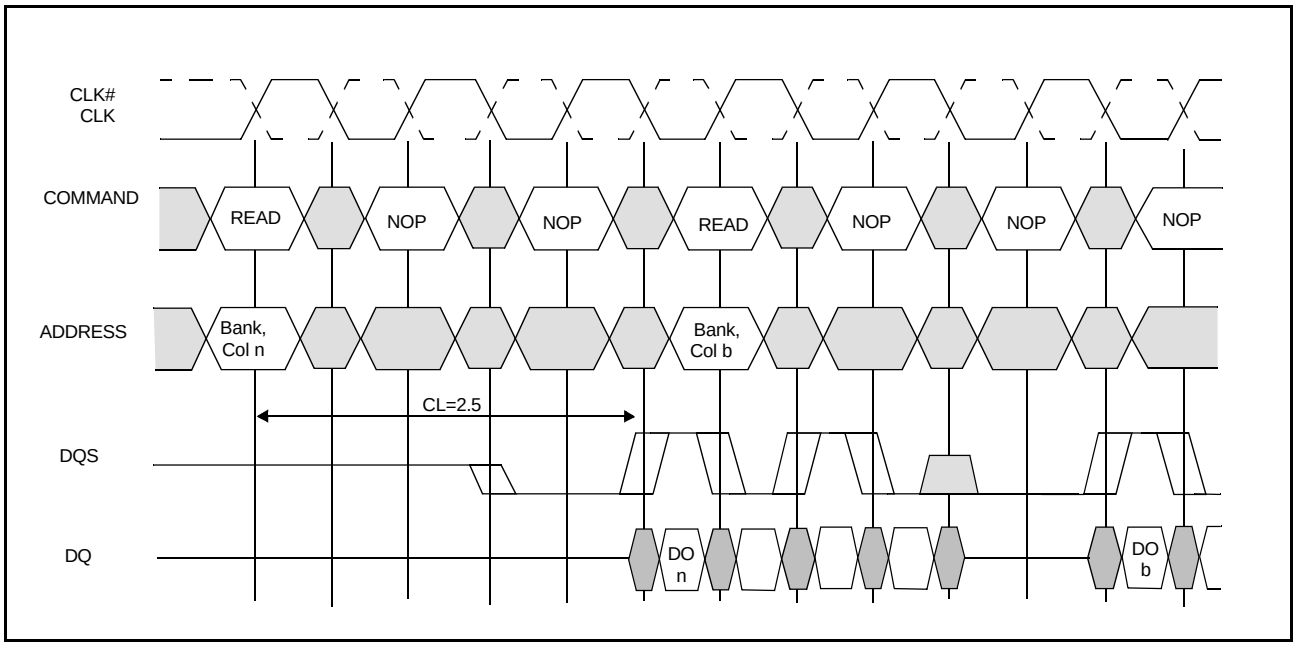




Do n(or b)= Data Out from column n (or column b)
Burst Length= 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO b

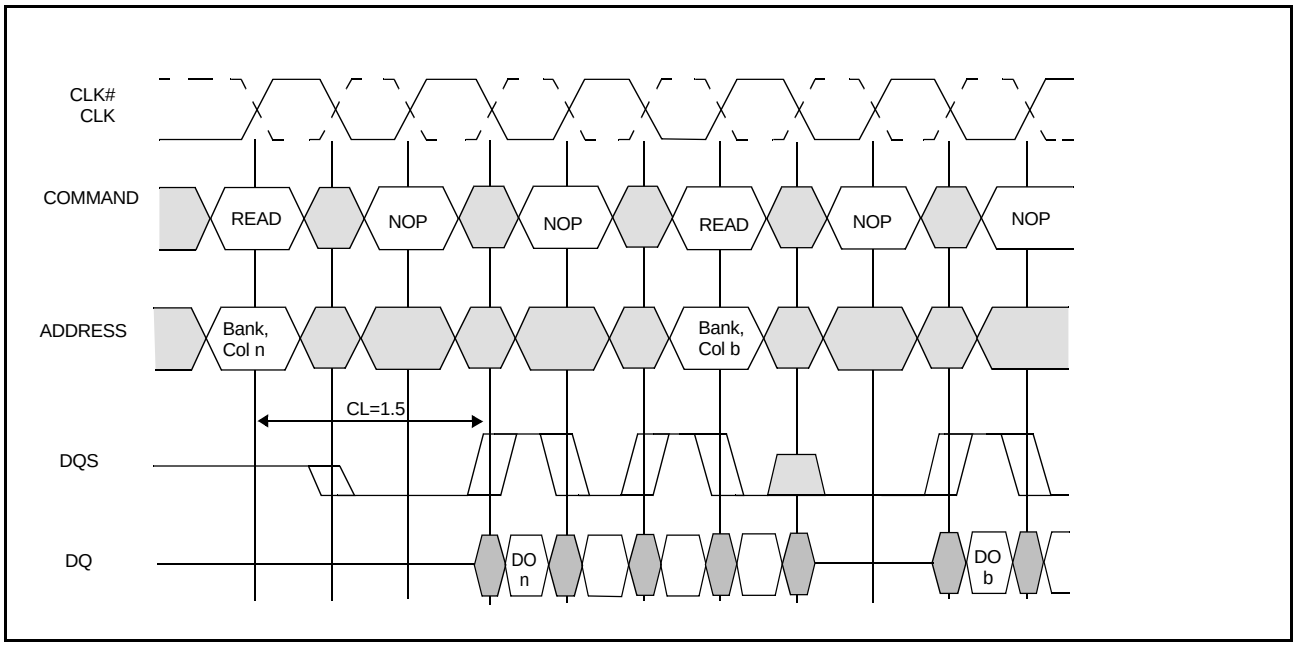
Figure 8b
CONSECUTIVE READ BURSTS - OPTIONAL CAS LATENCIES

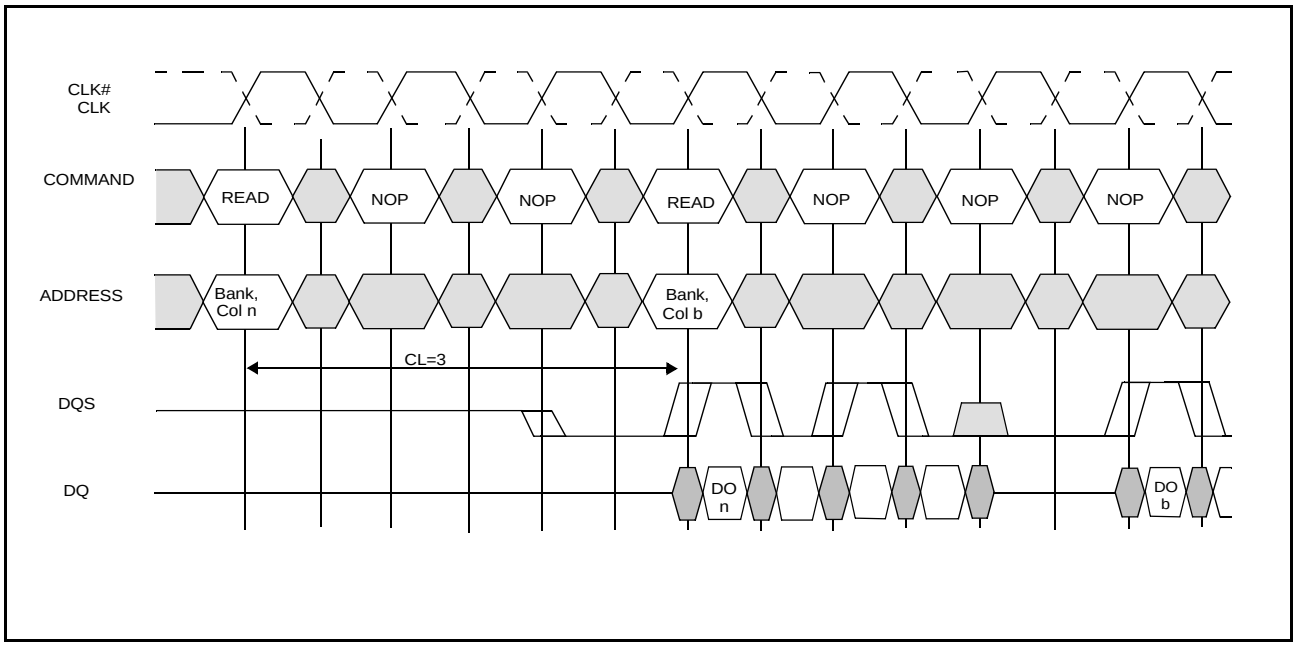




DO n(or b)=Data Out from column n (or column b)
Burst Length=4
3 Subsequent elements of Data Out appear in the programmed order following DO n(and following DO b)

Figure 9a
NON-CONSECUTIVE READ BURSTS-REQUIRED CAS LATENCIES



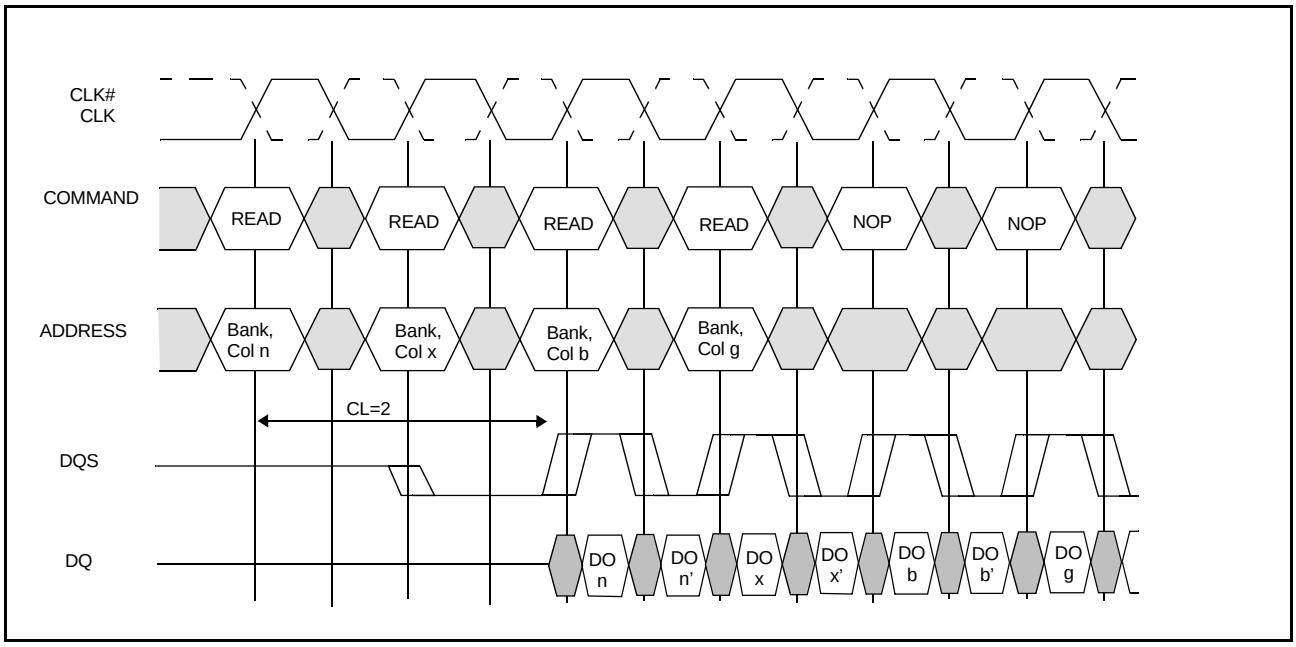


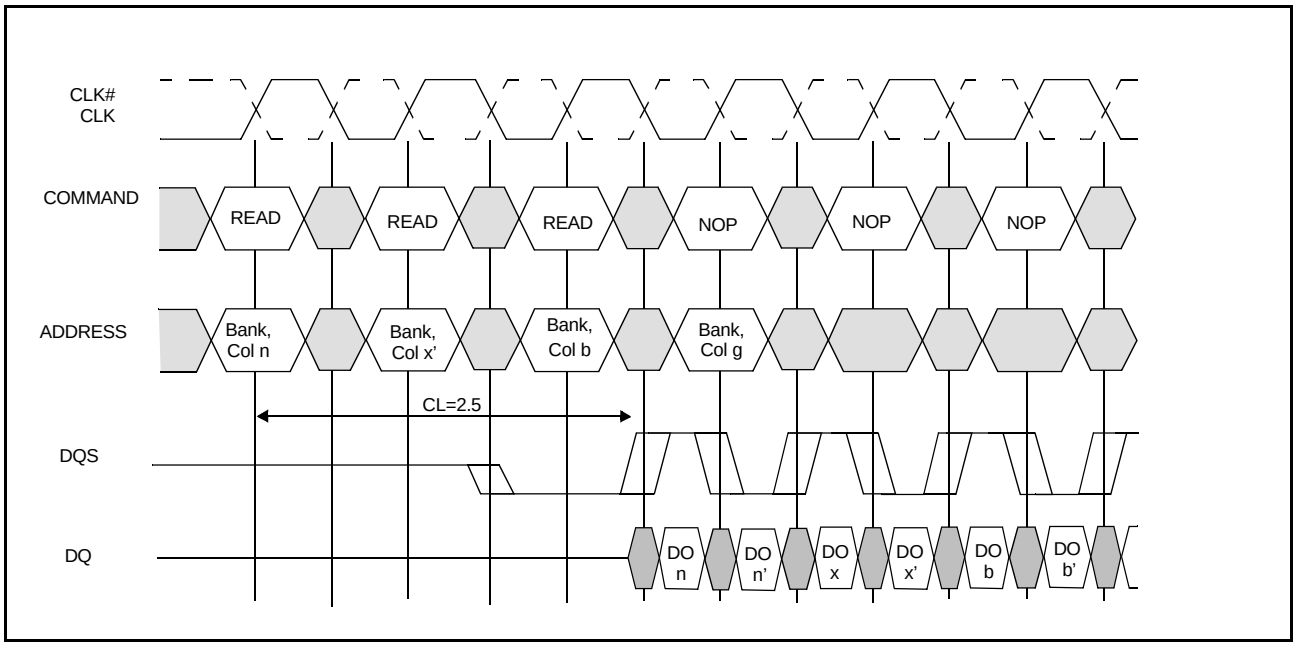
DONT CARE

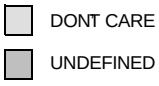
UNDEFINED

DO n(or b)=Data Out from column n (or column b)
Burst Length=4
3 Subsequent elements of Data Out appear in the programmed order following DO n(and following DO b)

Figure 9b
NON-CONSECUTIVE READ BURSTS-OPTIONAL CAS LATENCIES

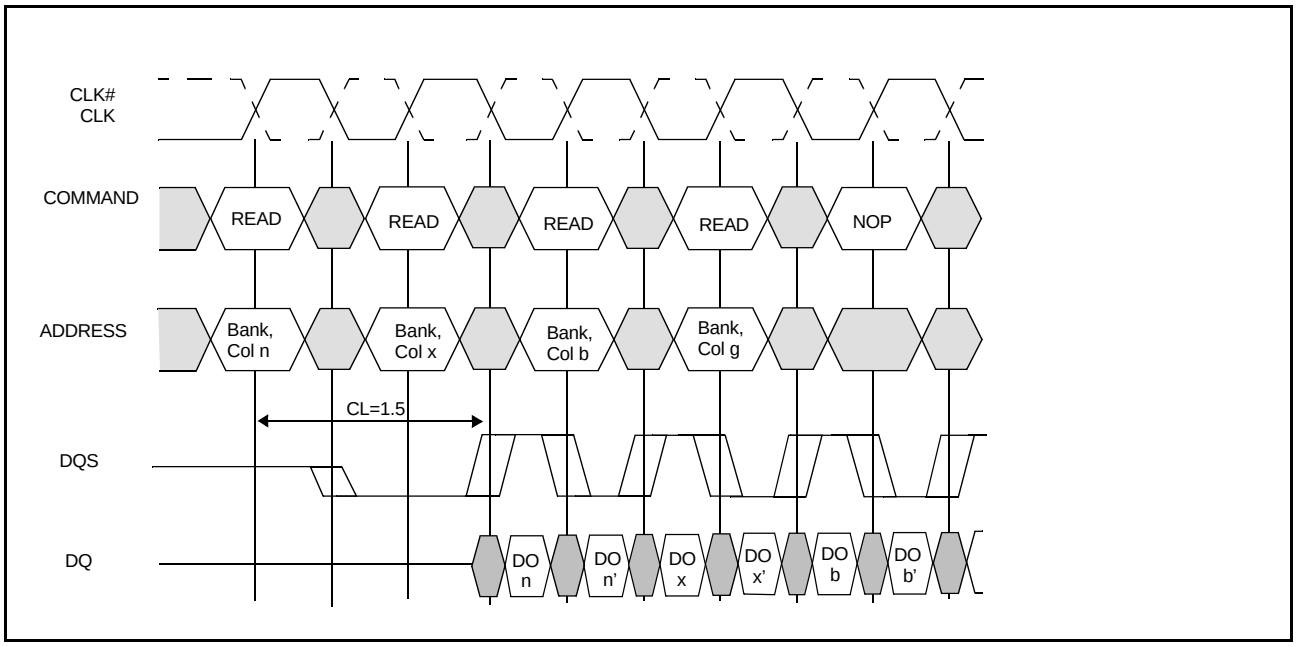


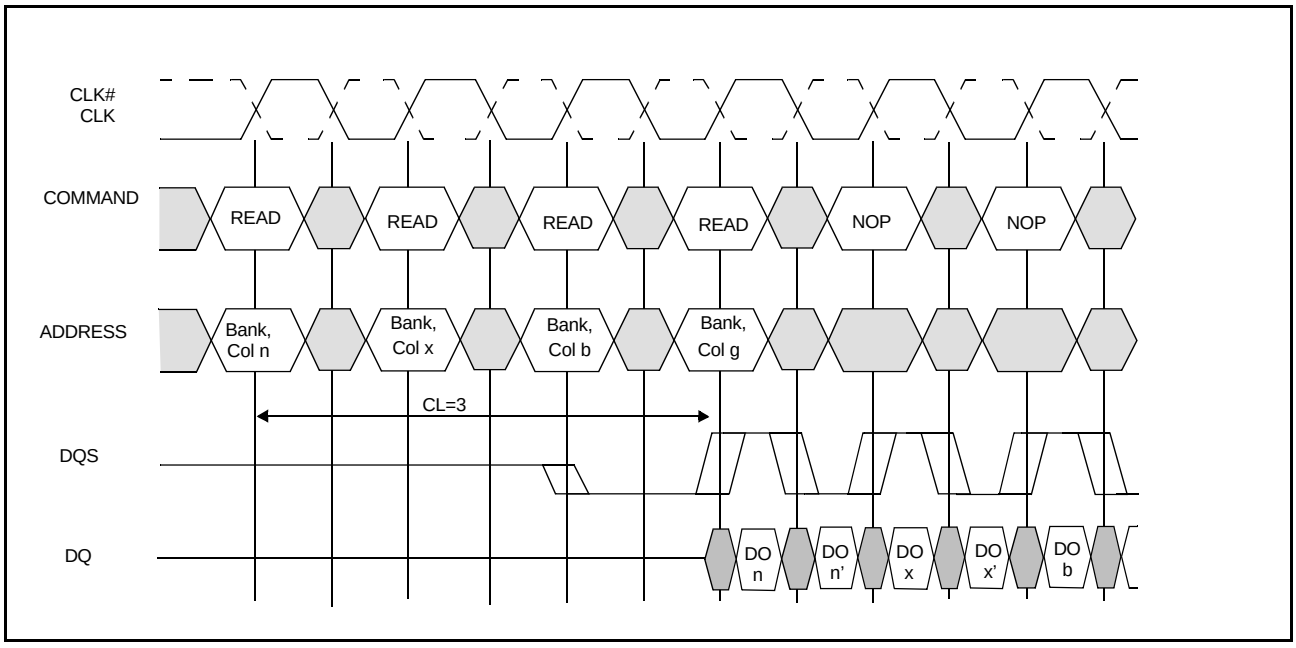




DO n, etc.= Data Out from column n, etc.
n', etc.=odd or even complement of n, etc. (i.e. column address LSB inverted)
Burst Length=2,4 or 8 in cases shown
Reads are to active rows in any banks

Figure 10a
RANDOM READ ACCESSES - REQUIRED CAS LATENCIES





DONT CARE

UNDEFINED

DO n, etc.= Data Out from column n, etc.
n', etc.=odd or even complement of n, etc. (i.e. column address LSB inverted)
Burst Length=2,4 or 8 in cases shown
Reads are to active rows in any banks

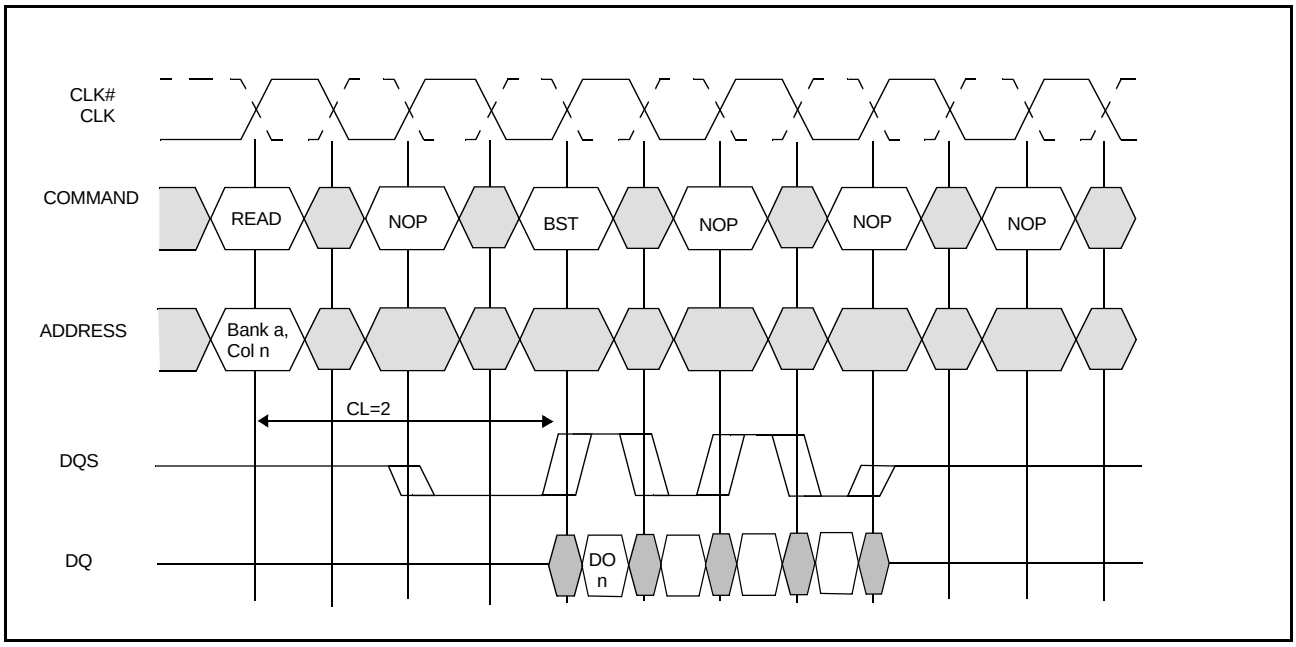
Figure 10b
RANDOM READ ACCESSES - OPTIONAL CAS LATENCIES

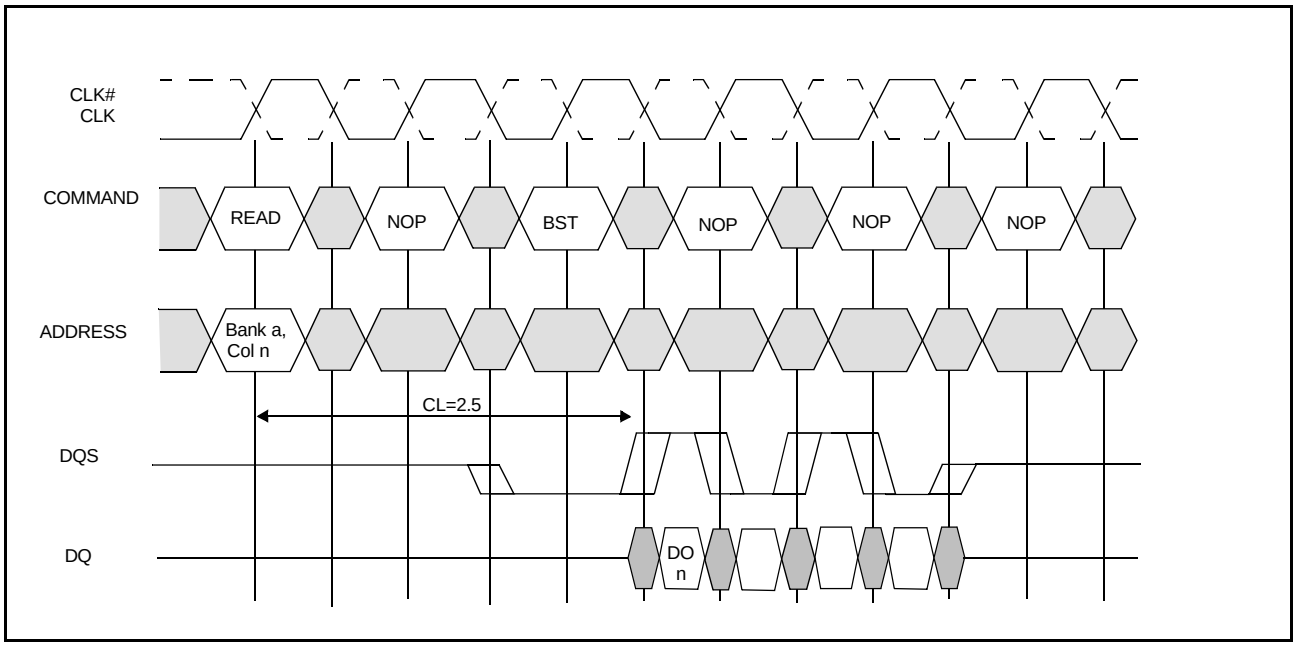
Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 11. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e. the BURST TERMINATE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture).

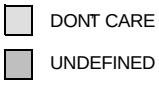
Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 12. The tDDS MIN case is shown; the tDDS MAX case has a longer bus idle time (tDDS MIN and tDDS MAX are defined in the section on WRITEs).

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that AUTO PRECHARGE was not activated). The PRECHARGE command should be issued x cycles after the READ command, where x equals the number of desired data element paires (pairs are required by the 2n prefetch architecture). This is shown if Figure 13 for READ latencies of 2.2.5 and 3. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. Note that part of the row precharge time is hidden during the access of the last data elements.

In the case of a READ being executed to completion. a PRECHARGE command issued at the optimum time (asdescribed above) provides the same operation that would result from the same READ burst with AUTO PRECHARGE enabled. The disadvantage of the precharge command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.

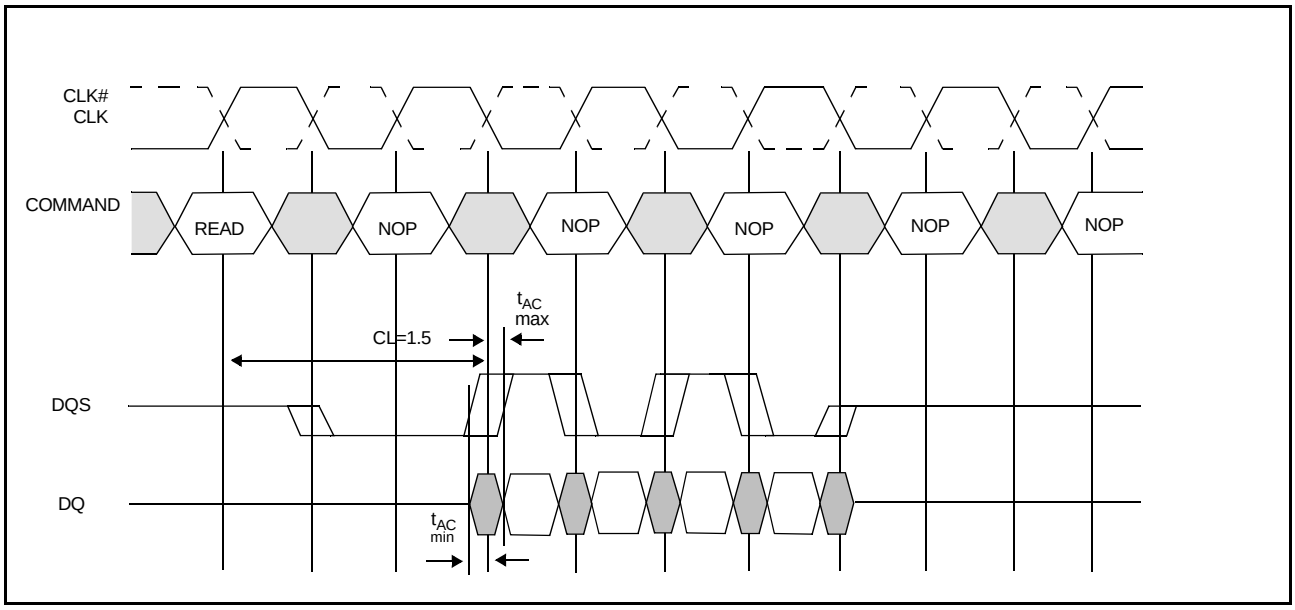


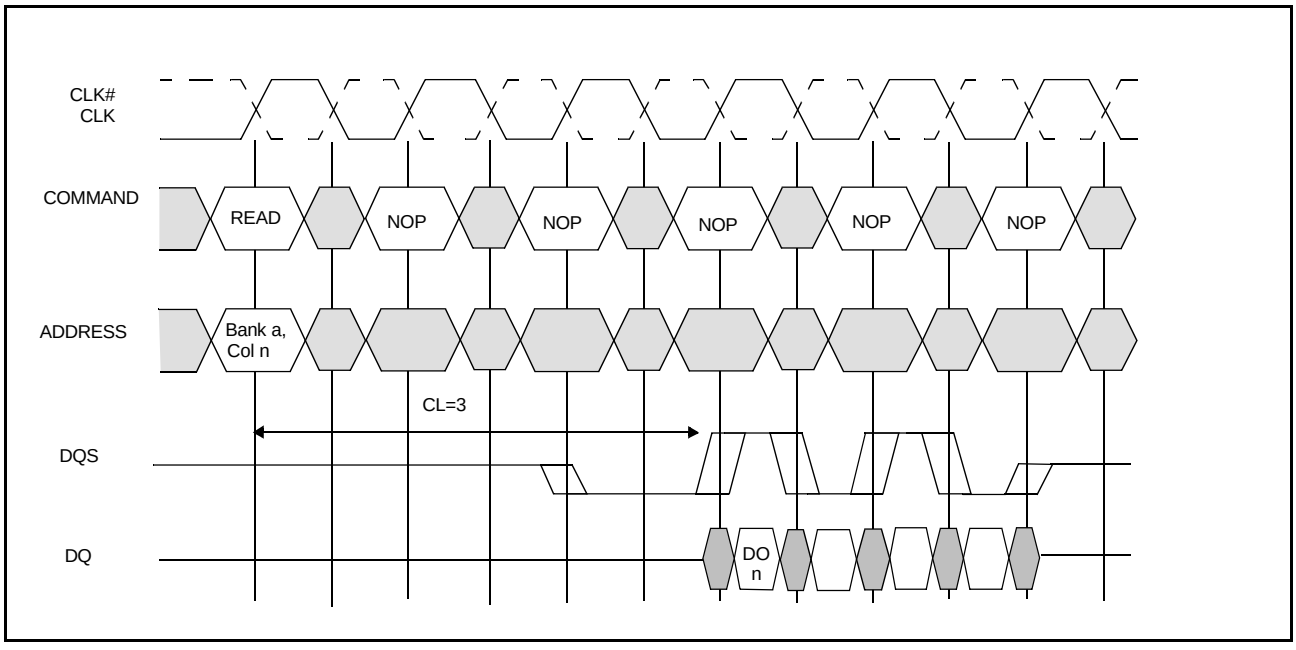




DO n=Data Out from column n
Cases shown are bursts of 8 terminated after 4 data elements
3 subsequent elements of Data Out appear in the programmed order following DO n

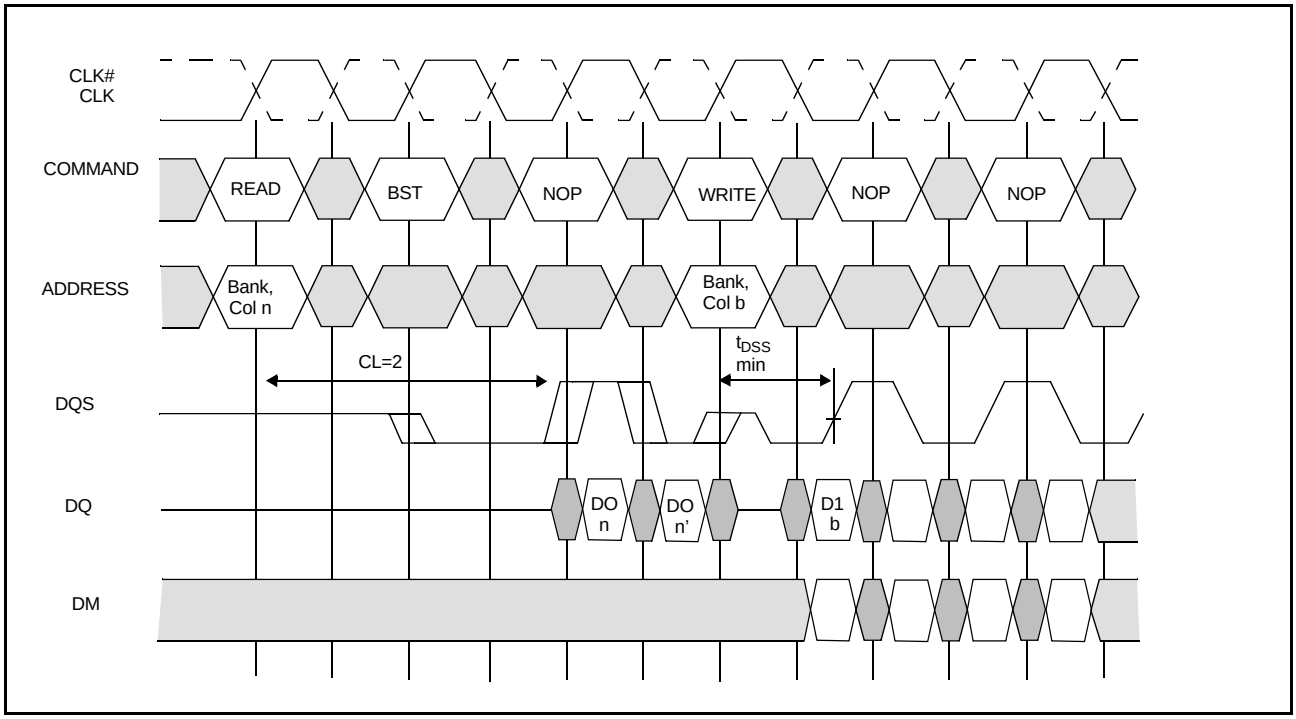
Figure 11a
TERMINATING A READ BURST - REQUIRED CAS LATENCIES

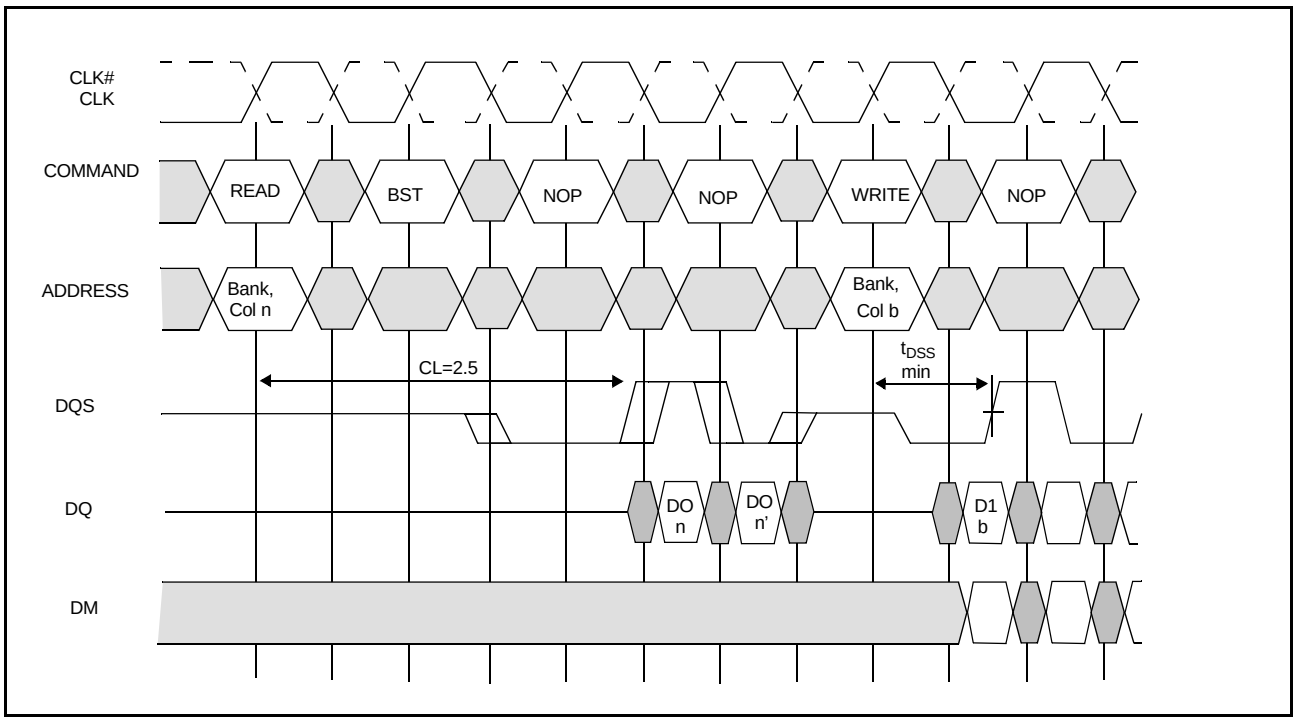




DO n= Data Out from coulmn n
Burst Length=4
3 subsequent elements of Data Out appear in the programmed order following DO n

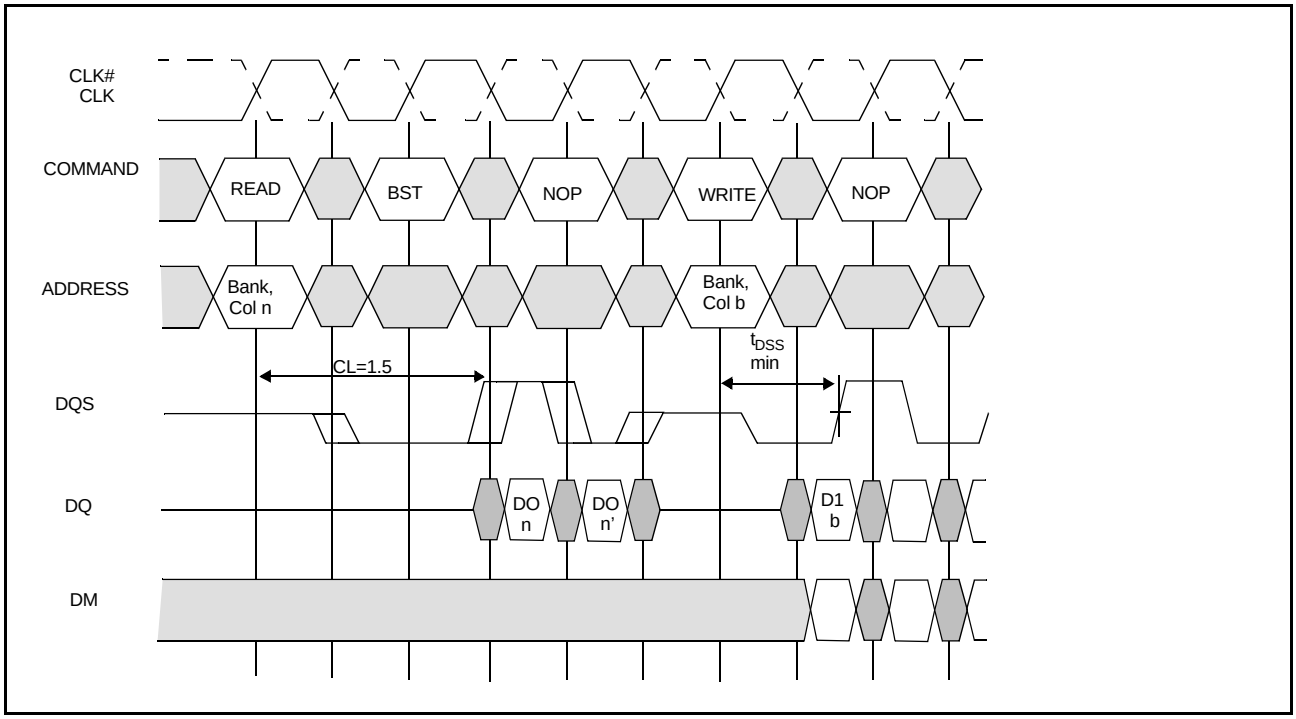
Figure 11b
TERMINATING A READ BURST - OPTIONAL CAS LATENCIES

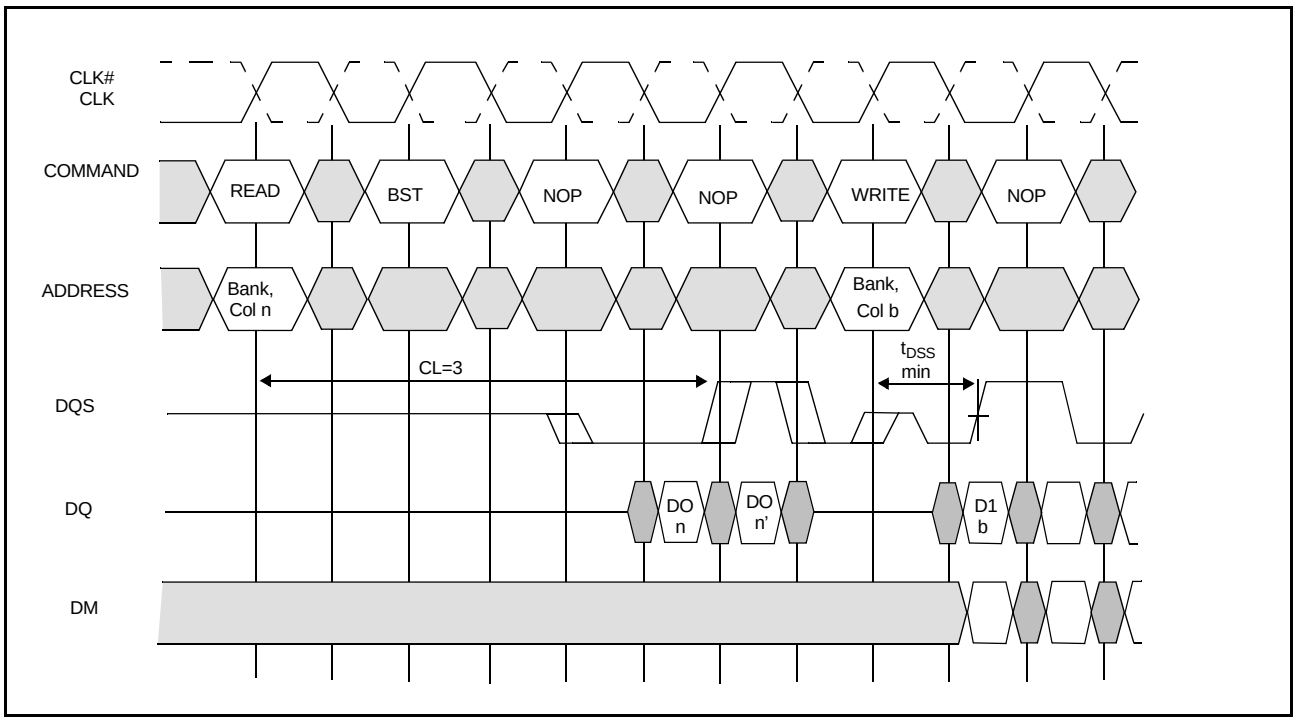




DO n(or b)=Data Out from column n (or column b)
Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)
3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO b)

Figure 12a
READ TO WRITE - REQUIRED CAS LATENCIES



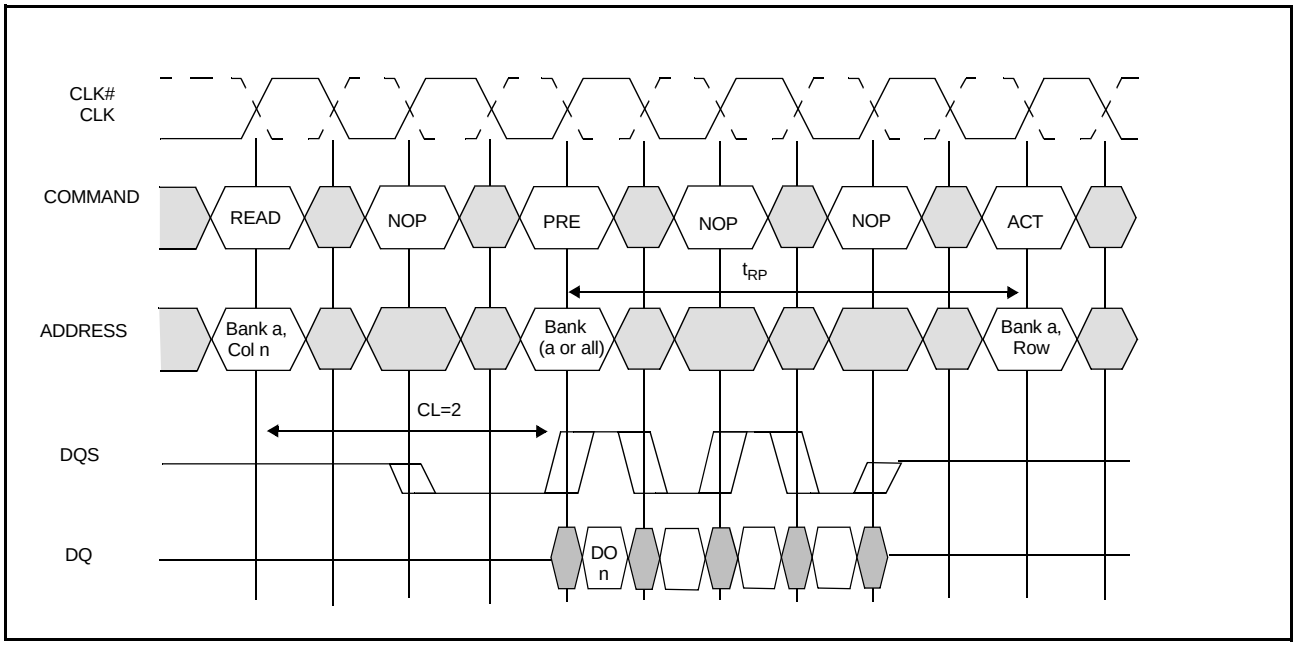


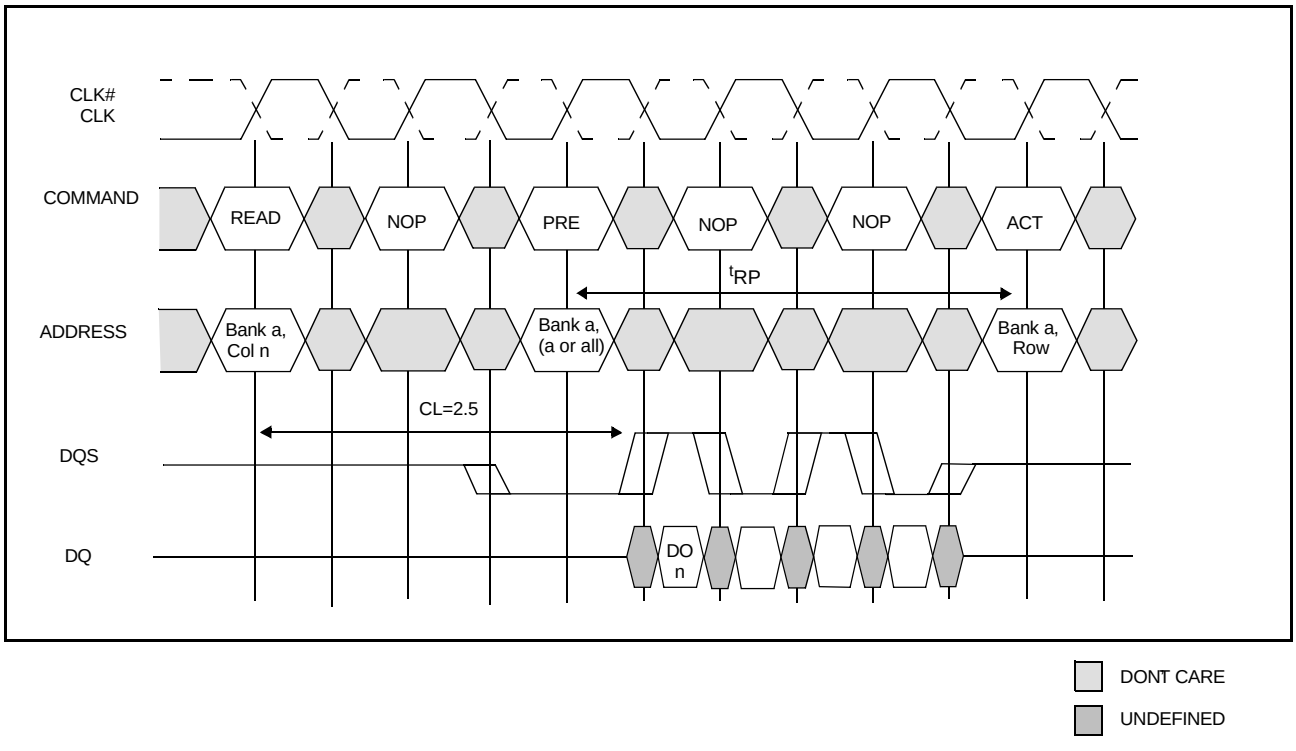
DONT CARE

UNDEFINED

DO n(or b)=Data Out column n (or column b)
Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)
3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO b)

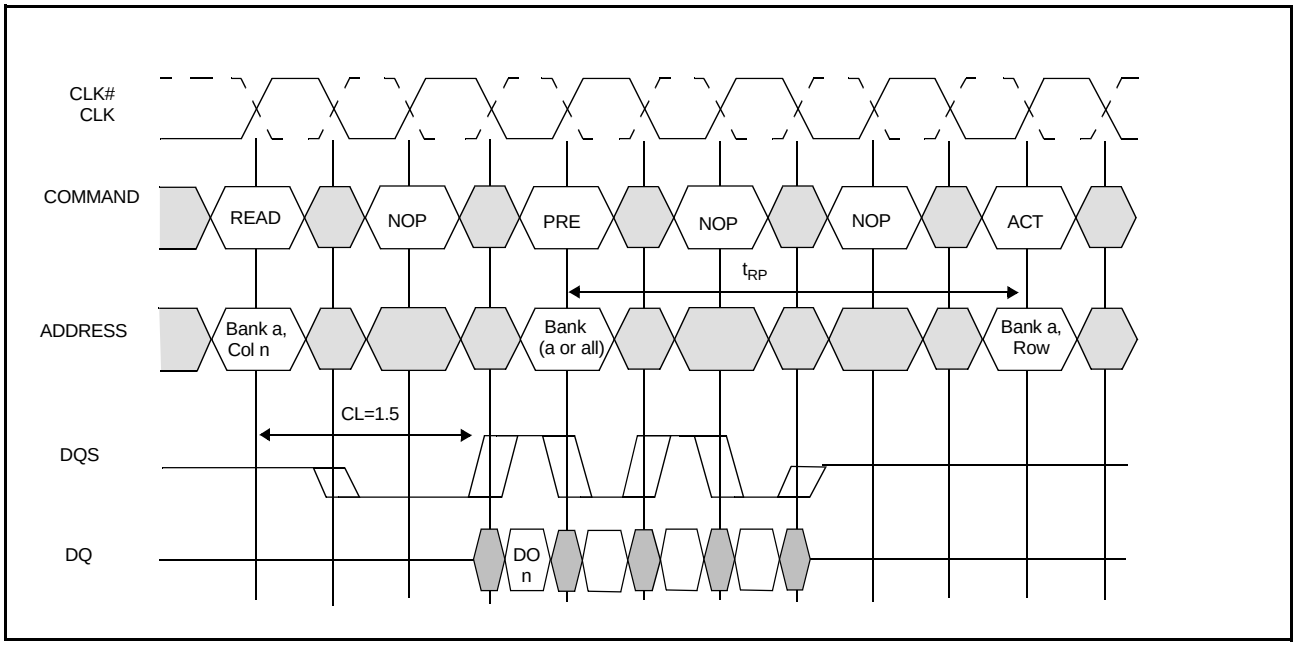
Figure 12b
READ TO WRITE -OPTIONAL CAS LATENCIES

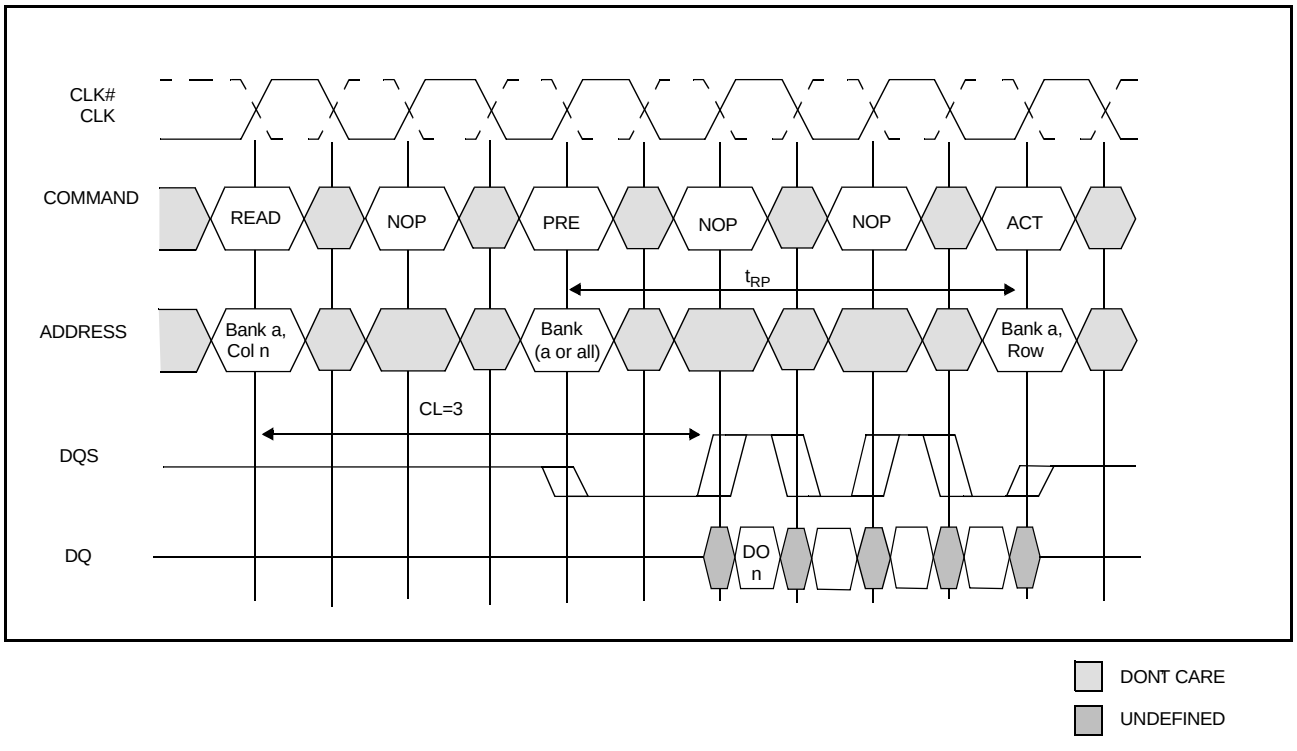




DO n=Data Out from column n
Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8
3 subsequent elements of Data Out appear in the programmed order following DO n

Figure 13a
READ TO PRECHARGE - REQUIRED CAS LATENCIES





DO n=Data Out from column n
Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8
3 subsequent elements of Data Out appear in the programmed order following DO n

Figure 13b
READ TO PRECHARGE - OPTIONAL CAS LATENCIES

WRITEs

WRITE bursts are initiated with a WRITE command, as shown in figure 14.

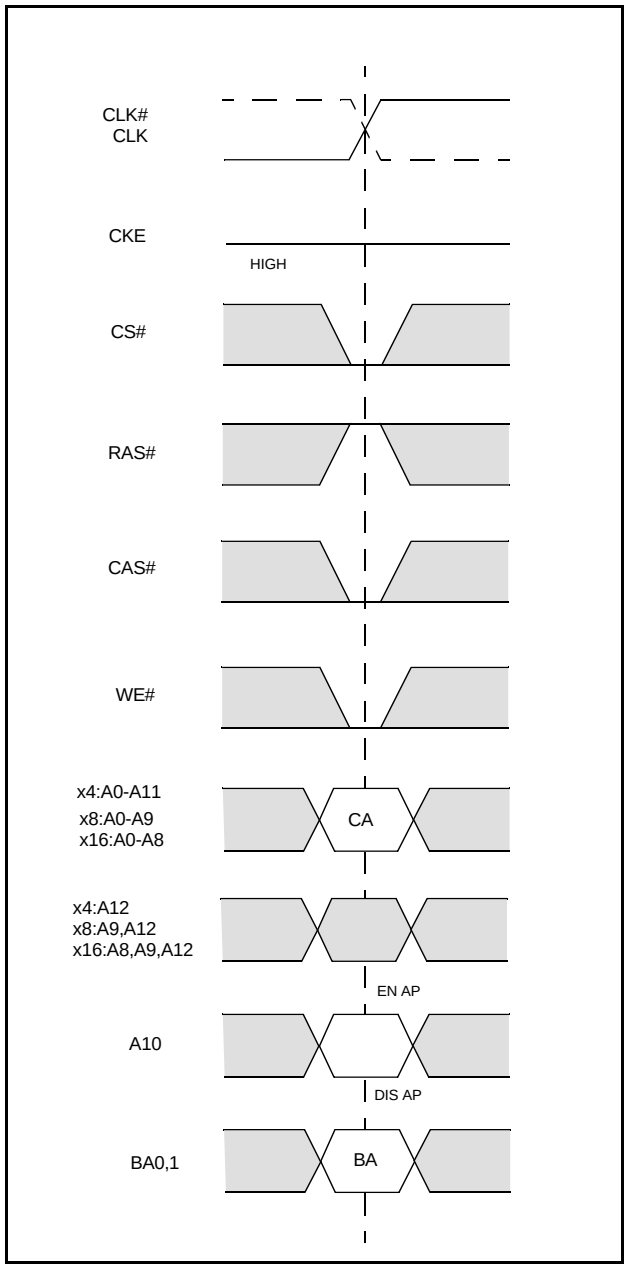
The starting column and bank addresses are provided with the WRITE command, and AUTO PRECHARGE is either enabled or disabled for that acess. If AUTOPRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, AUTOPRECHARGE is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the write command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble. The time between the WRITE command and the first corresponding rising edge of DQS (tDSS) is specified with a relatively wide range (from 75% to 125% of 1 clock cycle), so most of the WRITE diagrams that follow are drawn for the two extreme cases (i.e. tDSS MIN and tDSS MAX). Figures 15 and 16 show the two extremes of tDSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued x cycles after the first WRITE command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). Figures 17 and 18 show concatenated bursts of 4. An example of non-consecutive WRITEs is shown in Figure 19. Full-speed random write accesses within a page or pages can be performed as shown in Figures 20 and 21.

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the write burst, tWTR should be met as shown in Figures 22 and 23.

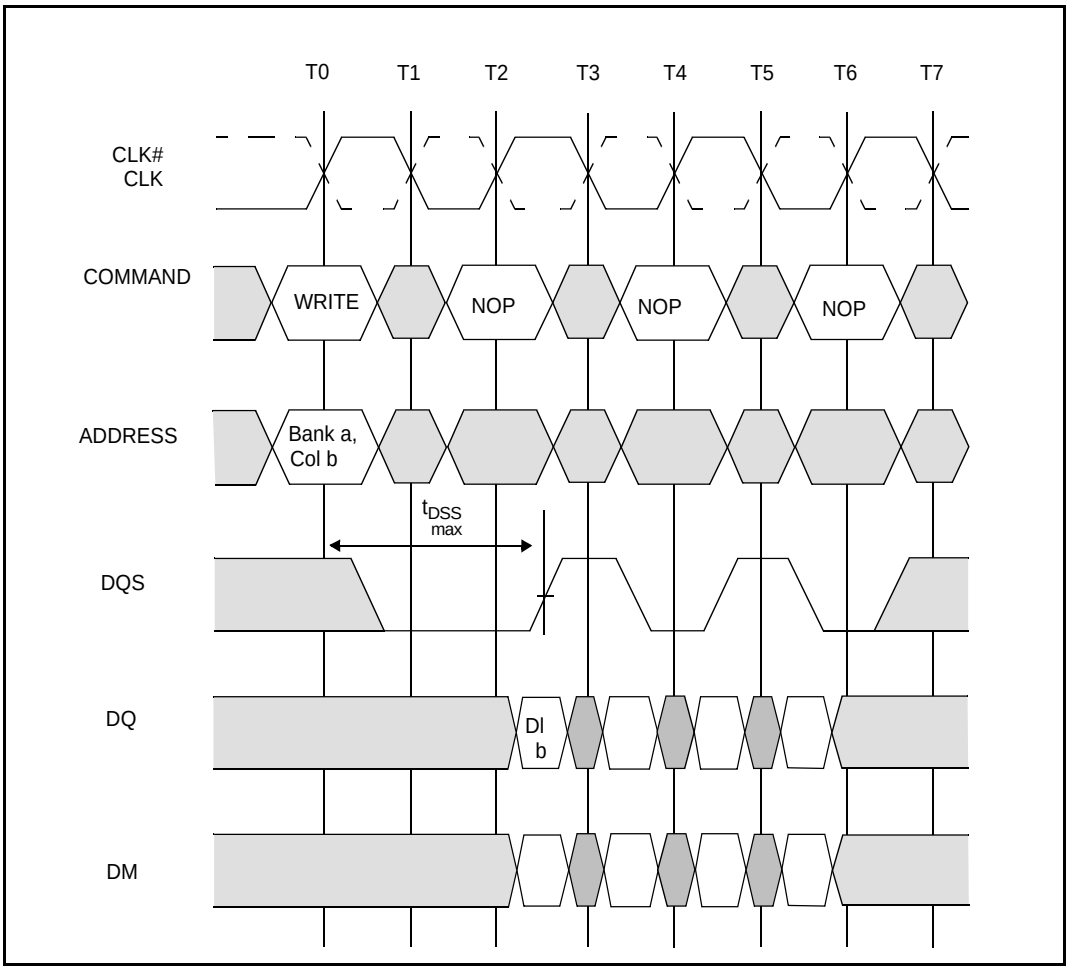
Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figures 24-27. Note that only the data-in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data-in should be masked with DM(through one-half clock after the READ command).



=DONT CARE

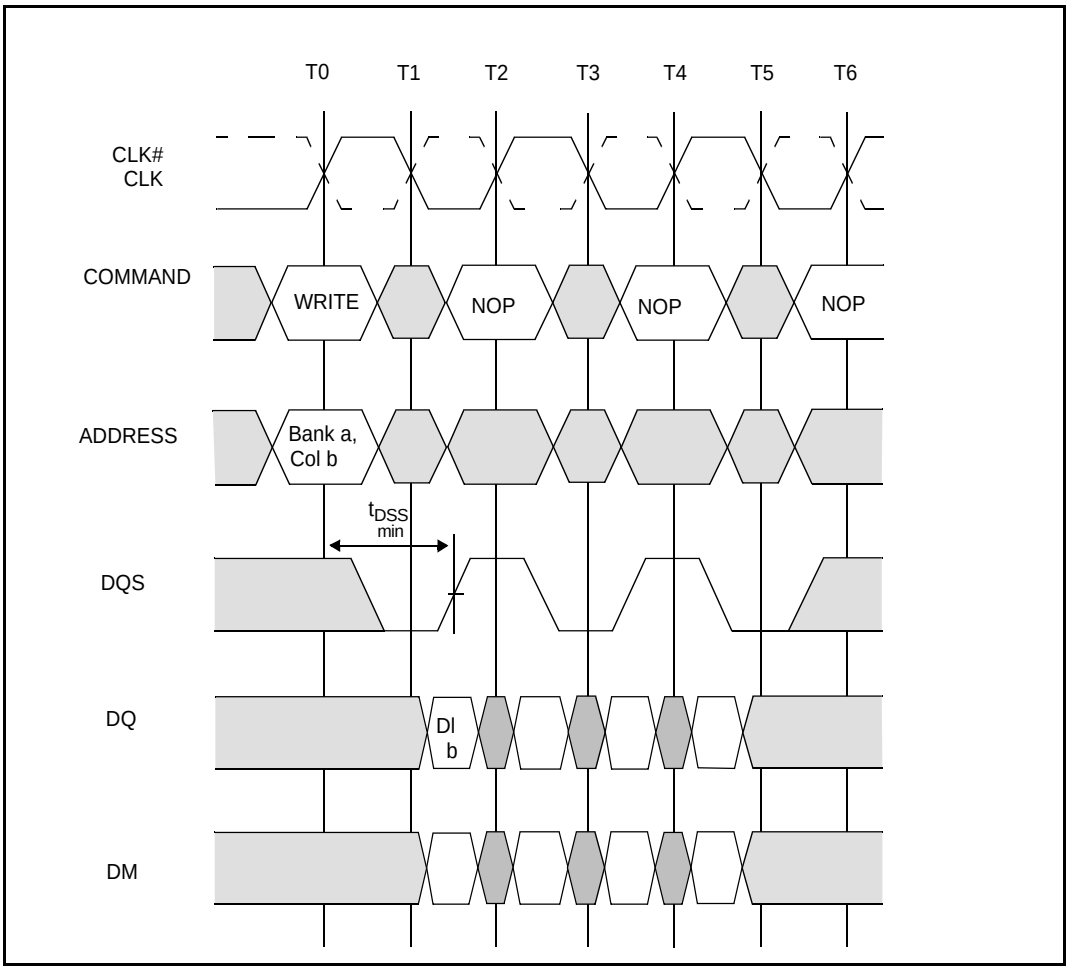
CA = Column Address
BA = Bank Address
EN AP = Enable Autoprecharge
DIS AP = Disable Autoprecharge

Figure 14
WRITE COMMAND



Dl b=Data In for column b
3 subsequent elements of Data In are applied in the programmed order following Dl b
A non-interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 15
WRITE BURST - MAX DSS



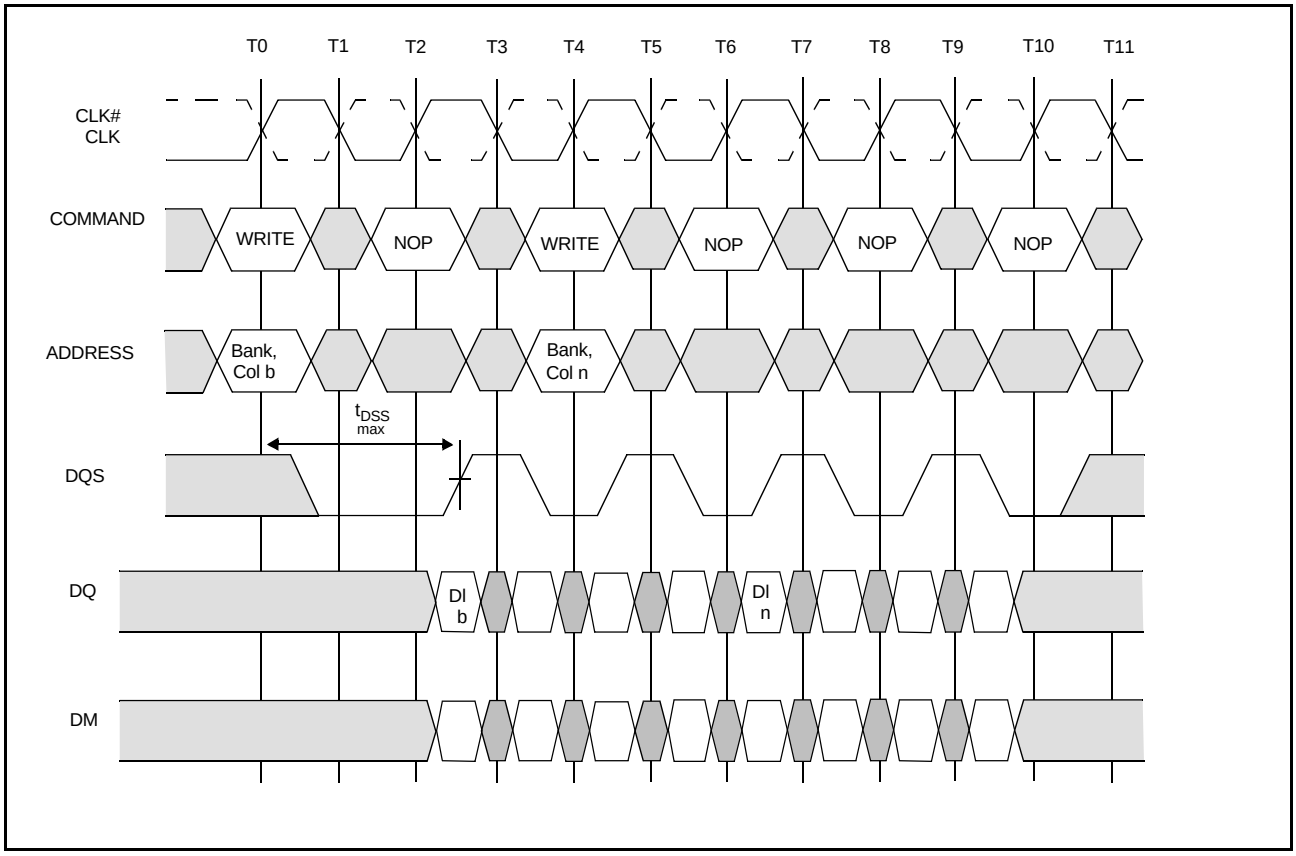
Dl b=Data In for column b
3 subsequent elements of Data In are applied in the programmed order following Dl b
A non-interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 16
WRITE BURST - MIN DSS

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE with out truncating the write burst, tWR should be met as shown in Figures 28 and 29.

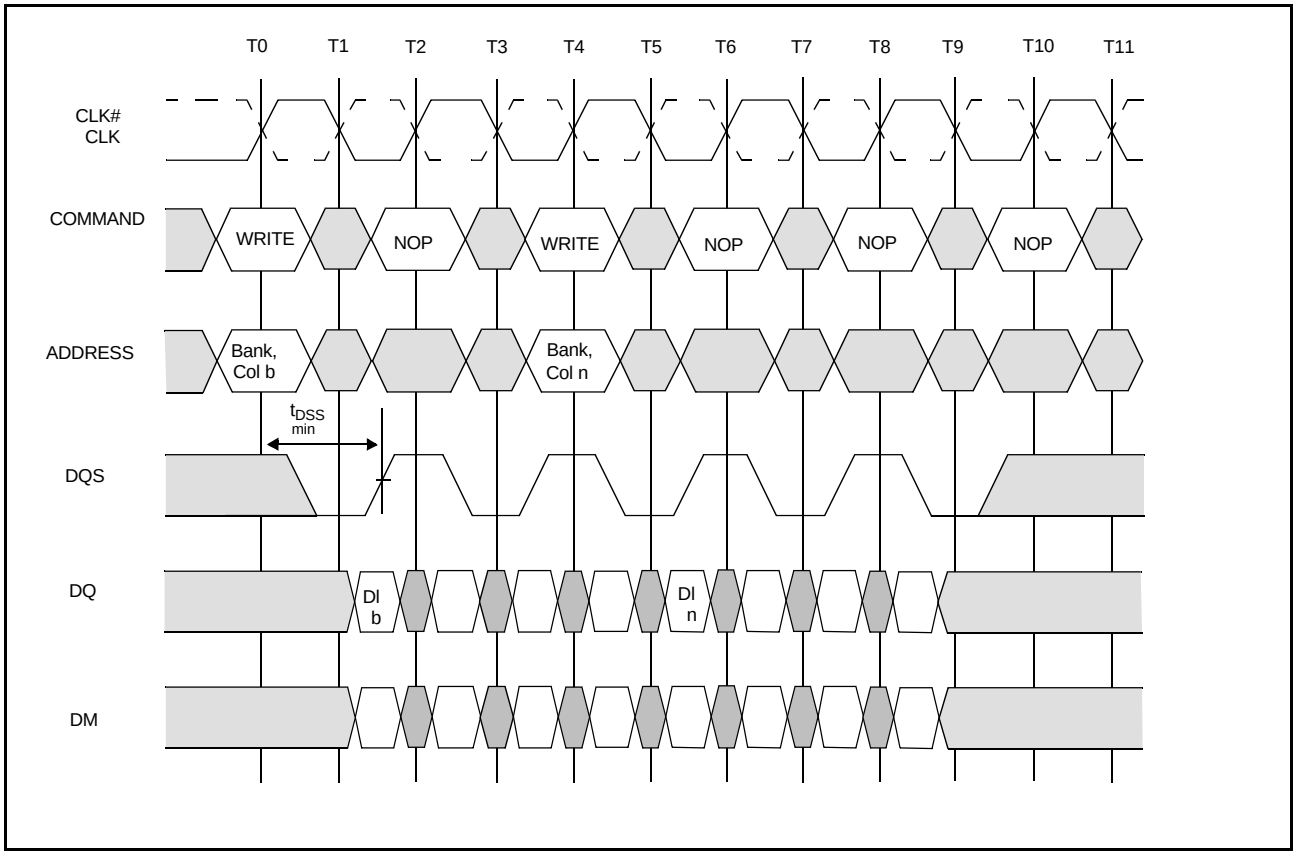
Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figures 30-33. Note that only the data -in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data-in should be masked with DM (through one-half clock after the READ command). Following the PRECHARGE command, a subsequent command to the same bank can not be issued until tRP is met.

In the case of a write burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same burst with AUTO PRECHARGE. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.



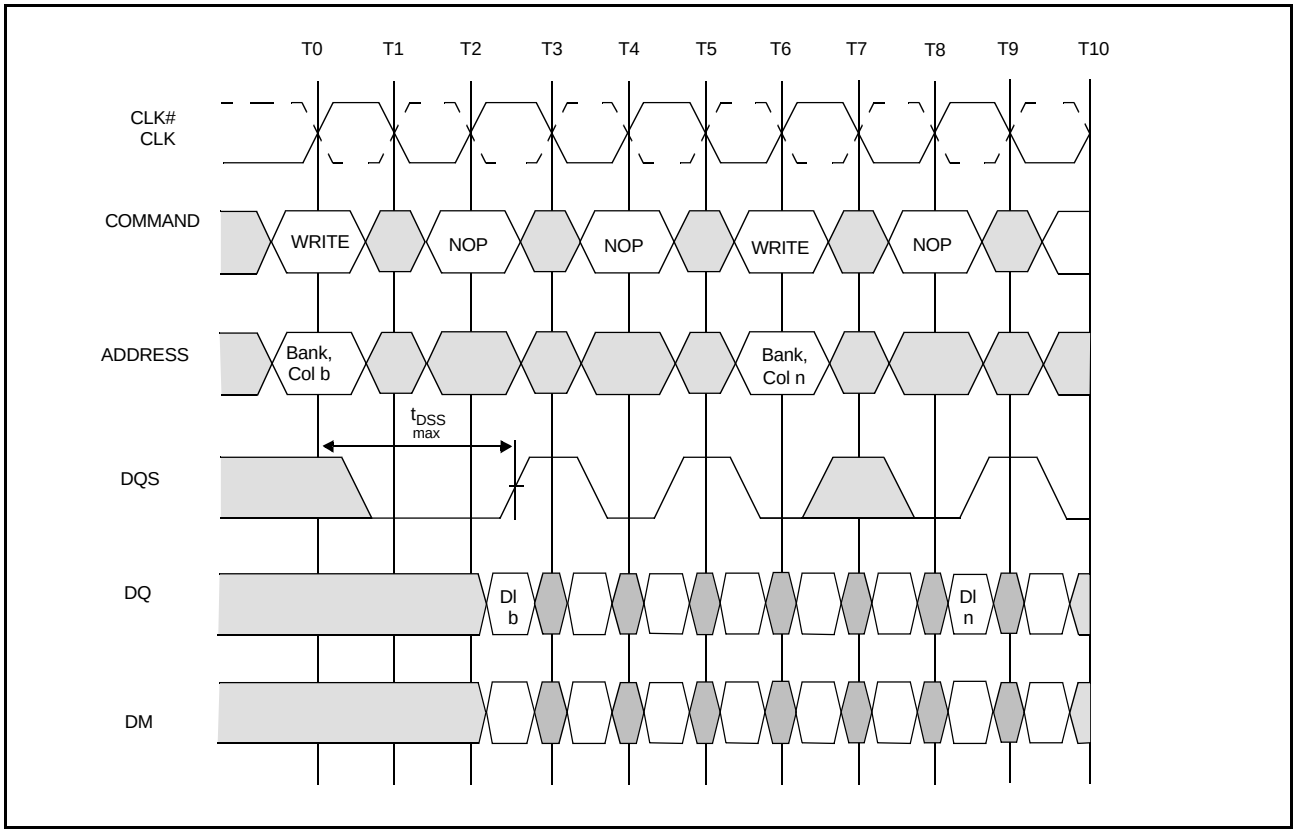
DI b, etc. = Data In for column b, etc.
3 subsequent elements of Data In are applied in the programmed order following DI b
3 subsequent elements of Data In are applied in the programmed order following DI n
A non-interrupted burst of 4 is shown
Each Write command may be to any bank

Figure 17
WRITE TO WRITE - MAX DSS



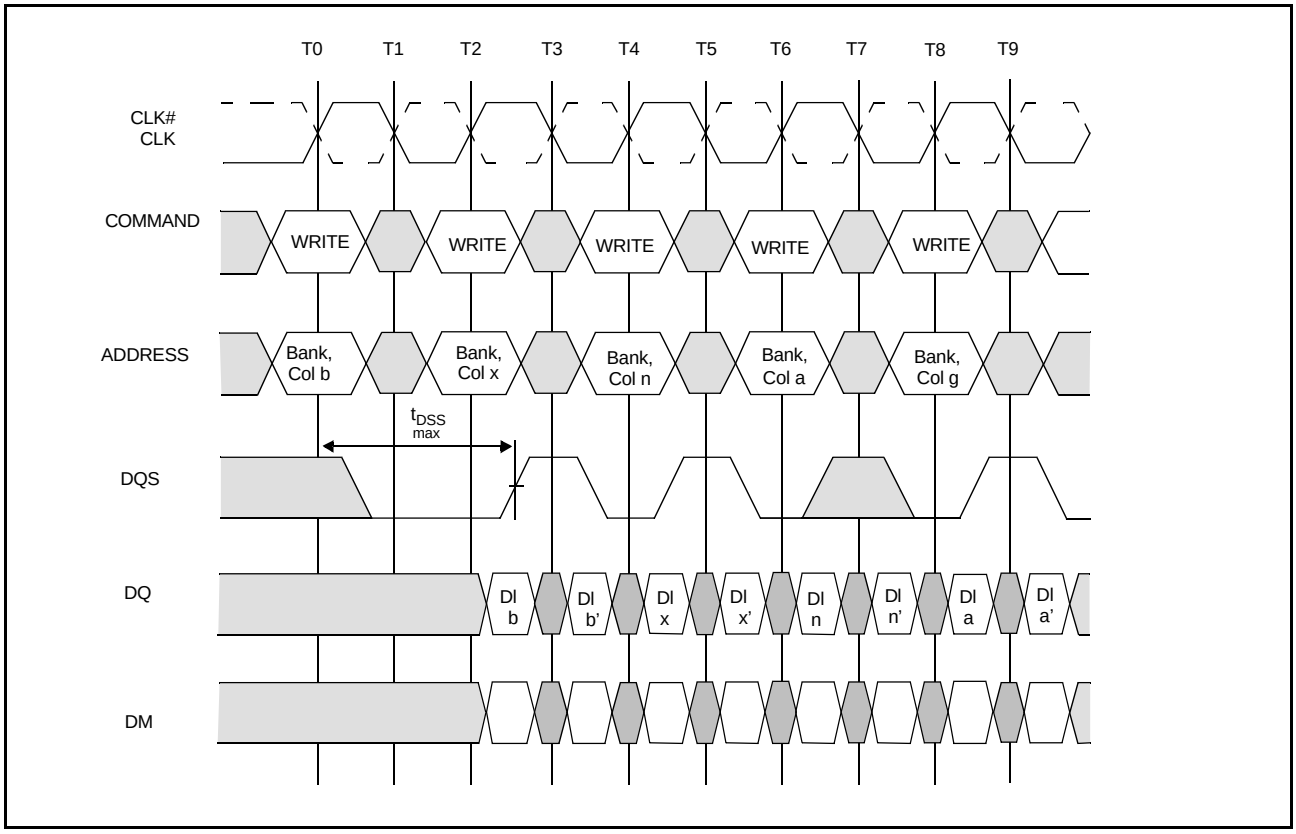
Dl b, etc. = Data In for column b, etc.
3 subsequent elements of Data In are applied in the programmed order following Dl b
3 subsequent elements of Data In are applied in the programmed order following Dl n
A non-interrupted burst of 4 is shown
Each Write command may be to any bank

Figure 18
WRITE TO WRITE - MIN DSS



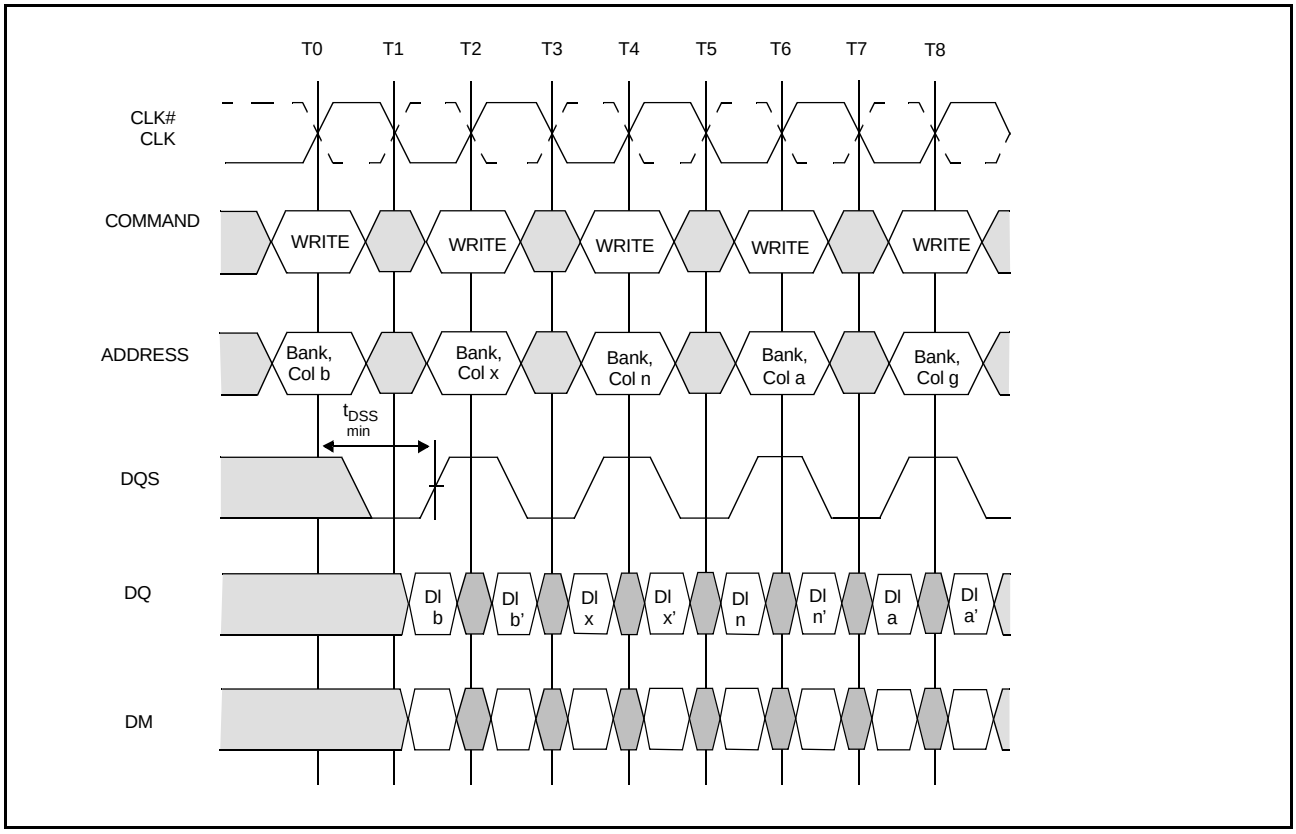
DI b, etc. = Data In for column b, etc.
3 subsequent elements of Data In are applied in the programmed order following DI b
3 subsequent elements of Data In are applied in the programmed order following DI n
A non-iterrupted burst of 4 is shown
Each Write command may be to any bank

Figure 19
WRITE TO WRITE - MAX DSS, NON-CONSECUTIVE



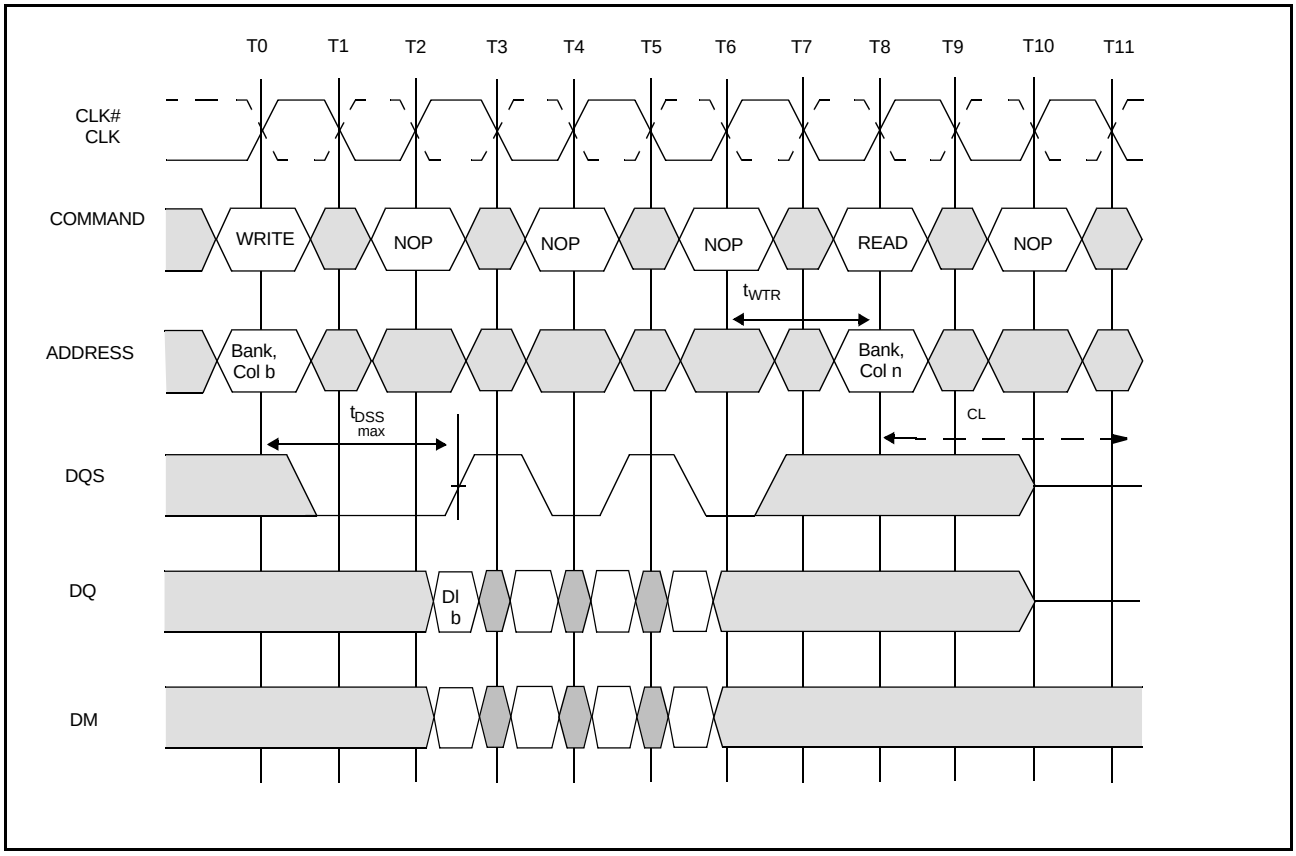
DI b, etc.=Data In for coulmn b, etc.
b',etc.=odd or even complement of b, etc.(i.e. column address LSB inverted)
Programmed burst Length=2,4 or 8 in cases shown
Each Write command may be to any bank.

Figure 20
RANDOM WRITE CYCLES - MAX DSS



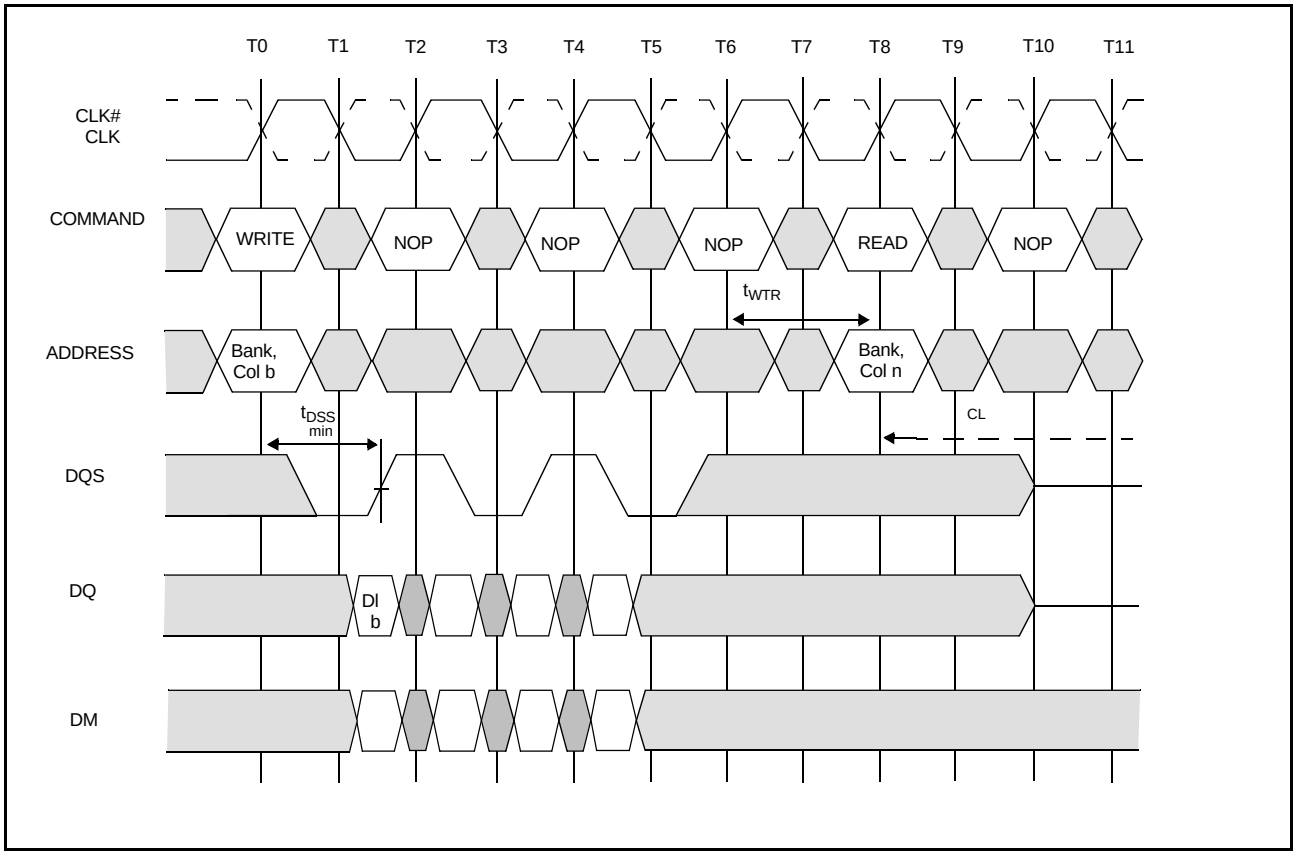
DI b, etc.=Data In for coulmn b, etc.
b',etc.=odd or even complement of b, etc.(i.e. column address LSB inverted)
Programmed burst Length=2,4 or 8 in cases shown
Each Write command may be to any bank.

Figure 21
RANDOM WRITE CYCLES - MIN DSS



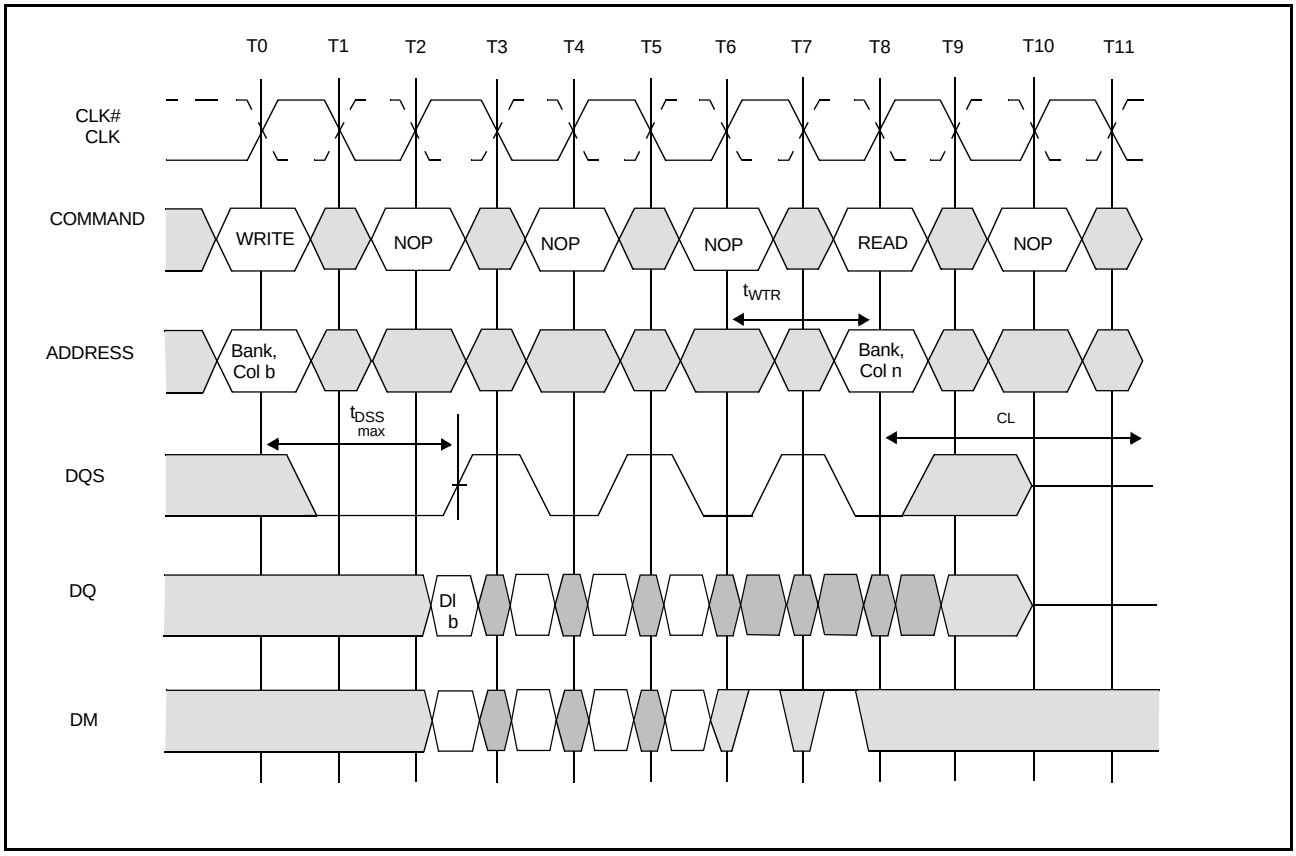
DI b=Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
t_{WTR} is referenced from the first positive CLK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 22
WRITE TO READ - MAX DSS, NON-INTERRUPTING



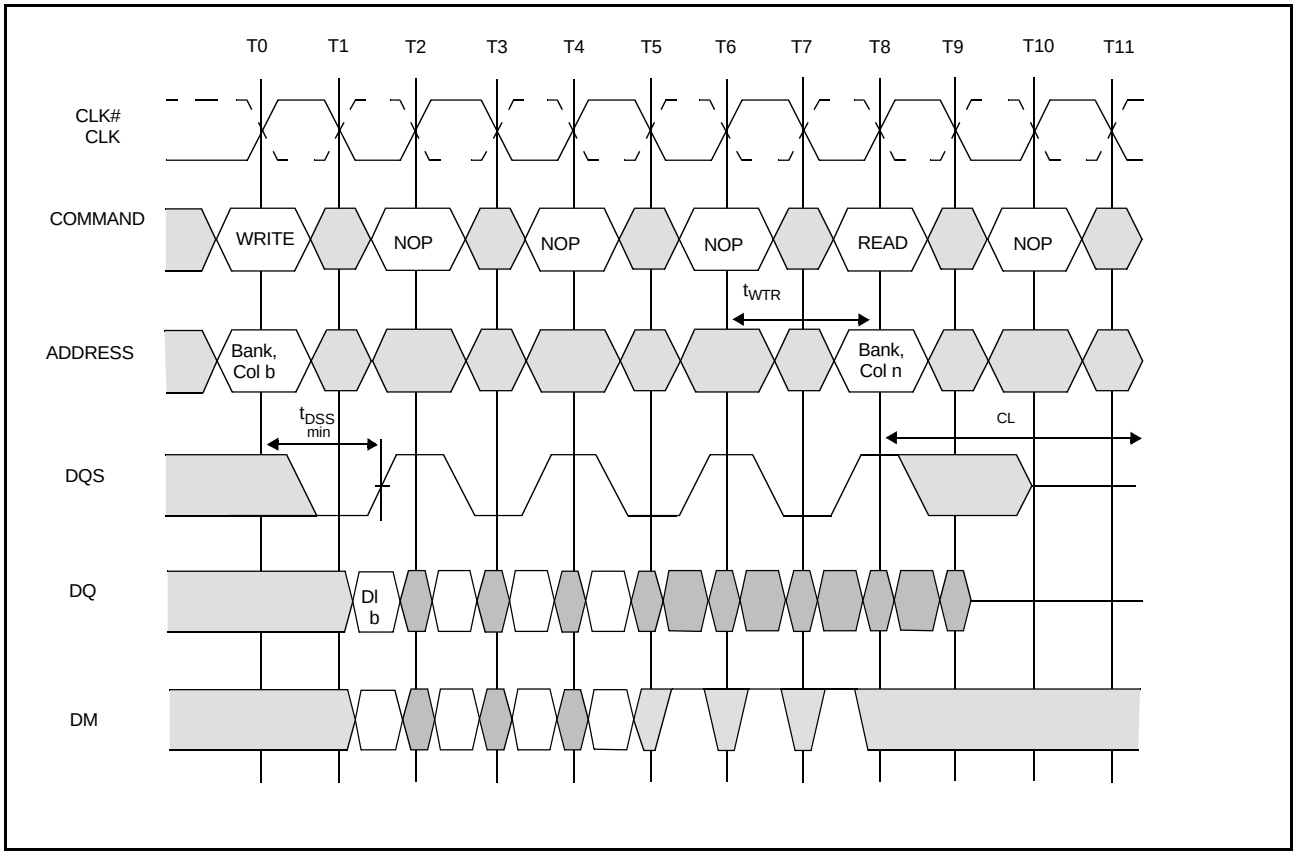
DI b=Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
t_{WTR} is referenced from the first positive CLK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 23
WRITE TO READ - MIN DSS, NON-INTERRUPTING



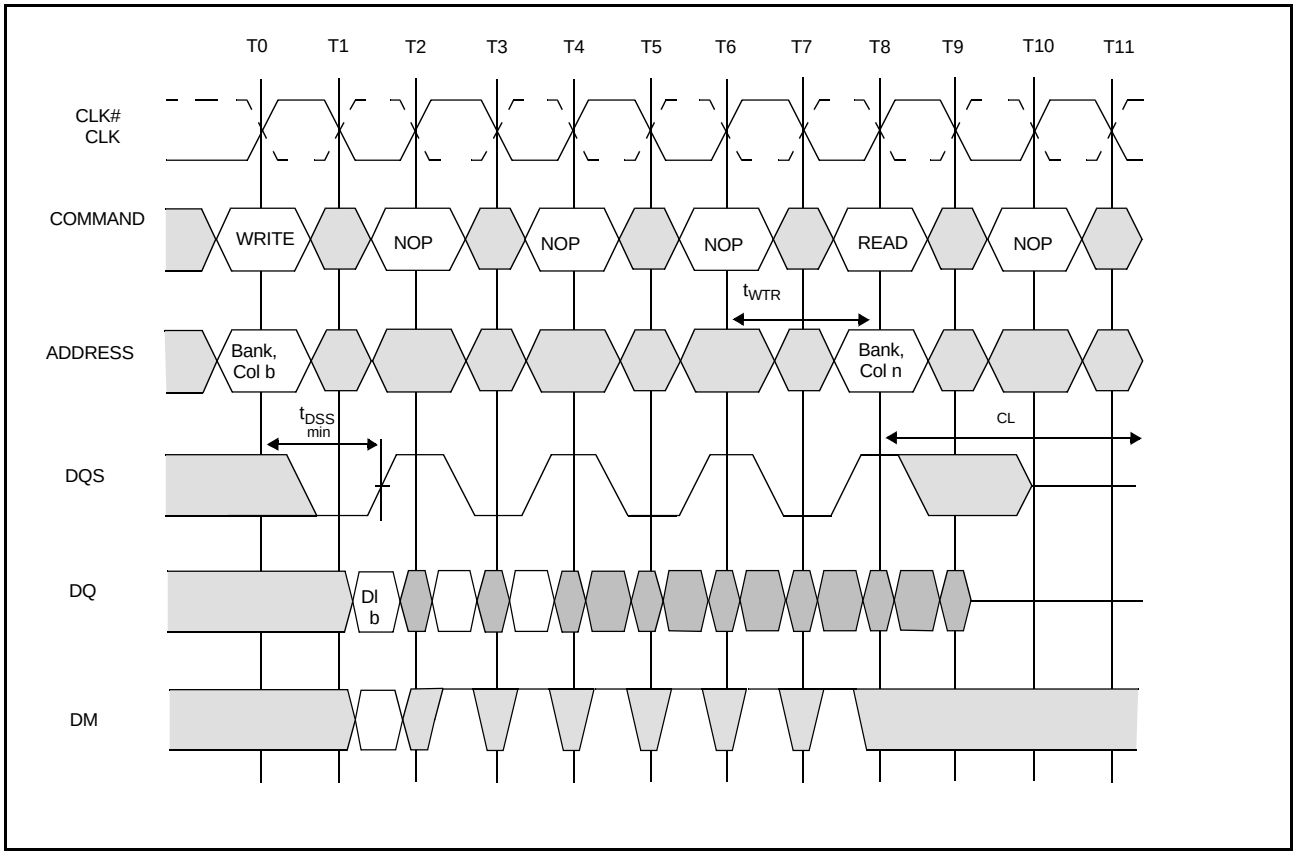
DI b=Data In for column b
An interrupted burst of 8 is shown, 4 data elements are written
3 subsequent elements of Data In are applied in the programmed order following DI b
t_{WTR} is referenced from the first positive CLK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 24
WRITE TO READ - MAX DSS, INTERRUPTING



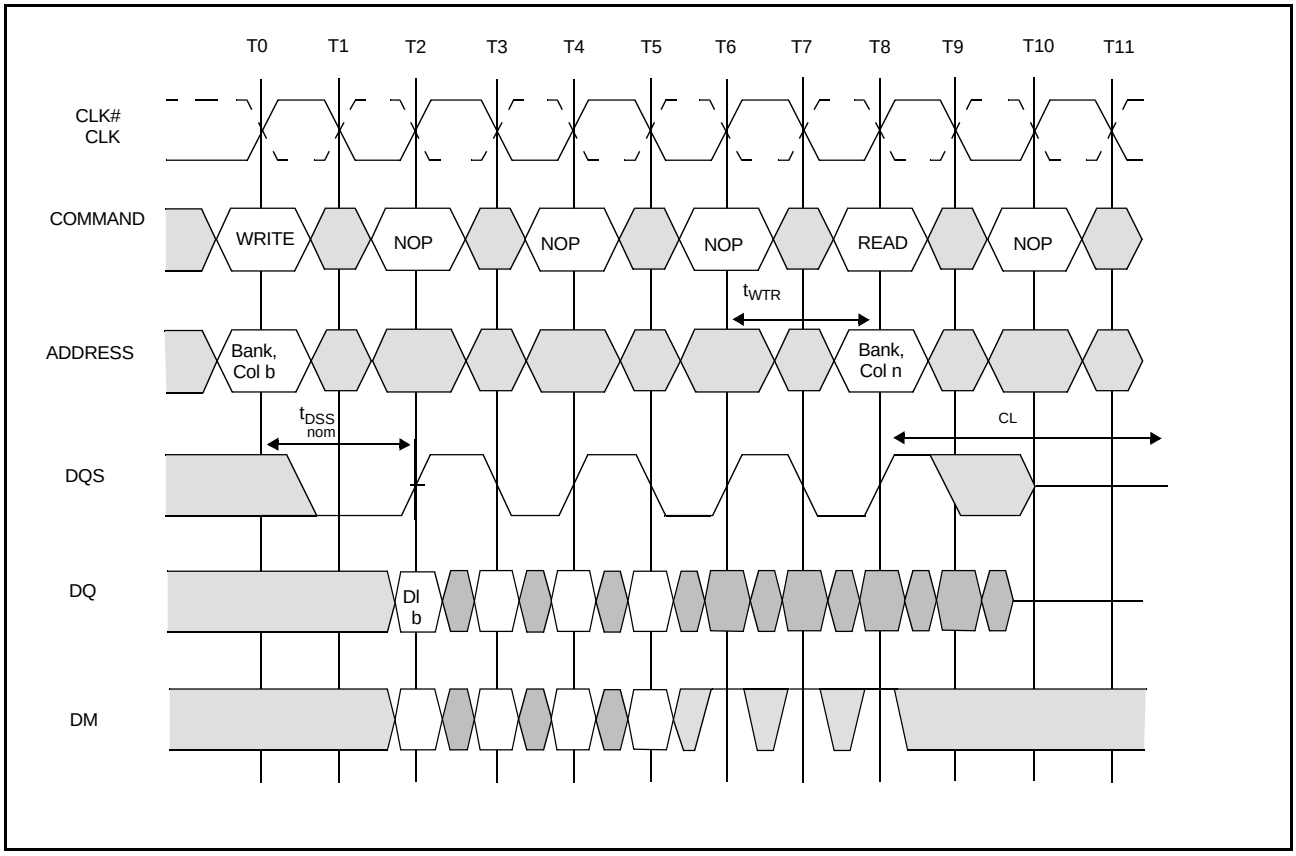
DI b=Data In for column b
An interrupted burst of 8 is shown, 4 data elements are written
3 subsequent elements of Data In are applied in the programmed order following DI b
t_{WTR} is referenced from the first positive CLK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 25
WRITE TO READ - MIN DSS, INTERRUPTING



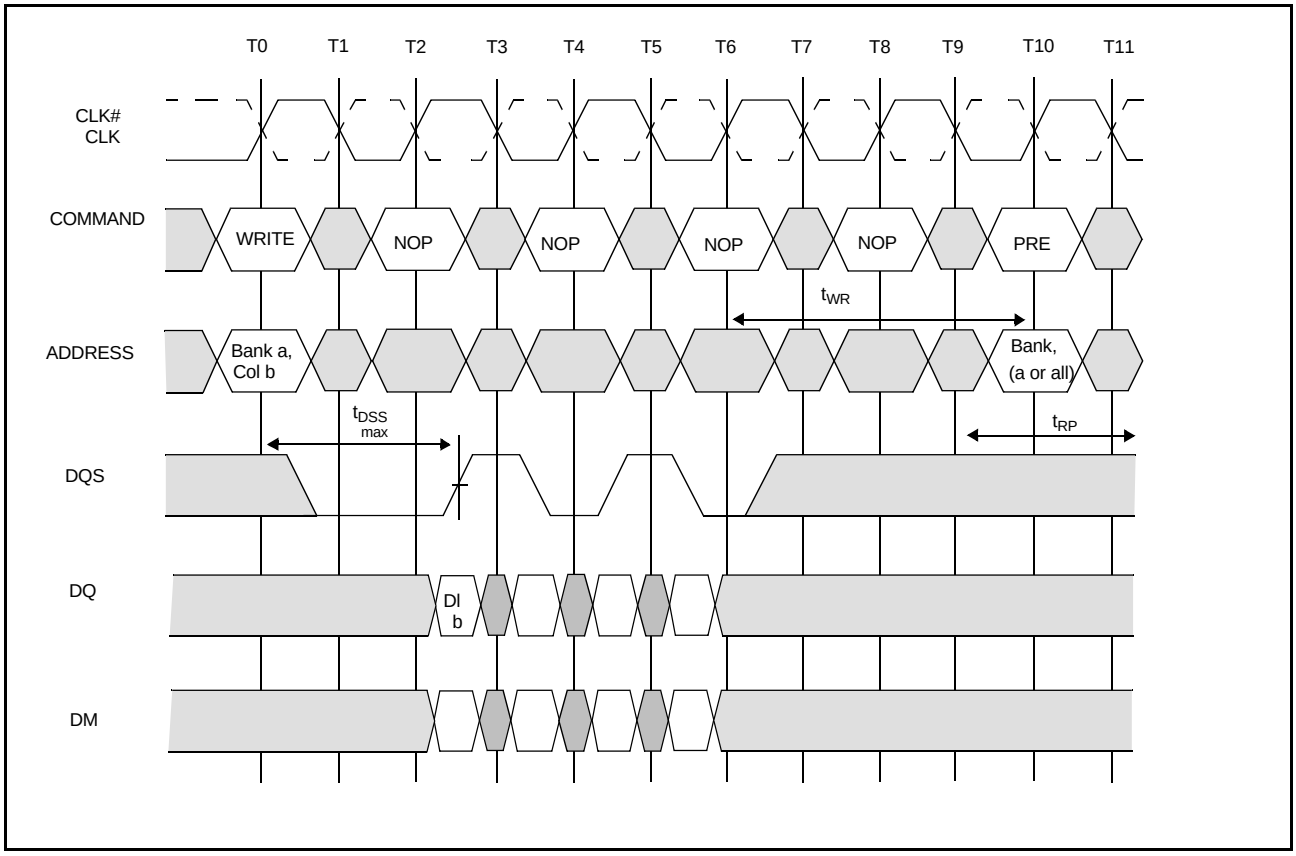
Dl b= Data In for column b
An interrupted burst of 8 is shown, 3 data elements are written
2 subsequent elements of Data In are applied in the programmed order following Dl b
t_{WTR} is referenced from the first positive CLK edge after the last desired Data in pair (not the last desired data in element)
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 26
WRITE TO READ - MIN DSS, ODD NUMBER OF DATA, INTERRUPTING



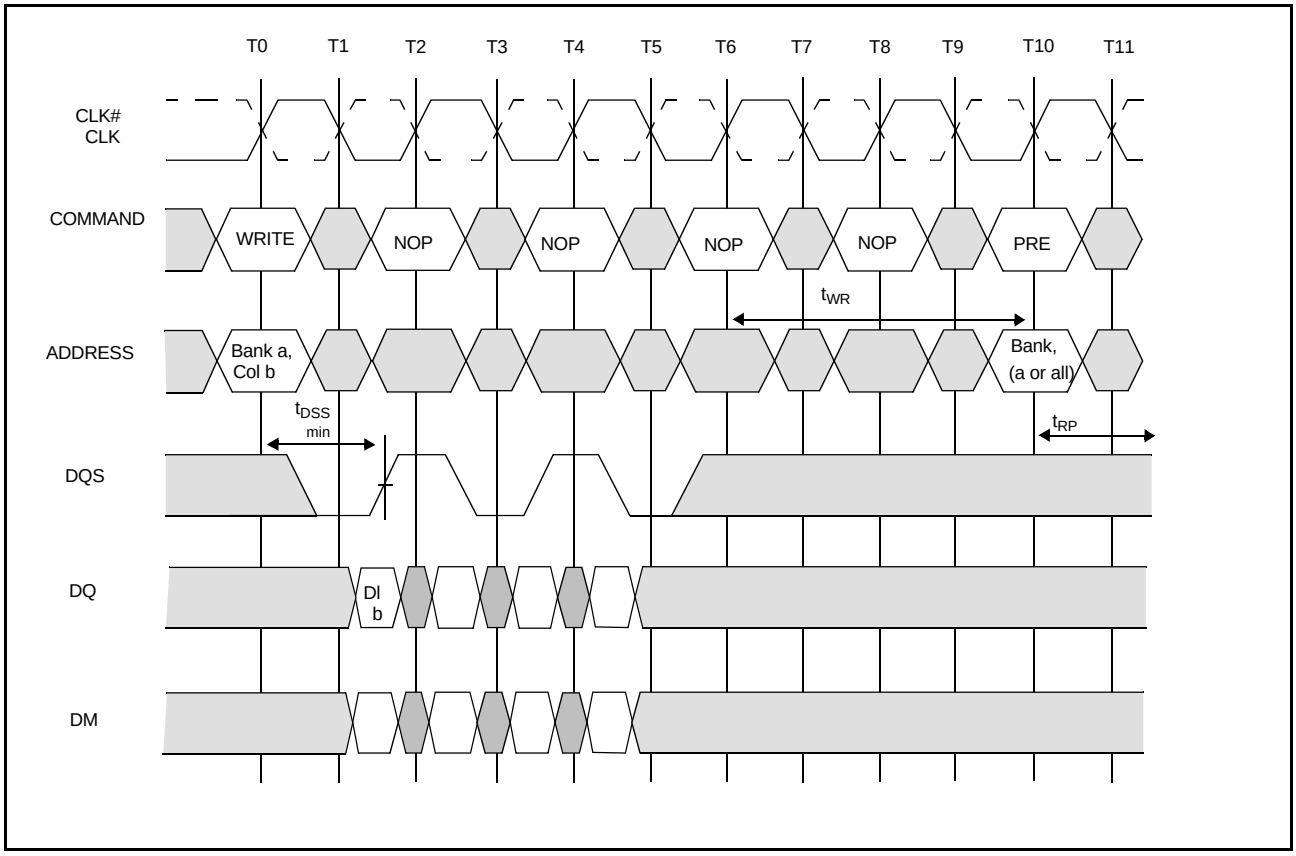
Dl b= Data In for column b
An interrupted burst of 8 is shown, 4 data elements are written
3 subsequent elements of Data In are applied in the programmed order following Dl b
t_{WTR} is referenced from the first positive CLK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 27
WRITE TO READ - NOMINAL DSS, INTERRUPTING



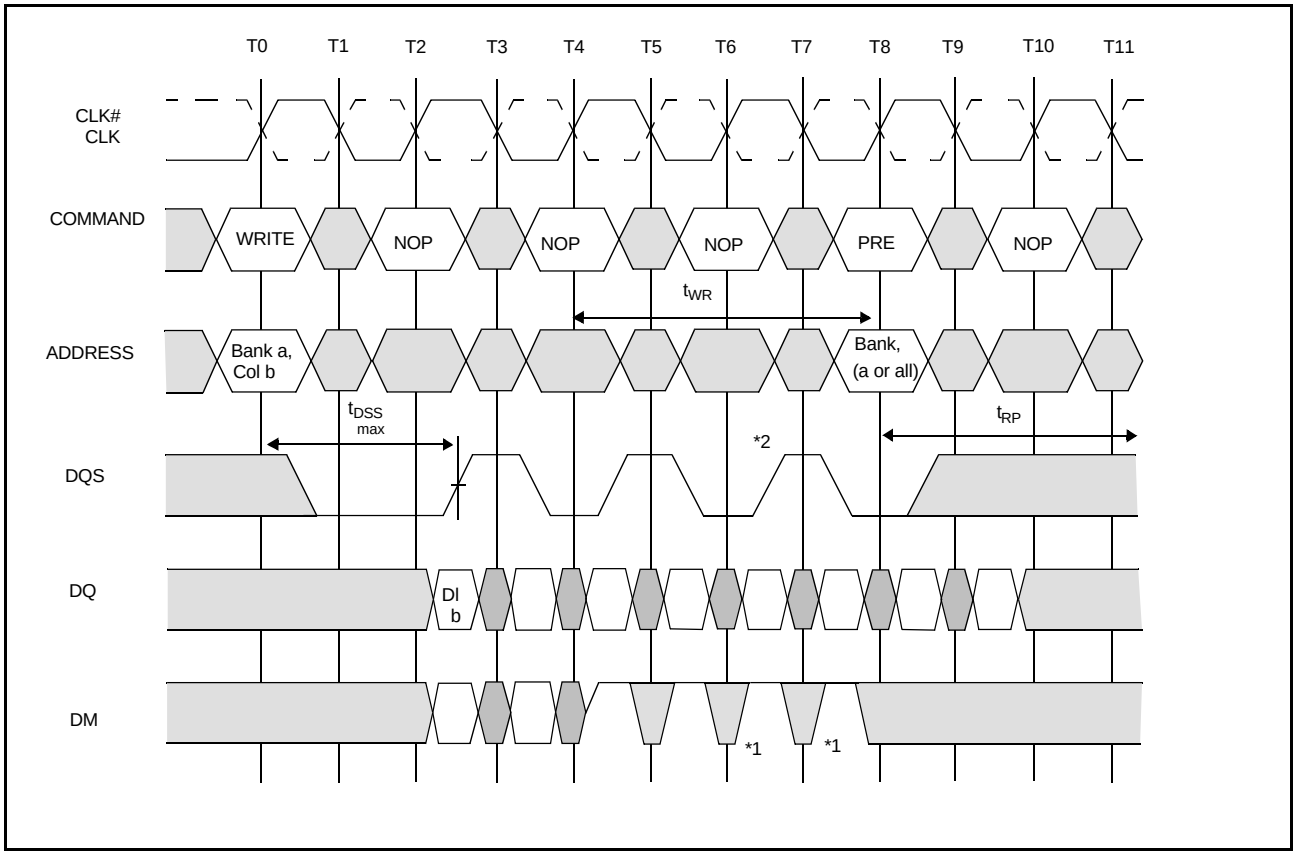
DI b=Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
t_{WTR} is referenced from the first positive CLK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 28
WRITE TO PRECHARGE - MAX DSS, NON-INTERRUPTING



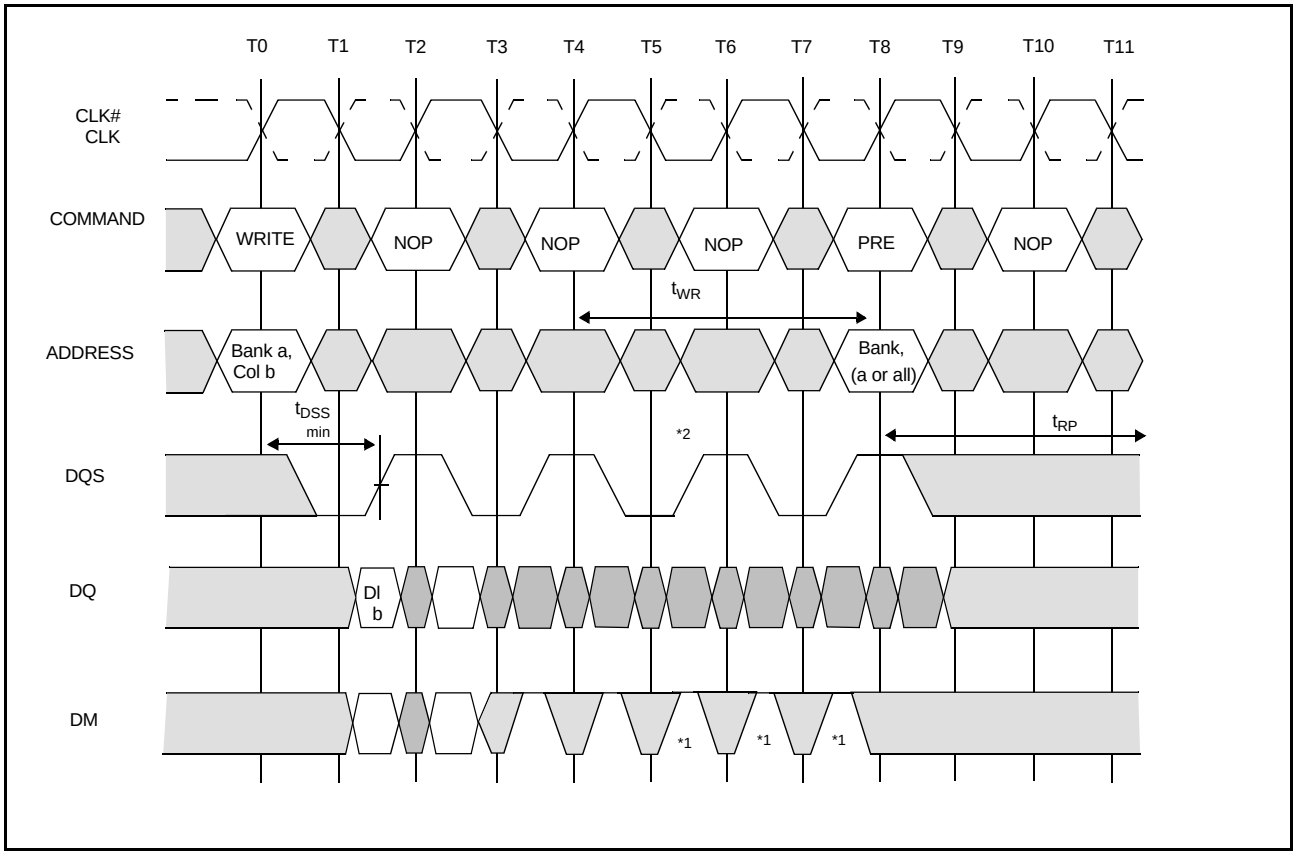
DI b=Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
t_{WR} is referenced from the first positive CLK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 29
WRITE TO PRECHARGE - MIN DSS, NON-INTERRUPTING



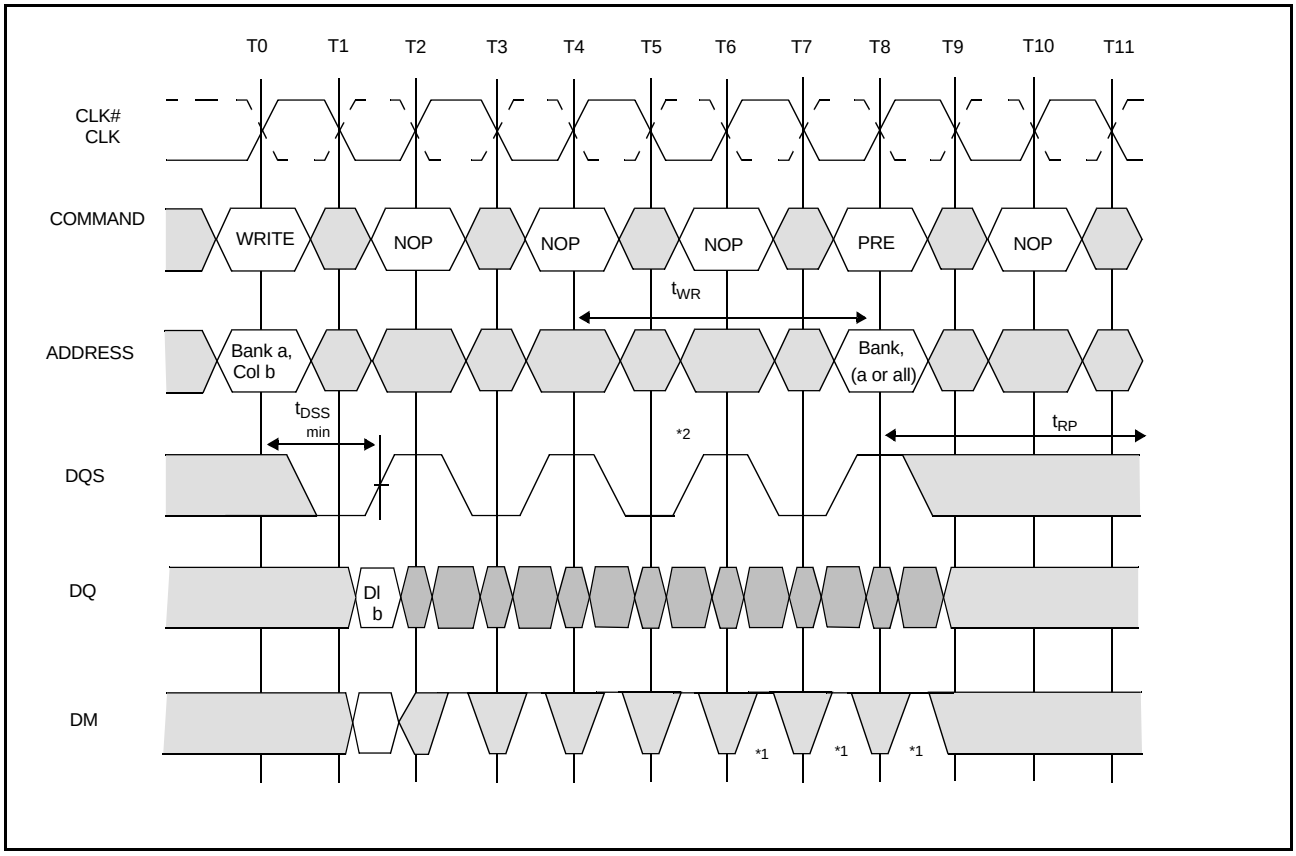
DI b =Data In for column b
An interrupted burst of 4 or 8 is shown, 2 data elements are written
1 subsequent element of Data In is applied in the programmed order following DI b
t_{WR} is referenced from the first positive CLK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1=can be dont care for programmed burst length of 4
*2=for programmed burst length of 4, DQS becomes dont care at this point

Figure 30
WRITE TO PRECHARGE - MAX DSS, INTERRUPTING



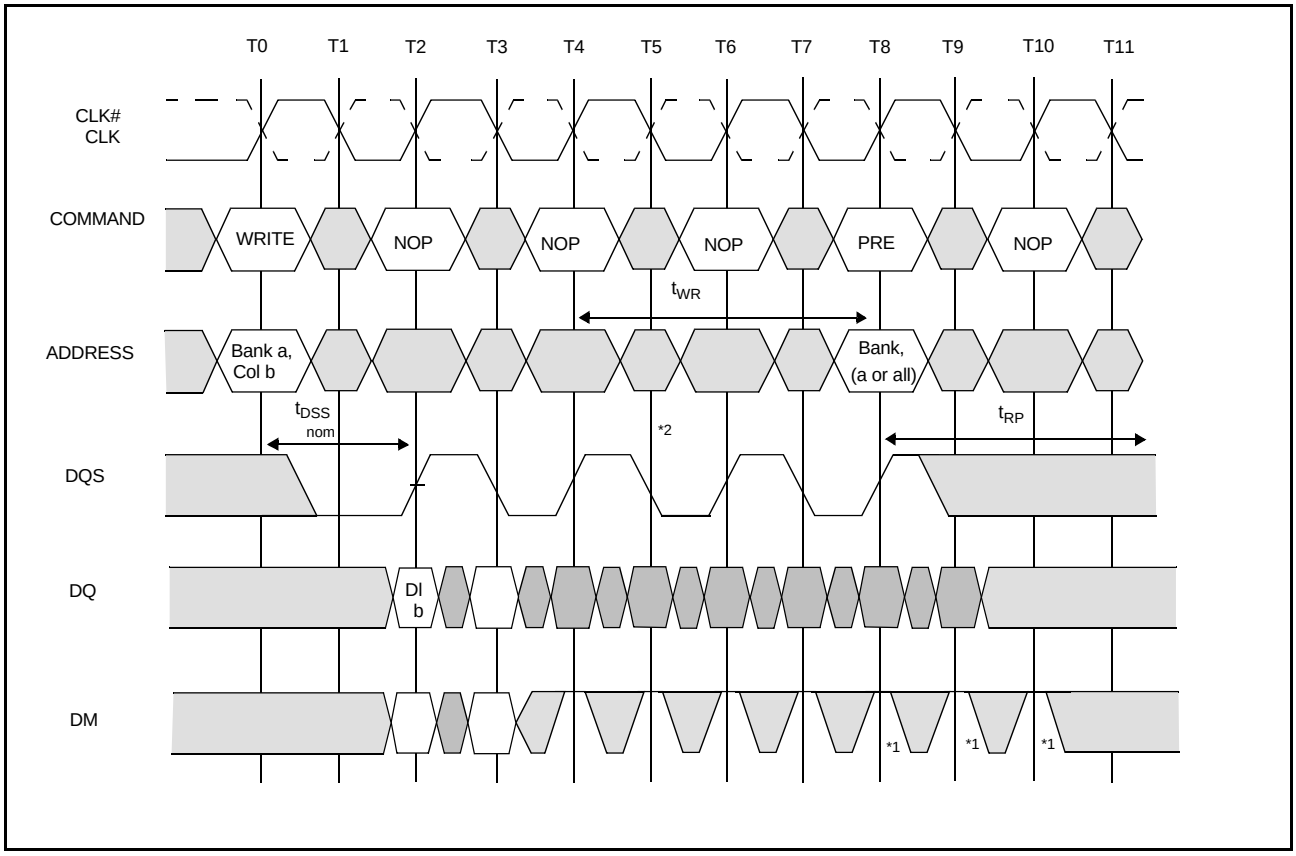
DI b=Data In for column b
An interrupted burst of 4 or 8 is shown, 2 data elements are written
1 subsequent element of Data In is applied in the programmed order following DI b
t_{WR} is referenced from the first positive CLK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1=can be dont care for programmed burst length of 4
*2=for programmed burst length of 4, DQS becomes dont care at this point

Figure 31
WRITE TO PRECHARGE - MIN DSS, INTERRUPTING



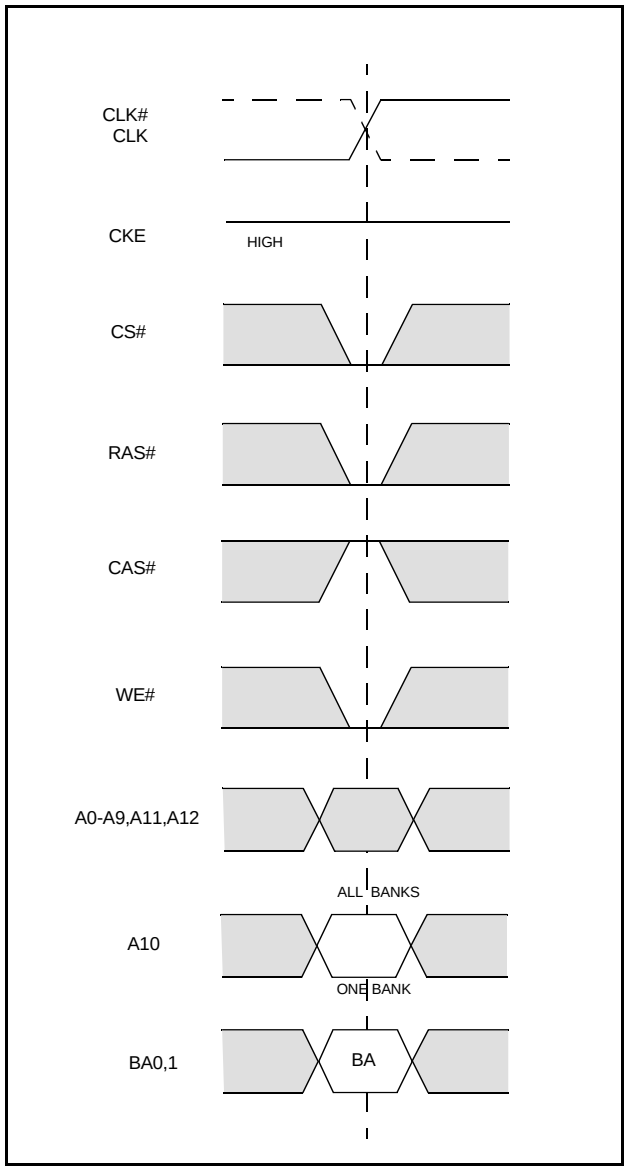
DI b=Data In for column b
An interrupted burst of 4 or 8 is shown, 1 data elements are written
t_{WR} is referenced from the first positive CLK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1=can be dont care for programmed burst length of 4
*2=for programmed burst length of 4, DQS becomes dont care at this point

Figure 32
WRITE TO PRECHARGE - MIN DSS, ODD NUMBER OF DATA, INTERRUPTING



DI b=Data In for column b
An interrupted burst of 4 or 8 is shown, 2 data elements are written
1 subsequent element of Data In is applied in the programmed order following DI b
t_{WR} is referenced from the first positive CLK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1=can be dont care for programmed burst length of 4
*2=for programmed burst length of 4, DQS becomes dont care at this point

Figure 33
WRITE TO PRECHARGE - NOMINAL DSS, INTERRUPTING



BA=Bank Address (if A10 LOW, otherwise dont care)

Figure 34
PRECHARGE COMMAND

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (t_{RP}) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be prcharged, inputs BA0,BA1 select the bank. When all banks are to be precharged, inputs BA0,BA1 are treated as "Dont Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

POWER-DOWN

Power-down is entered when CKE is registered LOW (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power down; if power-down occurs when there is a row active in either bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CLK, CLK# and CKE. For maximum power savings, the user has the option of disabling the DLL prior to entering Power-down. In that case, the DLL must be enabled after exiting power-down, and 200 clock cycles must occur before a READ command can be issued. In either case, CKE LOW and a stable clock signal should be maintained at the inputs of the DDR SDRAM, and all other input signals are "Dont Care". The device may not remain in the power-down state loger than the refresh period (64ms) since no refersh operations are performed in this mode.

The power-down state is exited when CKE is registered HIGH, and a command may be applied be applied one clock cycle later.

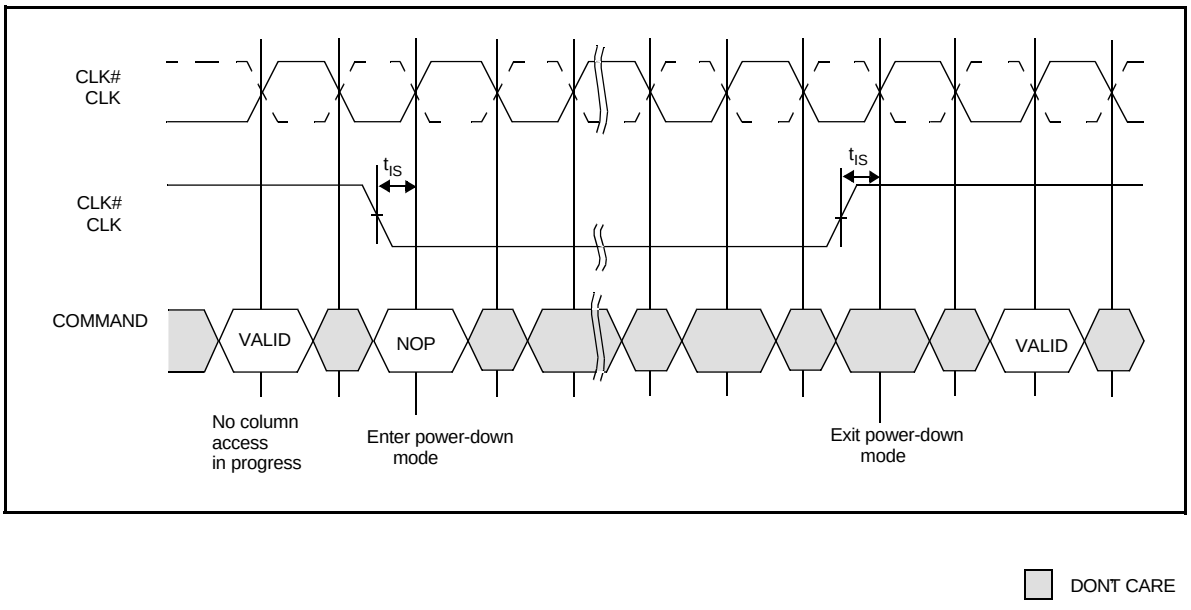


Figure 35
POWER-DOWN

TRUTH TABLE 2-CKE

(Notes: 1-4)

CKE_{n-1}	CKE_n	CURRENT STATE	$COMAND_n$	$ACTION_n$	NOTES
L	L	Power-Down	X	Maintain Power-Down	
		Self Refresh	X	Maintain Self Refresh	
L	H	Power-Down	COMMAND INHIBIT or NOP	Exit Power-Down	5
		Self Refresh	COMMAND INHIBIT or NOP	Exit Self Refresh	6
H	L	All Banks Idle	COMMAND INHIBIT or NOP	Precharge Power-Down Entry	
		Bank(s) Active	COMMAND INHIBIT or NOP	Active Power-Down Entry	
		All Banks Idle	AUTO REFERESH	Self Refresh Entry	
H	H		See Truth Table 3		

NOTE: 1. CKEn is the logic state of CKE at clock edge n, CKE_{n-1} was the state of CKE at the previous clock edge.

2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.

3. $COMMAND_n$ is the command registered at clock edge n, and $ACTION_n$ is result of $COMMAND_{n-}$

4. All states and sequences not shown are illegal or reserved.

5.Exiting power-down at clock edge n will put the device in the "all banks idle" state in time for clock edge n+1

6. Exiting self refreshh at clock edge n will put the device in the "all banks idle" state once ^tXSR is met. COMMAND INHIBIT or NOP commands should be issued on any clock edges occurring during the XSR period. A minimum of two NOP commands must be provided during t_{XSR} period. A minimum of 200 clock cycles is needed before applying a read command, for the DLL to lock.

TRUTH TABLE 3-Current State Bank n - Command to Bank n

(Notes: 1-6; notes appear below and on next page)

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMANDACTION	NOTES
Any	H	X	X	X	COMMAND INHBIT (NOP/continue previous operation	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
Row Active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE(truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start PRECHARGE)	8

NOTE:

1. This table applies when CKE_{n-1} was HIGH and CKE_n Is HIGH (see Turn Table 2) and after ^tXSR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state, Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^tRP has been met.

   Row Active: A row in the bank has been activated, and ^tRCD has been met. No data bursts/ accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.

4. The following states must not be interrupted by a command issued to the same bank, COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table3, and according to Truth Table 4.

   Precharging: Starts with registration of a PRECHARGE command and ends when ^{t}RP is met. Once ^{t}RP is met, the bank will be in the idle state.

   Row Activating: Starts with registration of an ACTIVE command and ends when ^{t}RCD is met. Once ^{t}RCD is met, the bank will be in the "row active" state.

   Read w/Auto-

   Precharge Enabled: Starts with registration of a READ command with AUTO PRECHARGE enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.

   Write w/Auto-

   Precharge Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.

   Write w/Auto

   Precharge Enabled: Starts with registrayion of a WRITE command with AUTO PRECHARGE enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFERESH command and ends when ^{t}RC is met. Once ^{t}RC is met, the DDR SDRAM will be in the "all banks idle" state.

   Accessing Mode

   Register: Starts with registration of a LOAD MODE REGISTER command and ends when ^{t}MTC has been met. Once ^{t}MTC is met, the DDR SDRAM will be in the "all banks idle" state.

   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. Once ^{t}RP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; reguired that all banks are idle.
8. May or may not be bank-specific; if all banks are to be precharged, all must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.

TRUTH TABLE 4-Current State Bank n - Command to Bank m

(Notes: 1-6; notes appear below and on next page)

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMANDACTION	NOTES
Any	H	X	X	X	COMMAND INHBIT (NOP/continue previous operation	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwiswe Allowed to Bank m	
Read Activating, Active, or Precharging	L	L	H	H	ACTIVE (select andactivate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE(select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Write (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (With Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Write (With Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	

NOTE:

1. This table applies when CKE_{n-1} was HIGH and CKE_n Is HIGH (see Truth Table 2) and after ^{t}XSR has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.

3. Current state definitions:

Idle: The bank has been precharged, and ^{t}RP has been met.

Row Active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.

Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.

Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.

Read with Auto Precharge Enabled: See following text

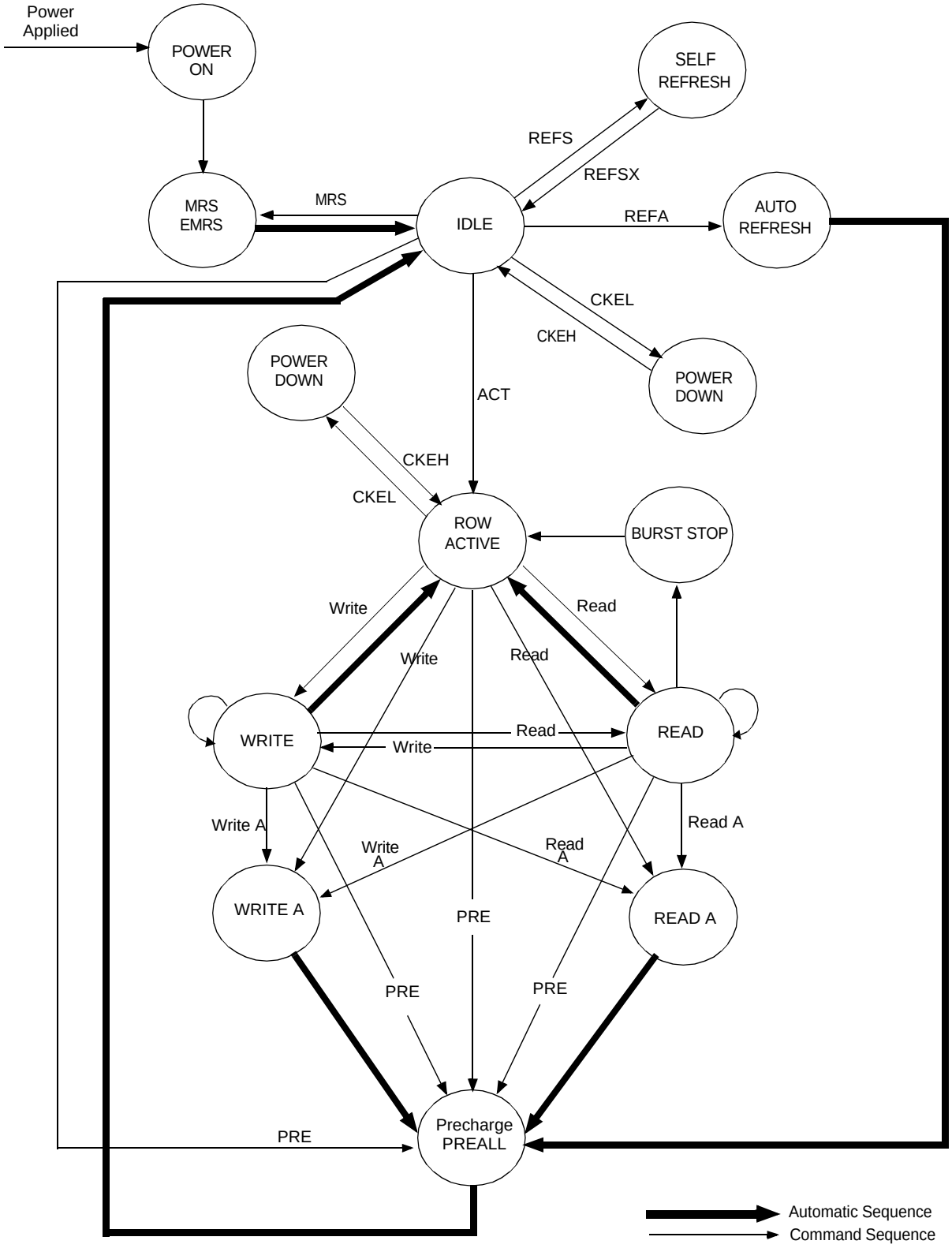
Write with Auto Precharge Enabled: See following text

The Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. The precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. The access period starts with registration of the command and ends where the precharge period (or ^{t}RP) begins.

During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other bank may be applied. In either case, all other related limitations apply (e.g. following a Read with Auto Precharge by a Write command to another bank is subject to the same data path limitations as when following a Read by a Write).

4. AUTO REFERESH, LOAD MODE REGISTER and PRECHARGE ALL commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.

Simplified state Diagram



Absolute Maximum ratings

Paramefer	Sysbol	Value	Unit
Supply voltage relative to Vss (With VDD 3.3V)	V_{DD}	-1.0 + 4.6	V
Voltage on VDDQ relative to Vss	V_{DDQ}	-1.0 + 3.6	V
Voltage on input pin relative to Vss	V_{IN}	-1.0 + 3.6	V
Voltage on I/O pin relative to Vss	$V_{I/O}$	-0.5 to VDDQ+0.5	V
Short circuit output current	V_{OUT}	50	mA
Power dissipation	P_D	1.0	W
Operating temperature (ambient)	T_{OPT}	0 to + 70	℃
Storage temperature (plastic)	PRE	-55 to + 125	℃

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage (with VDD 3.3V)	V_{DD}	3.0	3.3	3.6	V	
I/O Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	
I/O Reference Voltage	V_{REF}	1.15	1.25	1.35	V	6
I/O Termination Voltage (system)	V_{TT}	VREF-0.04	VREF	VREF+0.04	V	7
Input high Voltage, all inputs	$V_{IH(DC)}$	VREF +0.18	-	VDD+0.3	V	
Input Low voltage, all inputs	$V_{IL(DC)}$	-0.3	-	VREF-0.18	V	
Input Voltage Level. CLK and CLK# inputs	$V_{IN(DC)}$	-0.3	-	VDDQ+0.3	V	
Input Differential Voltage, CLK and CLK# inputs	$V_{ID(DC)}$	0.36	-	VDD+0.6	V	8
Input Crossing Point Voltage, CLK and CLK# inputs	$V_{IX(DC)}$	1.15	-	1.35	V	9
Input Leakage Current Any input $0V \geq VIN \leq VDD$ (All other pins not under test=0V)	I_I	-5	-	5	uA	
Output Leakage Current (DQs are disbled;) $0V \geq VOUT \leq VDDQ$	I_{OZ}	-5	-	5	uA	
Output Levels Output High Current (V_{out}=1.95V) Output Low current (V_{out}=0.35V)	I_{OH} I_{OL}	-15.2	-	- 15.2	mA	

Capacitance

(Ta=25°C, f=1MHZ)

Parameter	Symbol	Typ	Max	Unit	NOTES
Input capacitance: CLK, CLK#	C_{11}	2.5	3.5	pF	13
Input capacitance (all input pins except data pins)	C_{12}	2.5	3.5	pF	13
Data input/output capacitance: DQs, DQS, DM	$C_{I/O}$	4.0	5.5	pF	13

Recommended Electrical Characteristic and D.C. Operating Conditions ($V_{DD}Q$=+2.5±0.2V, V_{DD}=3.3V, Ta=0-70°C

Description/test condition		Symbol	Max		Unit	Notes
			-75	-8		
Operating Current: Active Mode $t_R \geq t_{RC(MIN)}$, Burst=4, READ or Write CL=2.5, tCK=7ns for -8		I_{CC1}			mA	
Precharge Standby Current: Power-down mode, All banks idle CKE ≥ VIL(MAX) CL=2.5, tCK=7ns for -8		I_{CC2P}		20		
Precharge Standby Current: $\overline{CS} \geq V_{IH}$ (MIN), All banks idle CKE ≥ VIL(MIN) CL=2.5, tCK=7ns for -8		I_{CC2N}		30		
Active Standby Current: $\overline{CS} \geq V_{IH}$ (MIN), All banks active after t_{RAS} met, no access in progress CKE ≤ VIL(MIN) CL=2.5, tCK=7ns for -8		I_{CC3}				
Operating Current: Burst=4, Continue burst CKE ≤ CIL(MAX) READ or WRITE, All banks active, address transition once per clock cycle; CL=2.5, tCK=7ns for-8		I_{CC4}		180		
Auto refresh Current:	$t_{RC} \geq t_{RC(MIN)}$	I_{CC5}		210		
Self Refresh Current: CKE ≤ 0.2V		I_{CC6}		2		11

AC OPERATIONS AND CONDITIONS:

Description	Parameter	Min.	Max.	Unit	NOTES
Input High Voltage: DQ, DQS and DM signals	V_{IH}(AC)	VREF+0.35	TBD	V	
Input Low Voltage: DQ, DQS and DM signals	V_{IL}(AC)	TBD	V_{REF}-0.35	V	
Input Differential Voltage, CLK and CLK# inputs	V_{ID}(AC)	0.7	V_{DDQ}+0.6	V	8
Input Crossing Point Voltage, CLK and CLK# inputs	V_{IX}(AC)	1.15	1.35	V	9

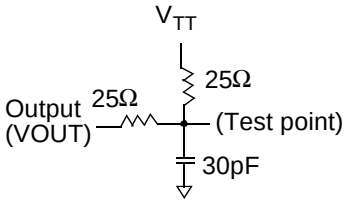
A.C Characteristics:

Test Conditions: (Ta=0 to 70°C V_{DDQ}=2.5V ±0.2V , V_{DD}=3.3V±0.3V , or V_{DD}=2.5V±0.2V

A.C. Parameter		Symbol	-75		-8		Unit	Note
			Min.	Max.	Min.	Max.	t_{CK}	
Access time from CLK/CLK#		t_{AC}	-0.1	+0.1	-0.1	+0.1	t_{CK}	
Clock high time		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	
Clock low time		t_{CL}	0.45	0.55	0.45	0.55	ns	
Clock cycle time	CL=3	t_{CK3Q}	5	15	6	15	ns	
	CL=2.5	$t_{CK2.5}$	6.2	15	7	15	ns	
	CL=2	t_{CK2}	7.5	15	8	15	ns	
	CL=1.5	t_{CK15}	10	15	10	15	t_{CK}	
Data-in hold time		t_{DH}	0.075		0.075		t_{CK}	
Data-in setup time		t_{DS}	0.075		0.075		t_{CK}	18
Data-out high imedance from CLK/CLK#		t_{HZ}	-0.1	+0.1	-0.1	+0.1	t_{CK}	18
Data-out low impedance from CLK/CLK#		t_{LZ}	-0.1	+0.1	-0.1	+0.1	t_{CK}	
DQS-DQ Skew		t_{DSDQ}	-0.075	+0.075	-0.075	+0.075	t_{CK}	
DQ/DQS output valid time		t_{DV}	0.35		0.35		t_{CK}	
Write command to first DQS latching transition		t_{DSS}	0.75	1.25	0.75	1.25	t_{CK}	
DQ/DQS input valid time		t_{DSLH}	0.40	0.60	0.40	0.60	t_{CK}	
LOAD MODE REGISTER COMMAND cycle time		t_{MRD}	2		2		t_{CK}	22
Write preamble setup time		t_{WPR}	0		0		ns	19
Write postamble		t_{WPO}	0.4	0.6	0.4	0.6	t_{CK}	20
Write command to DQS Low-Z		t_{WCP}	0		0		ns	
Input hold time		t_{IH}	0.15		0.15		t_{CK}	
Input setup time		t_{IS}	0.15		0.15		t_{CK}	
Read preamble		t_{RPR}	0.9	1.1	0.9	1.1	t_{CK}	
Read postamble		t_{RPO}	0.4	0.6	0.4	0.6	t_{CK}	
ACTIVE to PRECHARGE command		t_{RAS}	45	120,000	48	120,000	ns	
AUTO REFRESH, ACTIVE command period		t_{RC}	65		70		ns	
ACTIVE to READ or WRITE delay		t_{RCD}	20		20		ns	
Refresh period (8192 rows)		t_{REF}		64		64	ms	
PRECHARGE command period		t_{RP}	20		20		ns	
ACTIVE bank A to Active bank B command		t_{RRD}	15		20		ns	
Transition time		t_{T}					ns	
Write recovery time		t_{WR}	2		2		t_{CK}	
Write data In to Read Command Delay		t_{WTR}	1		1		t_{CK}	
Exit SELF REFRESH to ACTIVE command		t_{XSR}	60		70		ns	21

NOTES

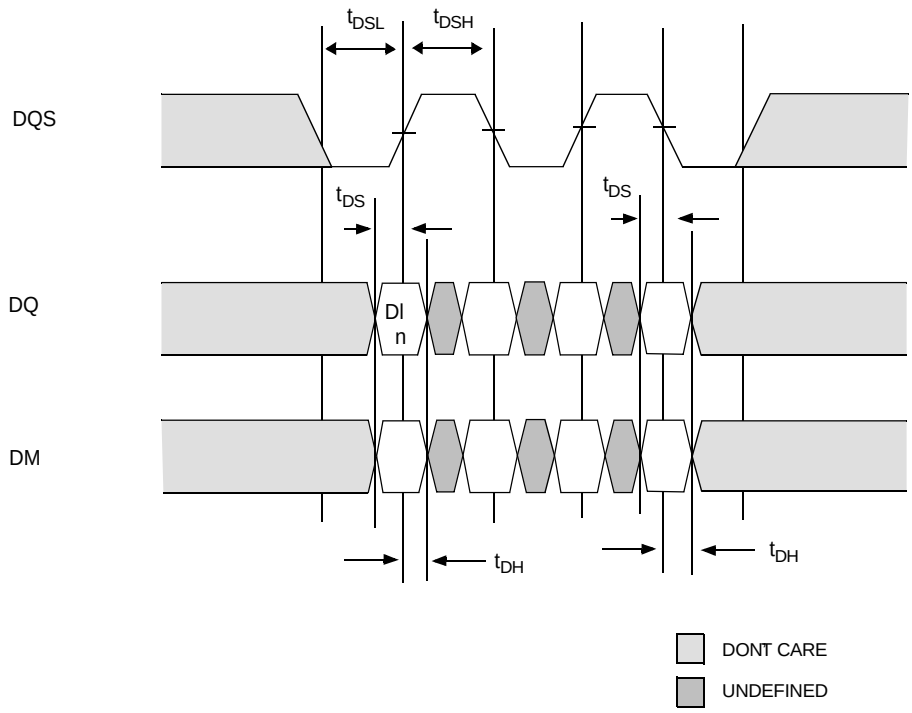
1. All voltages referenced to Vss.
2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and IDD tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CLK/CLK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above (below) the DC input LOW(HIGH) level.
6. V_{REF} is expected to track variations in the DC level of V_{DDQ} of the transmitting device. peak-to-peak noise on V_{REF} may not exceed +/-2% of the DC value.
7. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. VID is the magnitude of the difference between the input level on CLK and the input level on CLK#.
9. The value of V_{IX} is expected to equal V_{REF} and must track variations in the DC level of V_{REF}.
10. IDD is dependent on output loading and cycle rates.
    Specified values are obtained with minimum cycle time and the outputs open.
11. Enables on chip refresh and address counters.
12. IDD specifications are tested after the device is properly initialized.
13. This parameter is sampled. VDDQ+2.5V ±0.2V , VDD=+3.3V±3.3V , f=1MHz, ^{t}A=25**°C**
14. Input slew rate=1V/ns+/-20%.
15. The CLK/CLK# input reference level (for timeing referenced to CLK/CLK#) is the point at which CLK and CLK# cross; the input reference level for signals other than CLK/CLK#, is VREF.
16. Inputs are not recognized as valid until V_{REF} stabilizes. Exceptions: during the period before V_{REF} stabilizes, CKE=<0.3V_{DDQ} is recognized as LOW.
17. The output timing reference level, as measured at the test point indicated in Note 3, is V_{TT}.
18. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ), or begins driving (LZ).
19. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

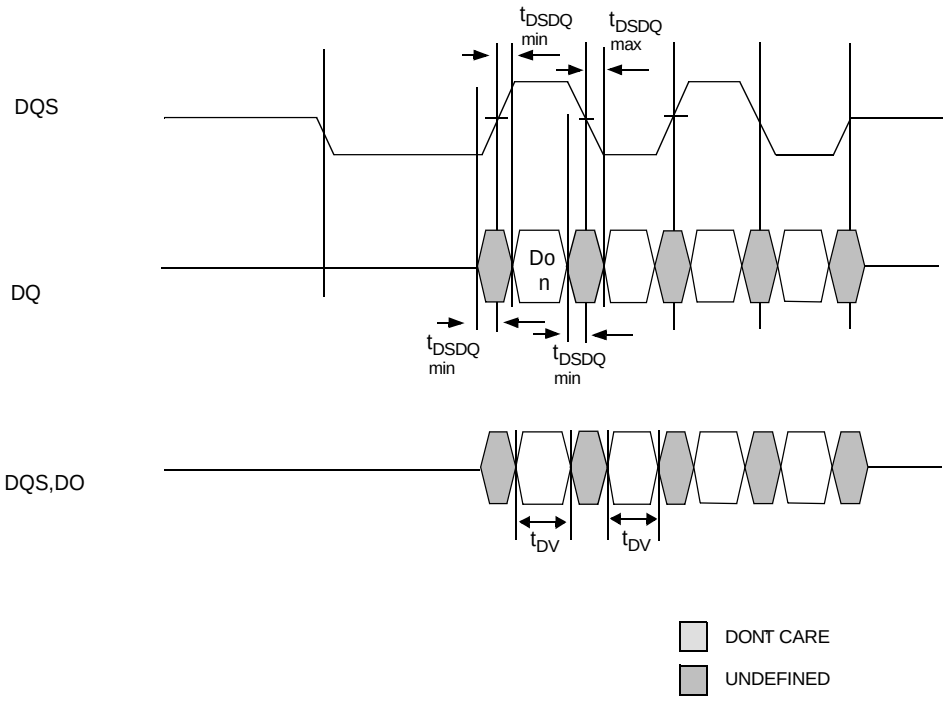
20. The minimum limit for this parameter is not a device limit. The device will operate with a negative value for this parameter, but system performance (bus turnaround) will degrade accordingly.
21. CLK must be toggled a minimum of two times during this period.
22. The specific reguirement is that DQS be valid (HIGH or LOW) on or befor this CLK edge. The case shown (DQS going from High-Z to logic LOW) applies when no writes were previously in progress on the bus. If a previous write was in progress. DQS could be HIGH at this time depending on tDSS.

DATA INPUT TIMING



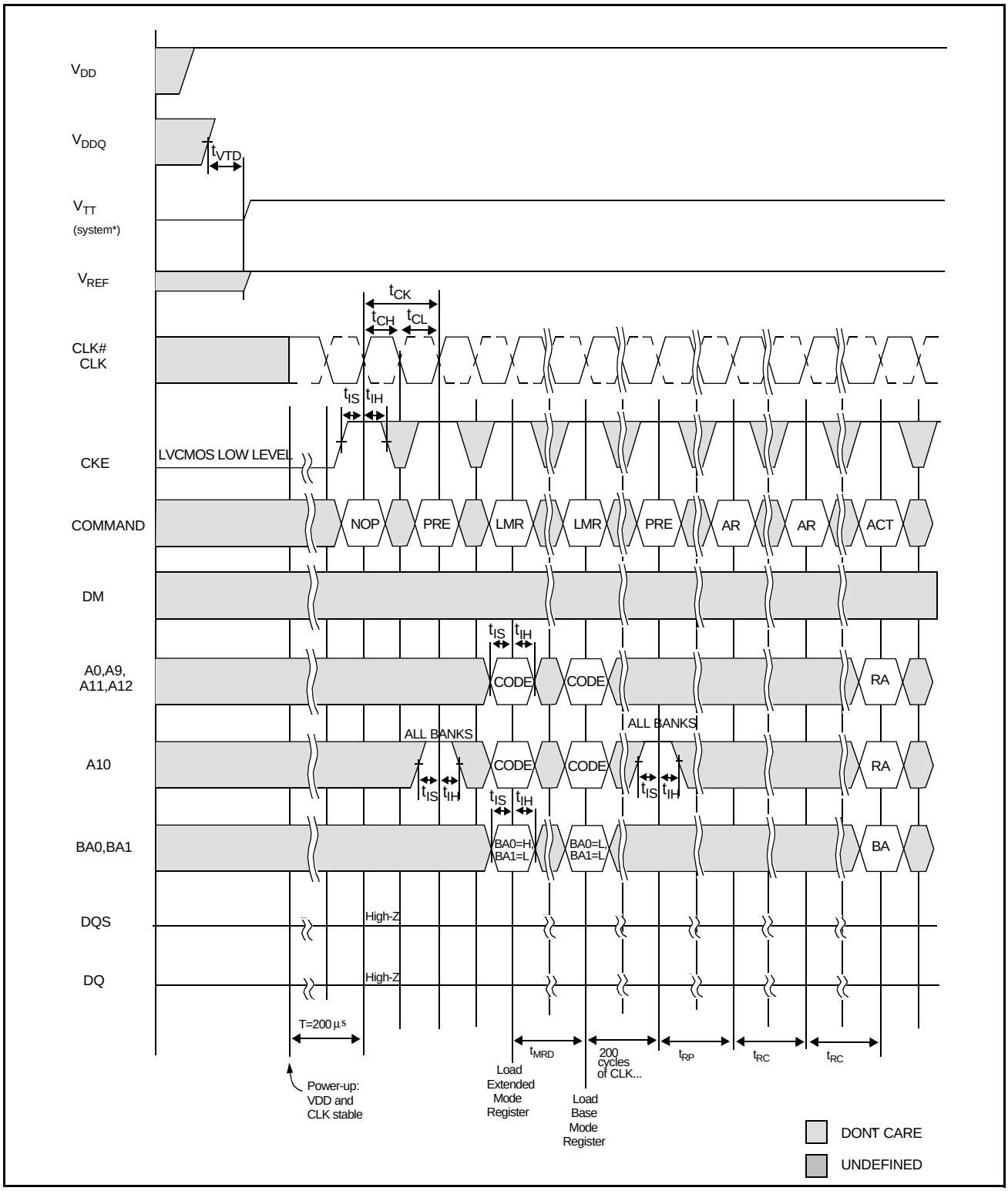
Dl n=Data In for column n
Burst Length=4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following Dl n

DATA OUTPUT TIMING



Burst Length=4 in the case shown

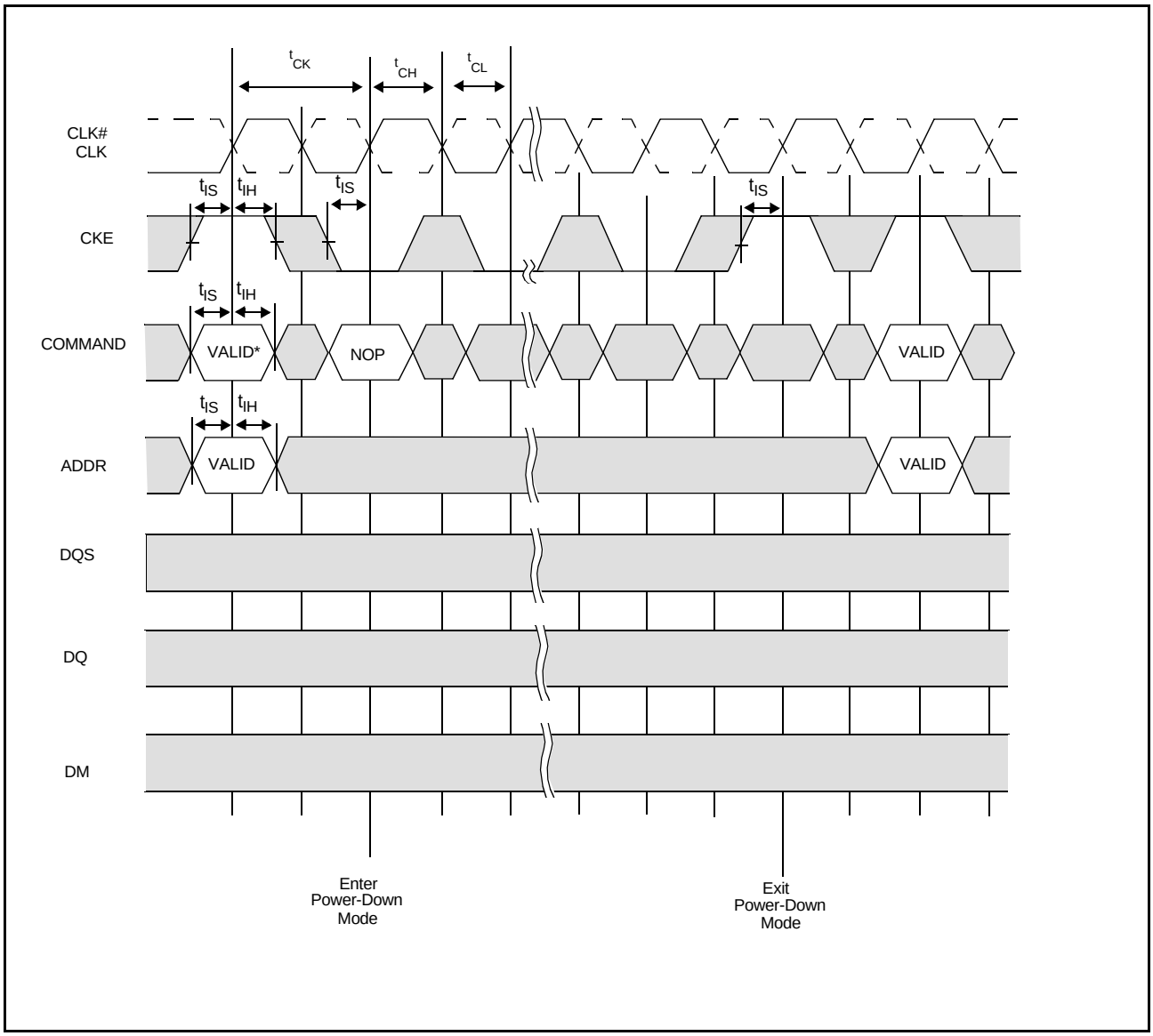
INITIALIZE AND LOAD MODE REGISTERS



•=VTT is not applied directly to the device, however t_{VTD} must be greater than or equal to zero to avoid device latch-up.

•=t_{MRD} is required before any command can be applied, and 200 cycles of CLK are required before a READ command can be applied.

POWER-DOWN MODE

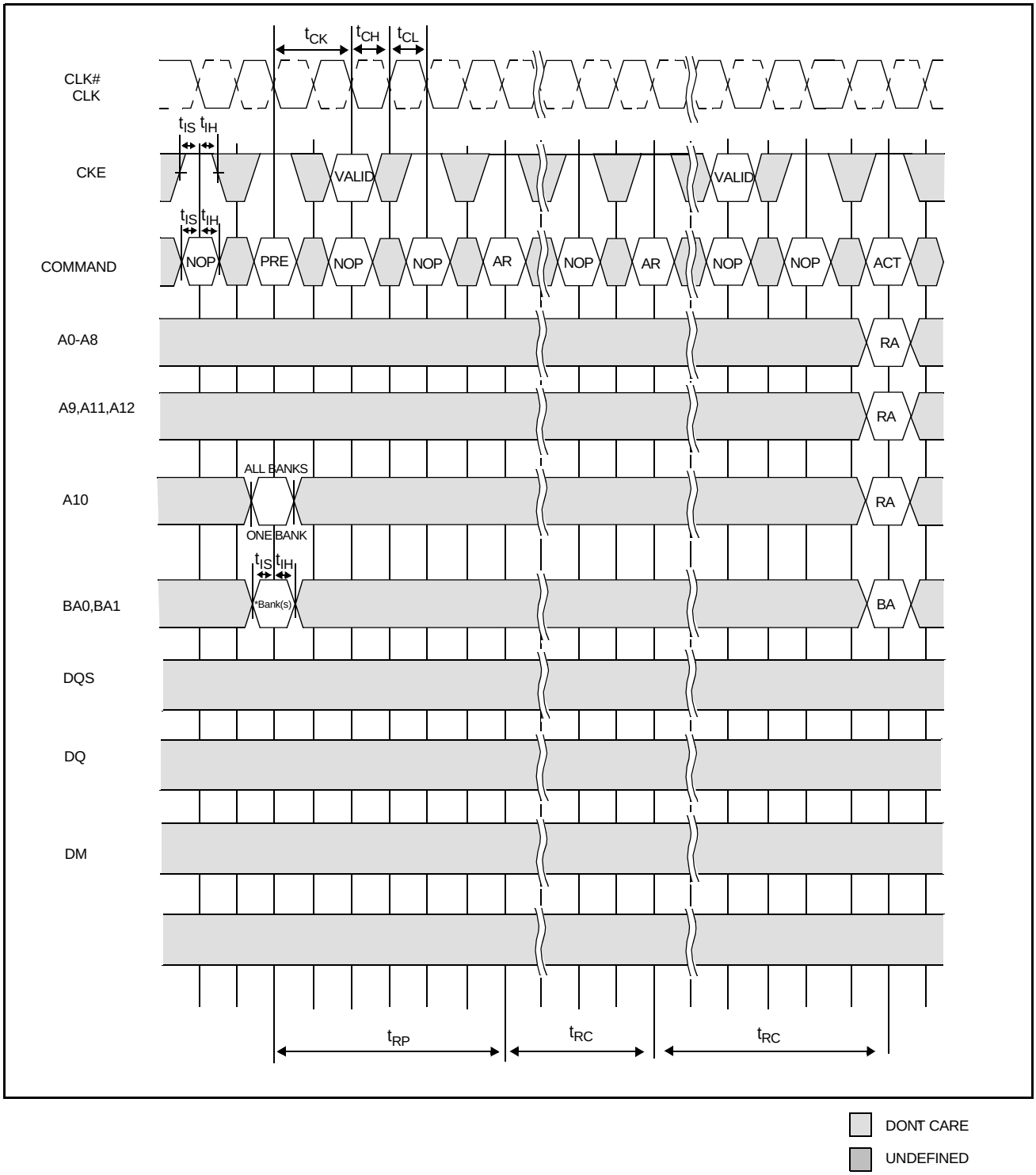


DONT CARE

UNDEFINED

No column accesses are allowed to be in progress at the time Power-Down in entered
*= If this command is a PRECHARGE (or if the device is already in the idle state) then the Power-Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at lease one row is already active) then the Power-Down mode shown is Active Power Down.

AUTO REFRESH MODE



DIS AP=Disable Autoprecharge

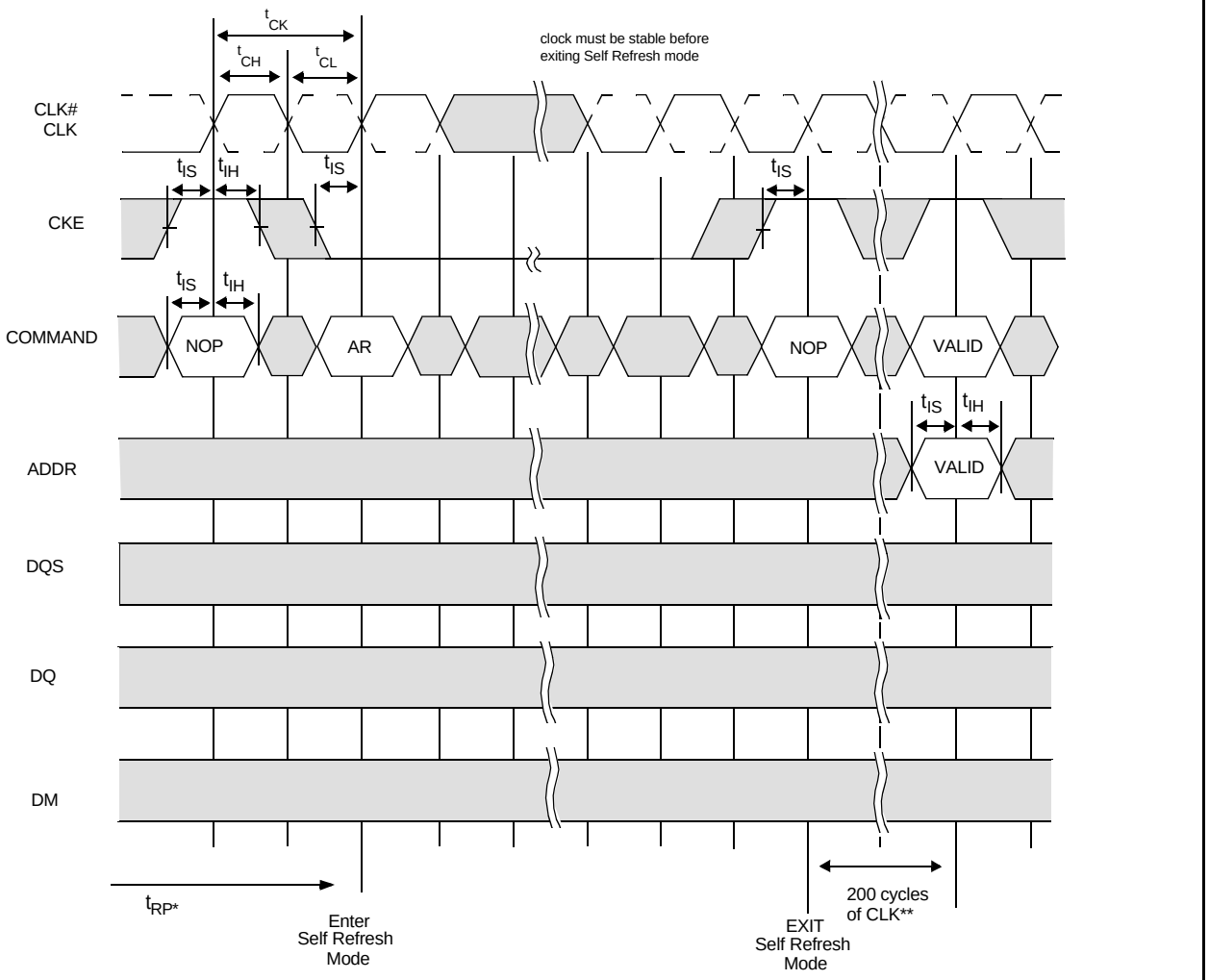
*=*Dont Care", if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active(i.e. must pre-charge all active banks)

PRE=PRECHARGE, ACT=ACTIVE, RA=Row Address, BA=Bank Address, AR=AUTOREFRESH

NOP commands are shown for ease of illustration; other valid commands may be possible at these times

DM, DQ and DQS signals are all *Dont Care"/High-Z for operations shown

SELF REFRESH MODE

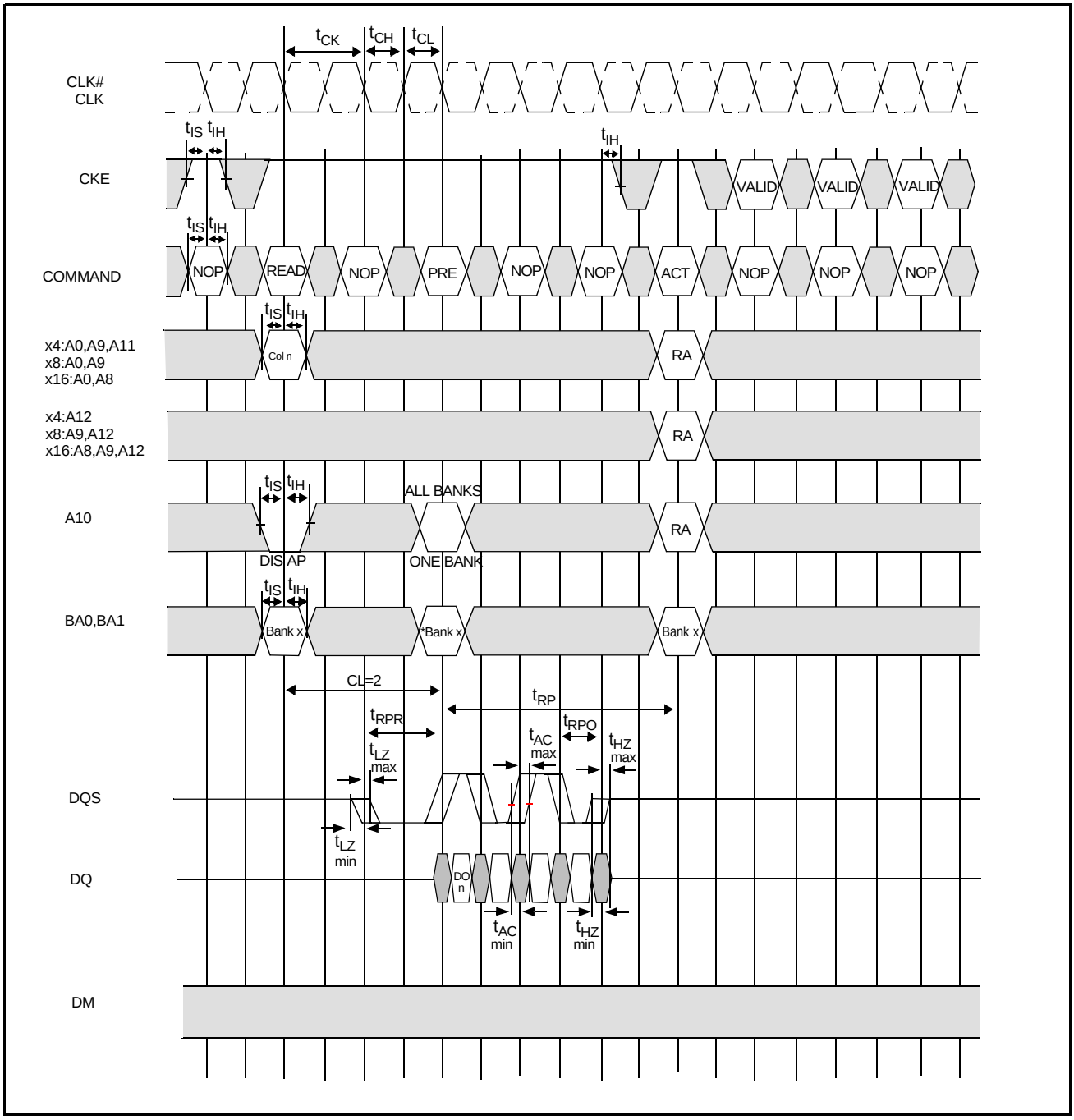


*=Device must be in the "All banks idle" state prior to entering Self Refresh mode

**=t_{RC} is required before any command can be applied, and 200 cycles of CLK are required before a READ command can be applied.

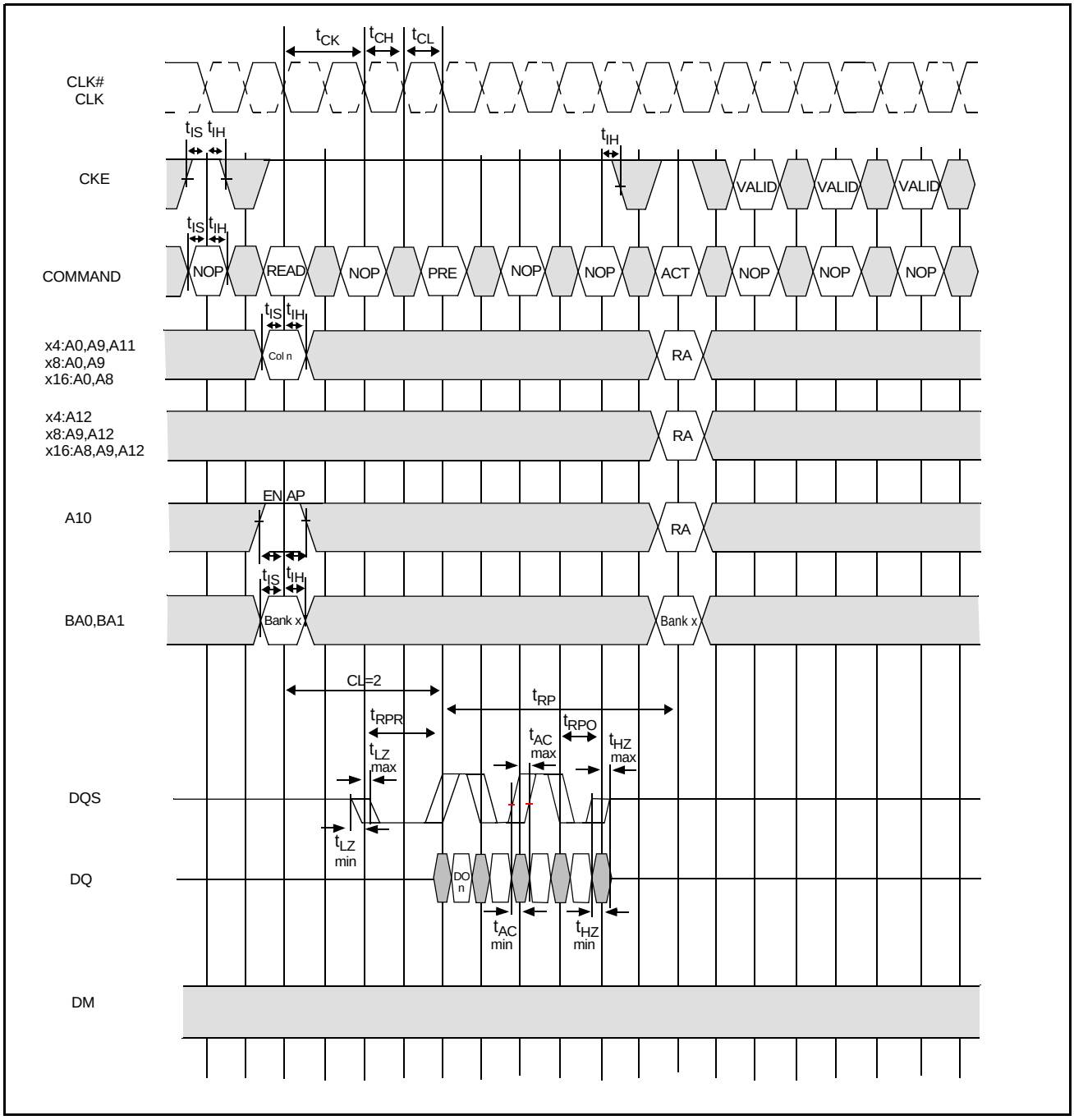
The minimum time in Self Refresh mode is t_{RAS} MIN.

READ-WITHOUT AUTO PRECHARGE



DO n=Data Out from column n
Burst Length=4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following Do n
DIS AP= Disable Autoprecharge
*="Dont Care", if A10 is HIGH at this point
PRE=PRECHARGE, ACT=ACTIVE,RA=Row Address, BA=Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

READ-WITH AUTO PRECHARGE

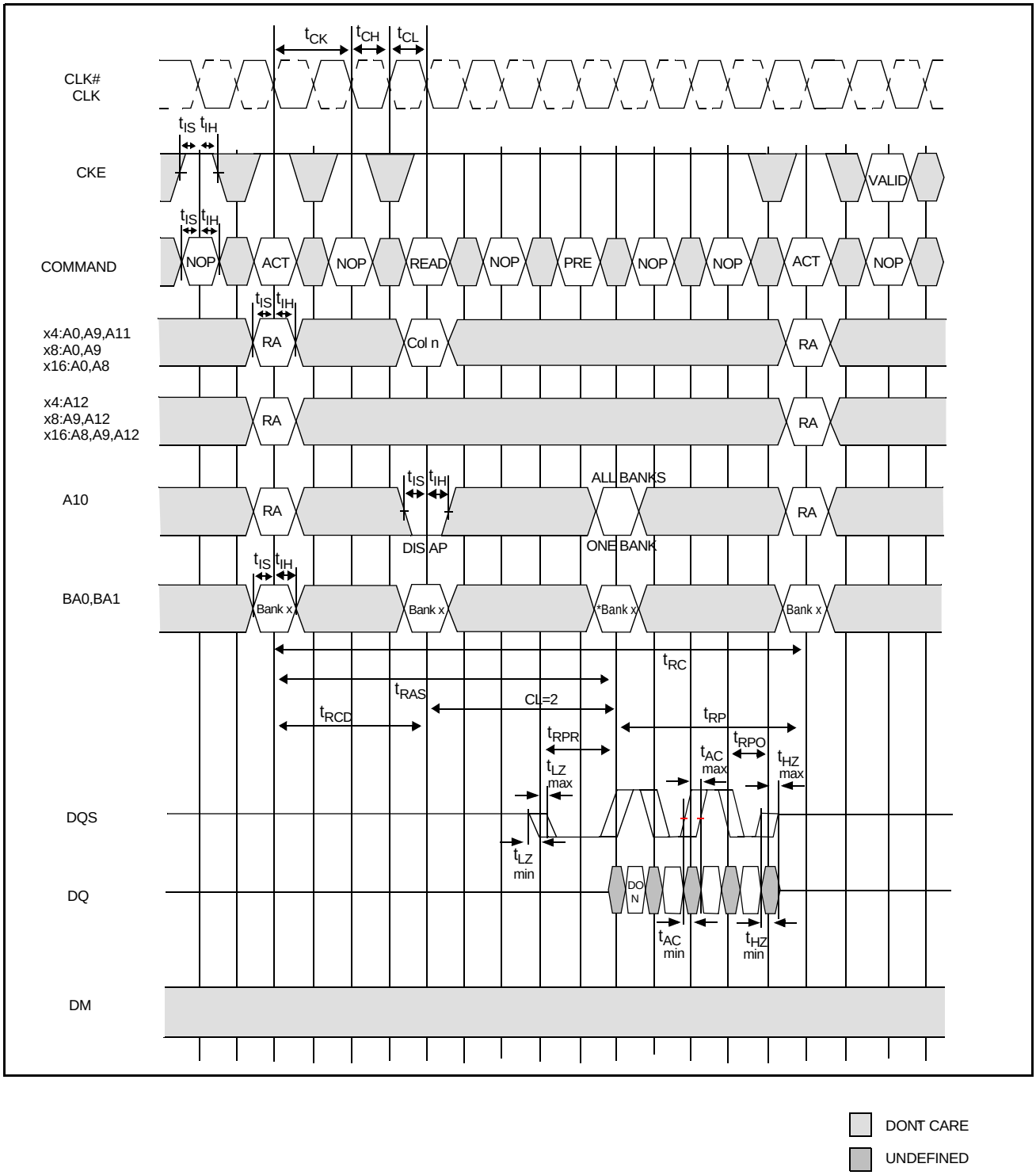


DONT CARE

UNDEFINED

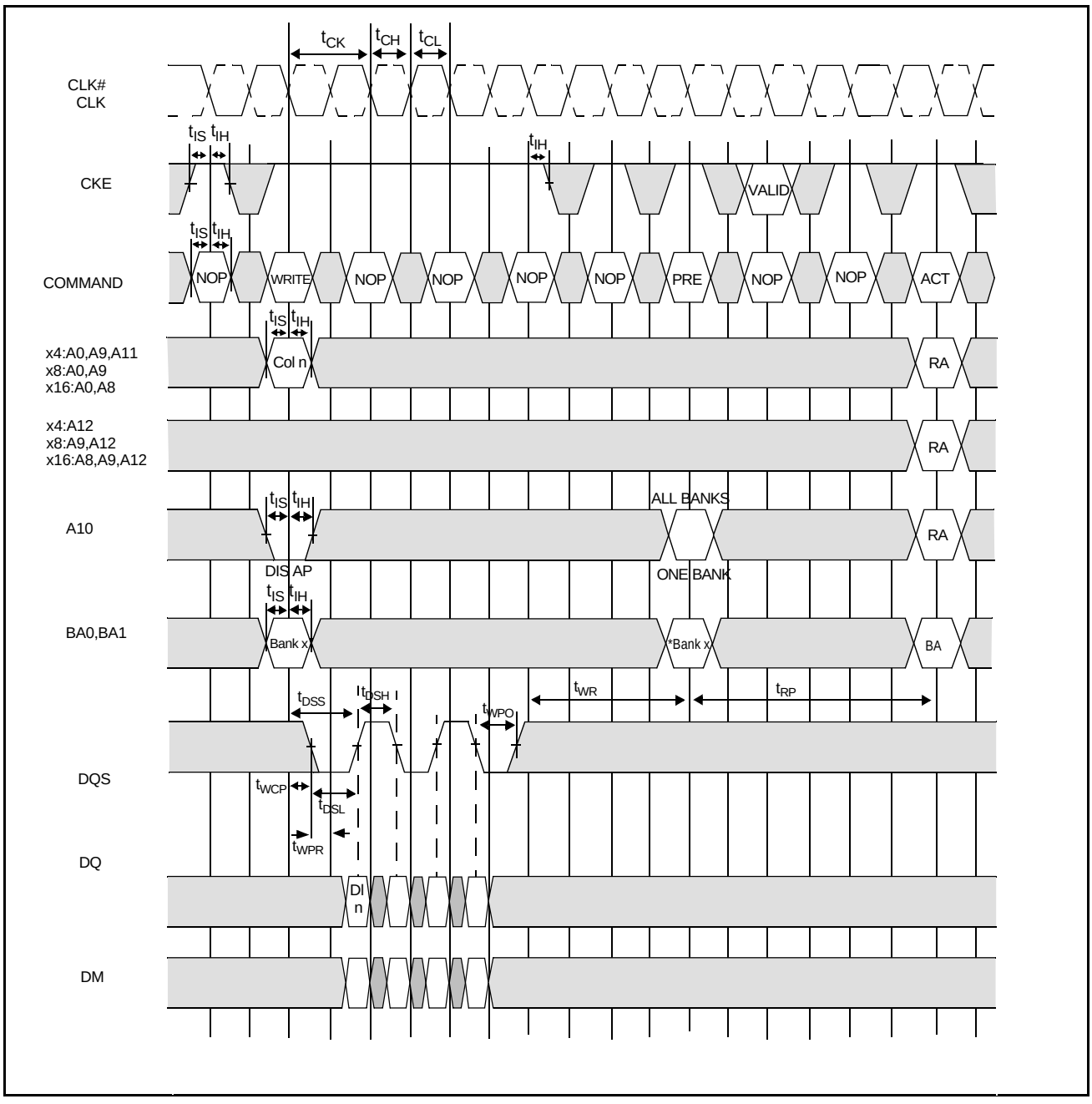
DO n=Data Out from column n
Burst Length=4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
EN AP=Enable Autoprecharge
ACT=ACTIVE, RA=Row Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

BANK READ ACCESS



DO n=Data Out from column n
Burst Length=4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP=Disable Autoprecharge
*="Dont Care", if A10 is HIGH at this point
PRE=PRECHARGE, ACT=ACTIVE, RA=Row Address, BA=Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

WRITE-WITHOUT AUTO PRECHARGE

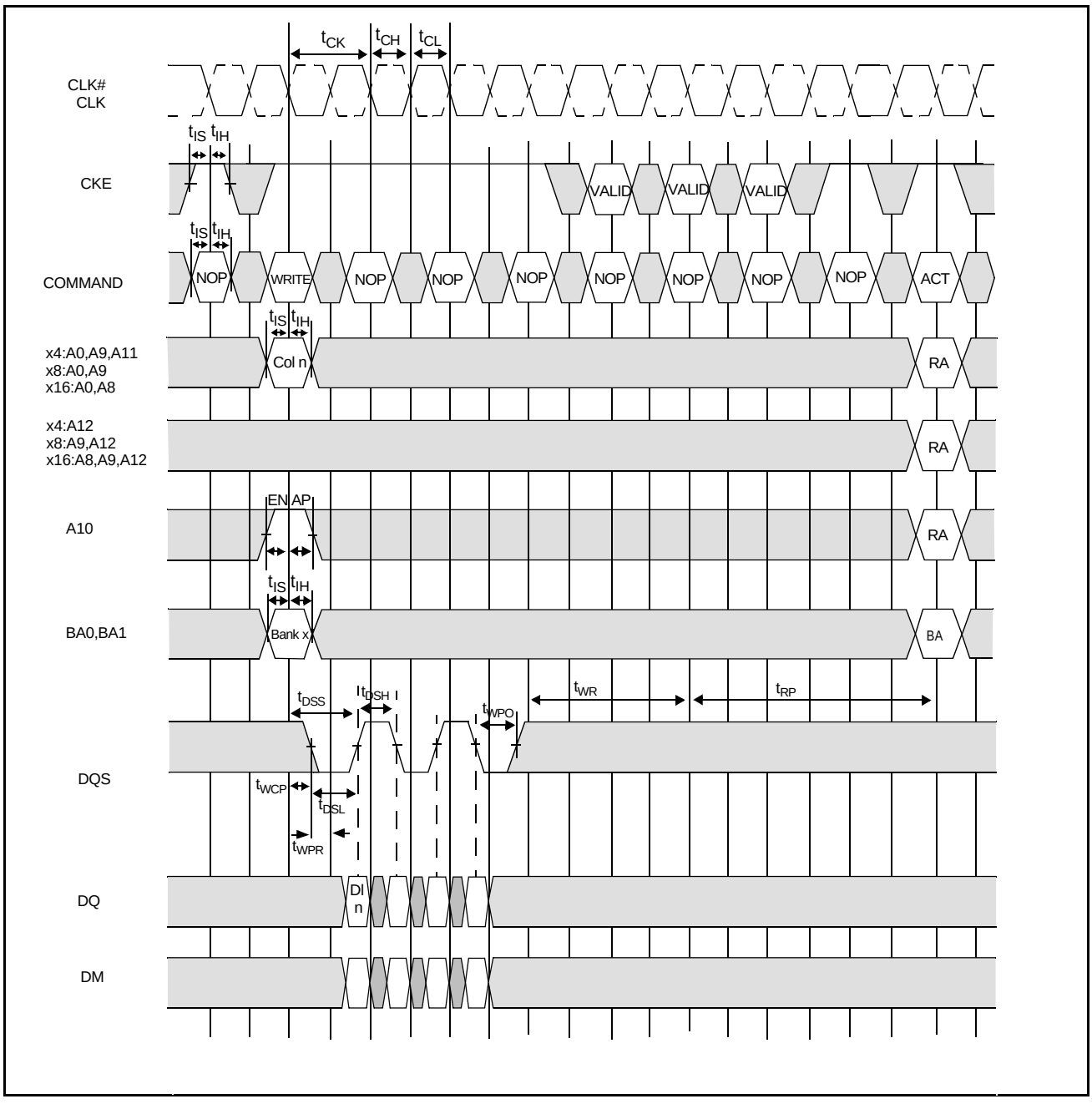


DONT CARE

UNDEFINED

DI n=Data In for column n
Burst Length=4 in the case shown
3 subsequent elements of Data In are provided in the programmed order following DI n
DIS AP=Disable Autoprecharge
*="Dont Care", if A10 is HIGH at this point
PRE=PRECHARGE, ACT=ACTIVE, RA=Row Address, BA=Bank Address
NOP commands are shown for ease of illustration; other commands may be possible at these times

WRITE-WITH AUTO PRECHARGE

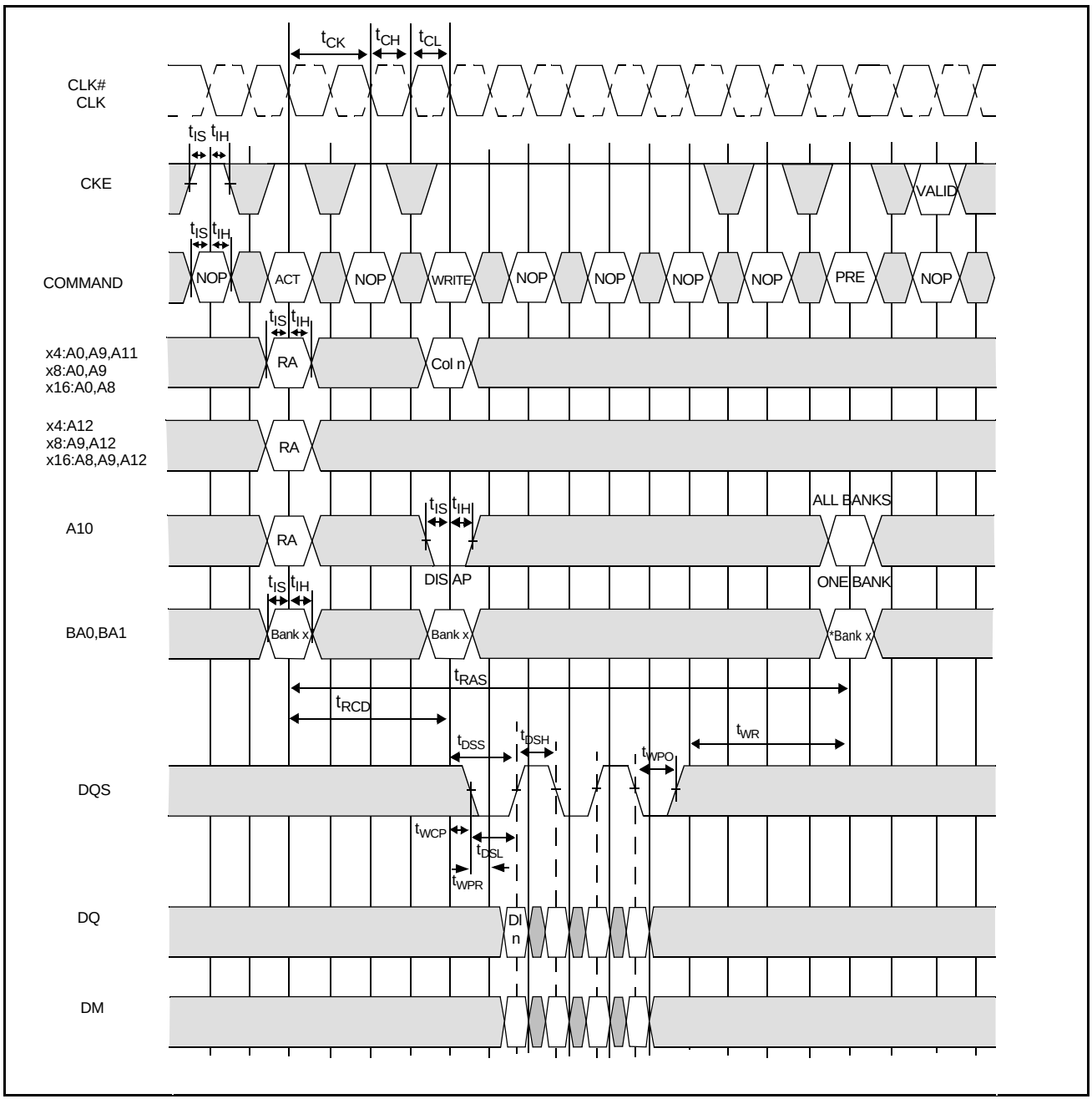


DONT CARE

UNDEFINED

DI n=Data In for column n
Burst Length=4 in the case shown
3 subsequent elements of Data In are provided in the programmed order following DI n
DIS AP=Disable Autoprecharge
*="Dont Care", if A10 is HIGH at this point
PRE=PRECHARGE, ACT=ACTIVE, RA=Row Address, BA=Bank Address
NOP commands are shown for ease of illustration; other commands may be possible at these times

BANK WRITE ACCESS

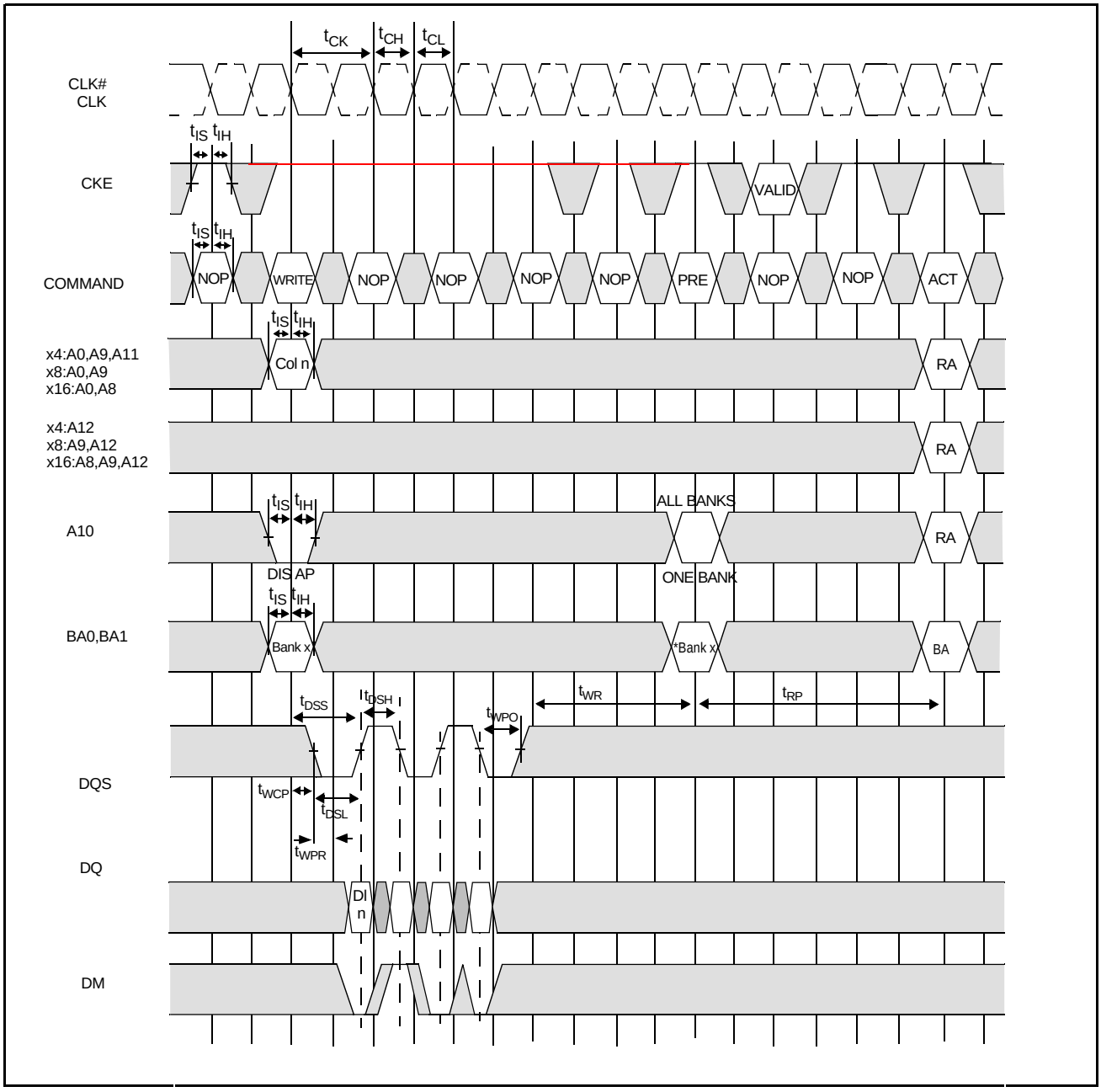


DONT CARE

UNDEFINED

DI n=Data In for column n
Burst Length=4 in the case shown
3 subsequent elements of Data In are provided in the programmed order following DI n
DIS AP=Disable Autoprecharge
*="Dont Care", if A10 is HIGH at this point
PRE=PRECHARGE, ACT=ACTIVE, RA=Row Address, BA=Bank Address
NOP commands are shown for ease of illustration; other commands may be possible at these times

WRITE-DQM OPERATION



DONT CARE

UNDEFINED

DI n=Data In for column n
Burst Length=4 in the case shown
3 subsequent elements of Data In are provided in the programmed order following DI n (The second element of the four is masked)
DIS AP=Disable Autoprecharge
*="Dont Care", if A10 is HIGH at this point
PRE=PRECHARGE, ACT=ACTIVE, RA=Row Address, BA=Bank Address
NOP commands are shown for ease of illustration; other commands may be possible at these times