VISION VV5404 Monolithic Sensor

CIF Format Digital Image Sensor

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PRELIMINARY DATASHEET

CHARACTERISTICS

- CIF Format

- Variable frame rate:
  30/15/7.5/3.75 fps & 25/12.5/6.25/3.125 fps

- On-chip 8-bit A/D convertor

- 4-wire digital video bus

- Serial control interface

- Programmable exposure and gain values

- Automatic black level calibration

- Low power

- Industry Standard 48 Pin LCC Package

GENERAL DESCRIPTION

VV5404 is a highly-integrated CMOS VLSI sensor targetted to video-conferencing applications. In addition to a 356 x 292 pixel image sensor array, it includes on-chip circuitry to drive and sense the array.

The output stage of the sensor contains a two stage flash 8-bit analogue-to-digital converter.

Device set-up is fully automatic via the CMOS sensor's built in automatic black level calibration algorithm.

The main features of the sensor's digital interface are as follows:

1. Tri-stateable 4-wire output video databus for 8-bit video data. Frame and line format information is encoded within the video output data stream.
2. A serial interface for controlling the operation of the sensor.
3. Data qualification clock, QCK (Tri-stateable)
4. Frame synchronisation signal, FST (Tri-stateable)

Exposure and gain values are programmed via the bi-directional 2-wire serial interface.

TECHNICAL SPECIFICATION

Pixel Resolution	356 x 292
Pixel Size	12.0 μm x 11.0 μm
Array Size	4.272 mm x 3.212 mm
Exposure control	25000:1
Format	CIF
Sensitivity	0.5 lux (with F2 lens @ 30fps)

SNR	52 dB
Supply Voltage	5.0 V DC +/- 5%
Supply Current	< 75 mA
Operating Temperature Range	0°C - 40°C
Technology	0.8um 2-Level Metal CMOS

Important:

1. VV5404 does NOT have any form of automatic exposure control. This must be performed externally.

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1. Introduction

VV5404 is a CIF format MOS image sensor module capable of outputing digital pixel data at frame rates of upto 30 frames per second.

The 356 x 292 pixel CMOS image sensor has an on-chip 8-bit analogue to digital converter (Figure 1). The sensor's offers a very flexible digital interface, the main components of which are listed below:

1. A tri-stateable 4-wire data bus (D[3:0]) for sending both video data and embedded timing references.
2. A data qualification clock, QCK, which can be programmable via the serial interface to behave in a number of different ways (Tri-stateable).
3. A frame start signal, FST (Tri-stateable).
4. A serial interface (SDA,SCL) for controlling and setting up the device.
5. The ability to synchronise the operation of multiple cameras - synchronisation input, SIN.

An 8-bit pixel value is transmitted across the 4 wire tri-stateable databus as series pair of 4-bit nibbles, most significant nibble first. Along within the pixel data, codes representing the start and end frames and the start and end of lines are embedded within the video data stream to allow synchronisation with video data the camera module is generating. Section 4. defines the format for the output video datastream.
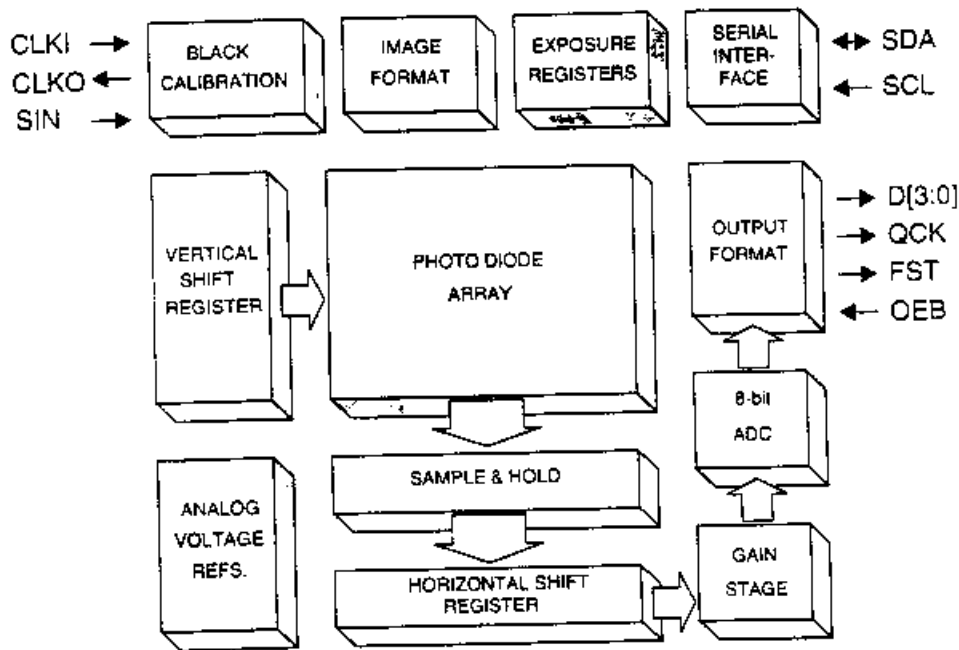
Figure 1 : Block Diagram of VV5404 Image Sensor

To complement the embedded control sequences a data qualification clock, QCK, and a frame start signal are also available. QCK can be set-up to either be:

1. Disabled
2. Free-running.
3. Qualify only the control sequences and the pixel data.
4. Qualify the pixel data only

The is also the choice of two different QCK frequencies where one is twice the frequency of the other.

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1. Fast QCK: the falling edge of the clock qualifies the nibble data irrespective of whether it is the most or the least signifcant nibble.
2. Slow QCK: the rising edge of the clock qualifies the most significant nibbles while the falling edge of the clock qualifies the least significant nibbles.

The FST can be enabled/disabled via the serial interface.

OEB tri-states all 4 databus lines, D[3:0], the qualification clock, QCK and the frame start signal, FST. The main way of interfacing to the VV5404 sensor based on the above signals is that the capture hardware uses a free-running QCK supplied by the sensor to sample the incoming video data stream. The embedded control sequences are used to synchronise the frame and line level timings. A crystal is used to generate the clock for the sensor.

The serial interface provides complete control over how the sensor is setup and run. Exposure and gain values are programmed via this interface. Section 5. defines the communications protocol and the register map of all the locations which can be accessed via the serial interface.
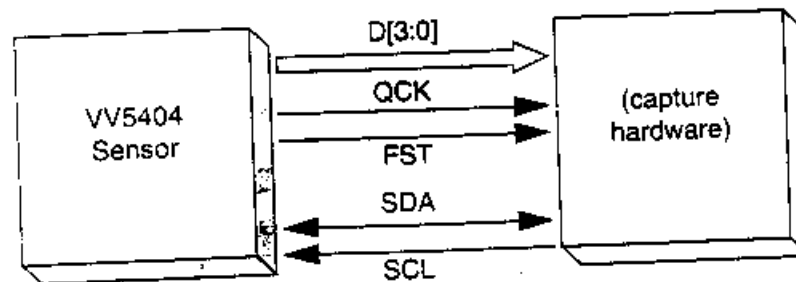
Figure 2 : Interfacing Options

It is possible to control the sensor and receive video data via a connection between the sensor and the capture hardware. The various image readout and frame rate options are detailled in Sections 2 and 3, respectively.

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2. Operating Modes

2.1 Image Readout Options

The output image format is CIF (352 x 288 pixel array). An optional border 2 pixels deep on all 4 sides of the array can be enabled (Figure 4). The resulting image size of 356 x 292 pixels is the default power up state for this camera module. The border option is programmable via the serial interface.

Border	Image size (column x row)	
Disabled	352 x 288	
Enabled	356 x 292	Default

Table 1 : Image Format Selection.

Image readout is non-interlaced raster scan.

2.2 Frame Rate Options

Two options: 30 fps or 25 fps (Assuming a 7.15909 MHz input clock and the default clock divder setting). 30 fps is the default option, the frame rate is programmable via the serial interface.

Frame Rate (fps)	Frame Timing (Pixels x Lines)	
25	471 x 304	
30	393 x 304	default

Table 2 : Frame Rate Selection

3. Exposure Control

The exposure time for a pixel and the gain of the input amplifier to the 8-bit ADC are programmable via the serial interface. The explanation below assumes that the gain and exposure values are updated together as part of a 5 byte serial interface auto-increment sequence.

The exposure is divided into 2 components - coarse and fine. The coarse exposure value sets the number of lines a pixel exposes for, while the fine exposure sets the number of additonal pixel clock cycles a pixel integrates for. The sum of the two gives the overall exposure time for the pixel array.

30 fps mode: Exposure Time = 2 x (Coarse x 393 + Fine) x (CKI clock period)/

25 fps mode: Exposure Time = 2 x (Coarse x 471 + Fine) x (CKI clock period)

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Value	Units	30 fps mode		25 fps mode	
		Min	Max	Min	Max
Coarse	Video Lines	0	302	0	302
Fine	Pixel Clocks	0	356	0	434

Table 3 : Coarse and Fine Exposure Ranges.

If an exposure value is loaded outwith the valid ranges listed in the above table the value is clipped to lie within the above ranges.

Gain Code, G[2:0]			Amplifier Gain
0	0	0	1
0	0	1	2
0	1	1	4
1	1	1	8

Table 4 : Main Gain Steps.

Exposure and gain values are re-timed within the sensor to ensure that a new set of values is only applied to the sensor array at the start of each frame. Bit 0 of the Status Register is set high when a new exposure value is written via the serial interface but has not yet been applied to the sensor array.

There is a 1 frame latency between a new exposure value being applied to the sensor array and the results of the new exposure value being readout. The same latency does not exist for the gain value. To ensure that the new exposure and gain values are aligned up correctly the sensor delays the application of the new gain value by one frame relative to the appilcation of the new exposure value.

To eliminate the possibility of the sensor array seeing only part of the new exposure and gain setting, if the serial interface communications extends over a frame boundary, the internal re-timing of exposure and gain data is disabled while writing data to any location in the Exposure page of the serial interface register map. Thus if the 5 bytes of exposure and gain data is sent as an auto-increment sequence, it is not possible for the sensor to consume only part of the new exposure and gain data.

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4. Digital Video Interface Format

4.1 General description

The video interface consists of a unidirectional, tri-stateable 4-wire databus. The nibble transmission is synchronised to the rising edge of the system clock (Figure 10).

Readout Order	Progressive Scan (Non-interlaced)
Form of encoding	Uniformly quantised, PCM, 8 bits per sample
Correspondence between video signal levels and quantisation levels:	Internally valid pixel data is clipped to ensure that 00_H and FF_H values do not occur when pixel data is being output on the data bus. This gives 254 possible values for each pixel (1 - 254). The video black level corresponds to code 16.

Table 5 : Video encoding parameters

Digital video data is 8 bits per sample, transmitted as serial pairs of parallel 4-bit nibbles (most significant nibble first) on 4 wires.

Multiplexed with the sampled pixel data is control information including both video timing references and sensor status/configuration data. Video timing reference information takes the form of field start characters, line start characters, end of line characters and a line counter.

Where hexadecimal values are used they are indicated by a subscript H, such as FF_H; other values are decimal.

4.2 Embedded control data

To distinguish the control data from the sampled video data all control data is encapsulated in embedded control sequences. These are a minimum of 6 words long and includes a combined escape/sync character, 1 control word (the 'command byte') and 2 words of supplementary data.

To minimise the susceptiblity of the embedded control data to random bit errors redundant coding techniques have been used to allow single bit errors in the embedded control words to be corrected. However, more serious corruption of control words or the corruption of escape/sync characters cannot be tolerated without loss of sync to the data stream. To ensure that a loss of sync is detected a simple set of rules has been devised. The four exceptions to the rules are outlined below:

1. Data containing a command word that has two bit errors.
2. Data containing two 'end of line' codes that are not separated by a 'start of line' code.
3. Data preceding an 'end of frame' code before a start of frame' code has been received.
4. Data containing line that do not have sequential line numbers (excluding the 'end of frame' line).

If the capture hardware detects one of these violations then it should abandon the current frame of video.

4.2.1 The combined escape and sync character

Each embedded control sequence begins with a combined escape and sync character that is made up of three words. The first two of these are FF_H FF_H- constituting two words that are illegal in normal data. The next word is 00_H - guaranteeing a clear signal transition that allows a capture hardware to determine the position of the word boundaries in the serial stream of nibbles. Combined escape and sync characters are always followed by a command word - making up the four word minimum embedded control sequence.

4.2.2 The command word

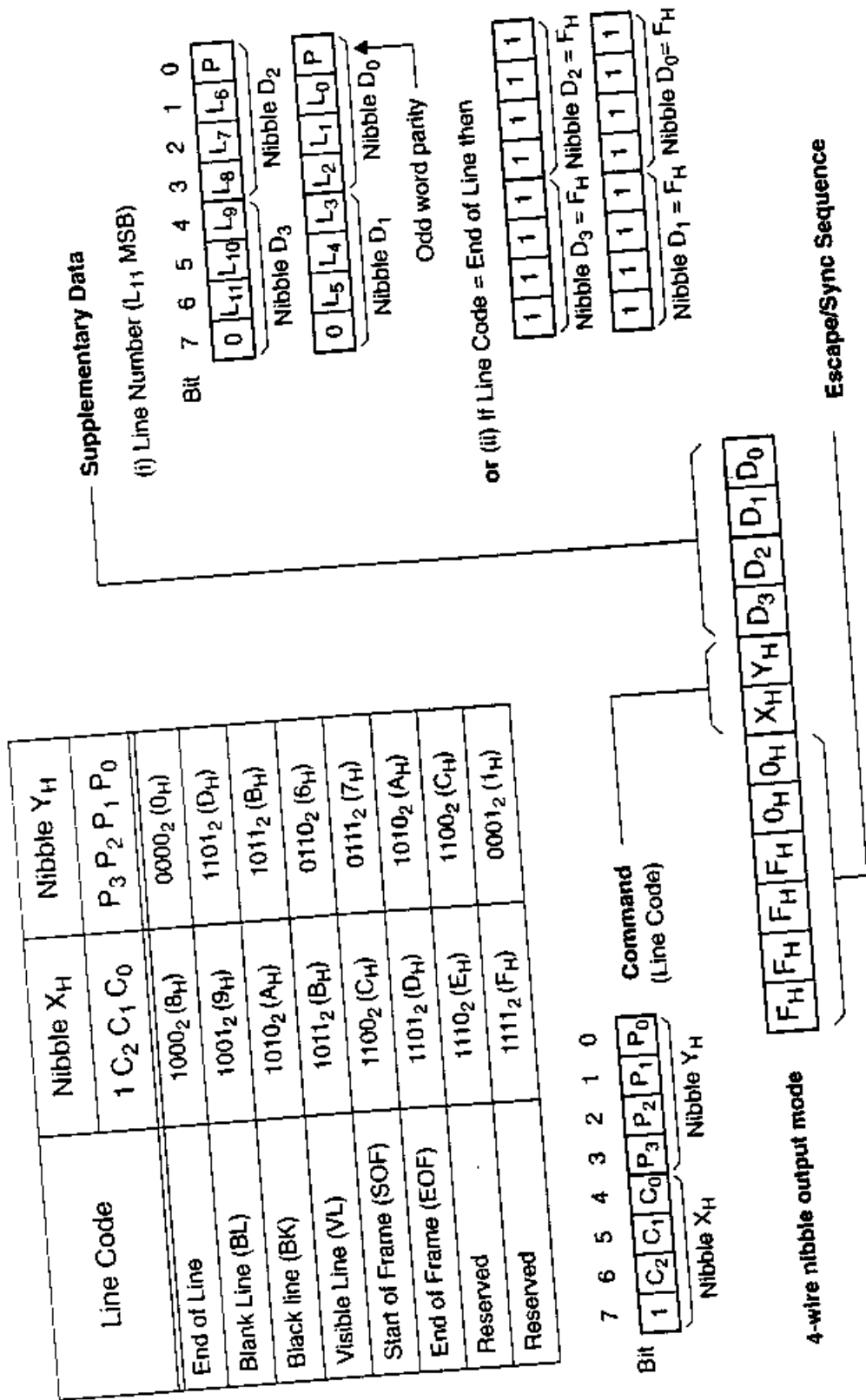The word that follows the combined escape/sync characters defines the type of embedded control data.

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Line Code	Nibble X_H $1\,C_2\,C_1\,C_0$	Nibble Y_H $P_3\,P_2\,P_1\,P_0$
End of Line	$1000_2\ (8_H)$	$0000_2\ (0_H)$
Blank Line (BL)	$1001_2\ (9_H)$	$1101_2\ (D_H)$
Black line (BK)	$1010_2\ (A_H)$	$1011_2\ (B_H)$
Visible Line (VL)	$1011_2\ (B_H)$	$0110_2\ (6_H)$
Start of Frame (SOF)	$1100_2\ (C_H)$	$0111_2\ (7_H)$
End of Frame (EOF)	$1101_2\ (D_H)$	$1010_2\ (A_H)$
Reserved	$1110_2\ (E_H)$	$1100_2\ (C_H)$
Reserved	$1111_2\ (F_H)$	$0001_2\ (1_H)$

Supplementary Data

(i) Line Number (L_{11} MSB)

Odd word parity

or (ii) If Line Code = End of Line then

Command (Line Code)

4-wire nibble output mode

Escape/Sync Sequence

Figure 3 : Emmbedded Control Sequence

Figure 4 : Frame Formats

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Figure 5 : Line Data Format.

P_M = Pixel Value - Most Significant Nibble, P_L = Pixel Value - Least Significant Nibble, P = 8-bit Pixel Value

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Three of the 8 bits are used to carry the control information, four are 'parity bits' that allow the capture hardware to detect and correct a certain level of errors in the transmission of the command words, the remaining bit is always set to 1 to ensure that the comand word never has the value 00_H. The coding scheme used allows the correction of single bit errors (in the 8-bit sequence) and the detection of 2 bit errors The three data bits of the command word are interpreted as shown in Figure 3.

Parity Checks				Comment
P_3	P_2	P_1	P_0	
X	X	X	X	Code word un-corrupted
X	X	X	✓	P_0 corrupted, line code OK
X	X	✓	X	P_1 corrupted, line code OK
X	✓	X	X	P_2 corrupted, line code OK
✓	X	X	X	P_3 corrupted, line code OK
✓	✓	X	✓	C_0 corrupted, invert sense of C_0
✓	X	✓	✓	C_1 corrupted, invert sense of C_1
X	✓	✓	✓	C_2 corrupted, invert sense of C_2
All other codes				2-bit error in code word.

Table 6 : Detection of 1-bit and 2-bit errors in the Command Word

The even parity bits are based on the following relationships:
1. An even number of ones in the 4-bit sequence (C_2, C_1, C_0 and P_0).
2. An even number of ones in the 3-bit sequence (C_2, C_1, P_1).
3. An even number of ones in the 3-bit sequence (C_2, C_0, P_2).
4. An even number of ones in the 3-bit sequence (C_1, C_0, P_3).

Table 6 shows how the parity bits maybe used to detect and correct 1-bit errors and detect 2-bit errors.

4.2.3 Supplementary Data

The last 2 bytes of the embedded control sequence contains supplementary data. This normally contains the current line number except if the line code is the end of line, the 2 bytes are padded out using null characters (FF_H). The 12 bit line number is packaged up by splitting it into two 6-bit values. Each 6-bit values is then converted into an 8-bit value by adding a zero to the start and an odd word parity bit at the end.

4.3 Video timing reference and status/configuration data

The video sequence is made up of lines of data. Each field of data is constructed of the following data lines:
1. A start of frame line
2. 2 of 'black lines' (used for black level calibration)
3. 7 (9) of blank lines
4. 292 (288) active video lines
5. An end of frame line
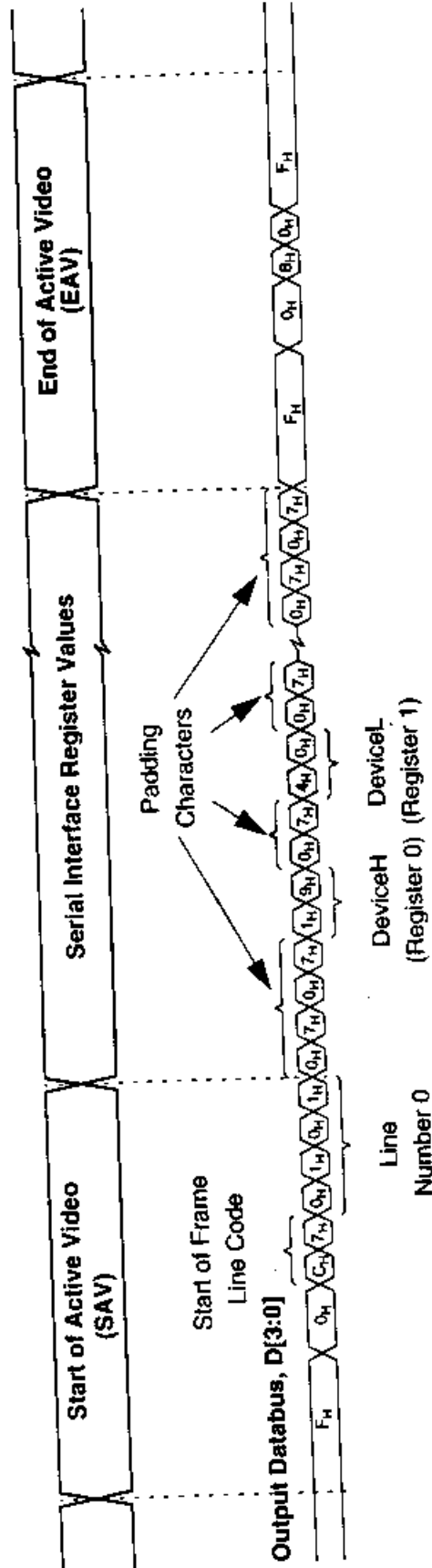6. 1 (3) blank lines

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Figure 6 : Status Line Data Format.

The numbers given in () are for when the border rows and columns are not output on the databus.
Each line of data starts with an embedded control sequence that identifies the line type (as outlined in Table 3). The control sequence is then followed by two bytes that, except in the case of the end-of-frame line, contain a coded line number. The line number sequences starts with the start-of-frame line at 00_H and increments one per line up until the end-of-frame line. Each line is terminated with an end-of-line embedded control sequence. The line start embedded sequences must be used to recognise data lines as a number of null bytes may be inserted between data lines.

4.3.1 Blank lines

In addition to padding between data lines, actual blank data lines may appear in the the positions indicated above. These lines begin with start-of-blank-line embedded control sequences and are constructed identically to active video lines except that they will contain only blank bytes (07_H).

4.3.2 Valid video line timing

All valid video data is contained on active video lines. The pixel data appears as a continuous stream of bytes within the active lines. The pixel data may be separated from the line header and end-of-line control sequence by a number of 'blank' bytes (07_H), e.g. when the border lines and pixels are disabled 07_H is output in place of pixels 0, 1, 354 and 355.

4.3.3 Start of frame line timing

The start of frame line which begins each video field contains no video data but instead contains the contents of all the serial interface registers. This information follows the start-of-line header immediately and is terminated by an end-of-line control sequence. To ensure that no escape/sync characters appear in the sensor status/configuration information the code 07_H is output after each serial interface value. Thus it takes 256 pixel clock periods (512 system clocks) to output all 128 of the serial interface registers. The remainder of the 356 pixel periods of the video portion of the line is padded out using 07_H values. The first two pixel locations are also padded with 07_H characters (Figure 6)

If a serial interface register location is unused then 07_H is output. The readout order of the registers is independent of whether the pixel readout order is shuffled or un-shuffled.

4.3.4 End of frame line timing

The end of frame line which begins each video field contains no video data. Its sole purpose is to indicate the end of a frame.

4.4 Resetting the Sensor Via the Serial Interface

Bit 2 of setup register 0 allows the VV5404 sensor to be reset to its power-on state via the serial interface. Setting this "Soft Reset" bit causes all of the serial interface registers including the "Soft Reset" bit to be reset to their default values. This "Soft Reset" leaves the sensor in low-power mode and thus an "Exit Low-Power Mode" command (Section 4.4.2) must be issued via the serial interface before the sensor will start to generate video data (Figure 7).

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4.4.1 Power-Up/Down (Figure 8)

On power-up all of the databus lines will go high Immediately (F_H), and the device enters it low-power mode (Section 4.4.2).

After the "Exit Low-Power Mode" command has been sent the sensor will output for one frame, a continuous stream of alternating 9_H and 6_H values on D[3:0]. By locking onto the resulting 0101/1010 patterns appearing on the data bus lines the capture hardware can determine the best sampling position for the nibble data. After the last 9_H 6_H pair has been output the databus returns to F_H until the start of fifth frame after CKI has been enabled when the first active frame output. After the capture hardware has determined the correct sampling position for the data, it should then wait for the next start of frame line (SOF).

If the capture hardware detects 32 consecutive 0_H values on the data bus, then the sensor has been removed. The sensor clock, CKI, should be held low.

4.4.2 Low-Power Mode (Figure 8)

Under the control of the serial interface the sensor analogue circuitry can be powered down and then be powered up. When the low-power bit is set via the serial interface, all the databus lines will go high at the end of the end of frame line of the current frame. At this point the analogue circuits in the sensor will power down. The system clock must remain active for the duration of low power mode.

Only the analogue circuits are powered down, the values of the serial interface registers e.g. exposure and gain are preserved.

The internal frame timing is reset to the start of a video frame on exiting low-power mode.

In a similar manner to the previous section, the first frame after the serial comms contains a continuous stream of alternating 9_H and 6_H to allow the capture hardware to re-confirm its sampling position. Then three frames latter the first start of frame line is generated.

4.4.3 Sleep Mode (Figure 9)

Sleep mode is similar to the low-power mode, except that analogue circuitry remains powered. When the sleep comand is received via the serial interface the pixel array will be put into reset and the data lines all will go high at the end of the current frame. Again the system clock must remain active for the duration of sleep mode.

When sleep mode is disabled, the CMOS sensor's frame timing is reset to the start of a frame. During the first frame after exiting from sleep mode the databus will remain high, while the exposure value propogrates through the pixel array. At the start of the second frame the first start of field line will be generated.

### 4.4.4 Application of the system clock during sensor low-power modes

For successfully entry and exit into and out of low power and 'sleep' modes the system clock, CLKI, must remain active for the duration of these modes.

4.5 Qualification of Output Data

There are two distinct ways for qualifing the data nibbles appearring of the output data bus

4.5.1 Using the External Clock signal applied to CKI

The data on the output data bus, changes on the rising edge of CKI. The delay between the capture hardware supplying a rising clock edge and the data on the databus becoming valid, depends on the length of the cable between the sensor and the capture hardware. To allow the capture hardware to find the best sampling position for the data nibbles, via the the serial interface the databus can be forced to output continuously 9_H,

Figure 7 : Reseting the VV5404 Sensor via the Serial Interface.
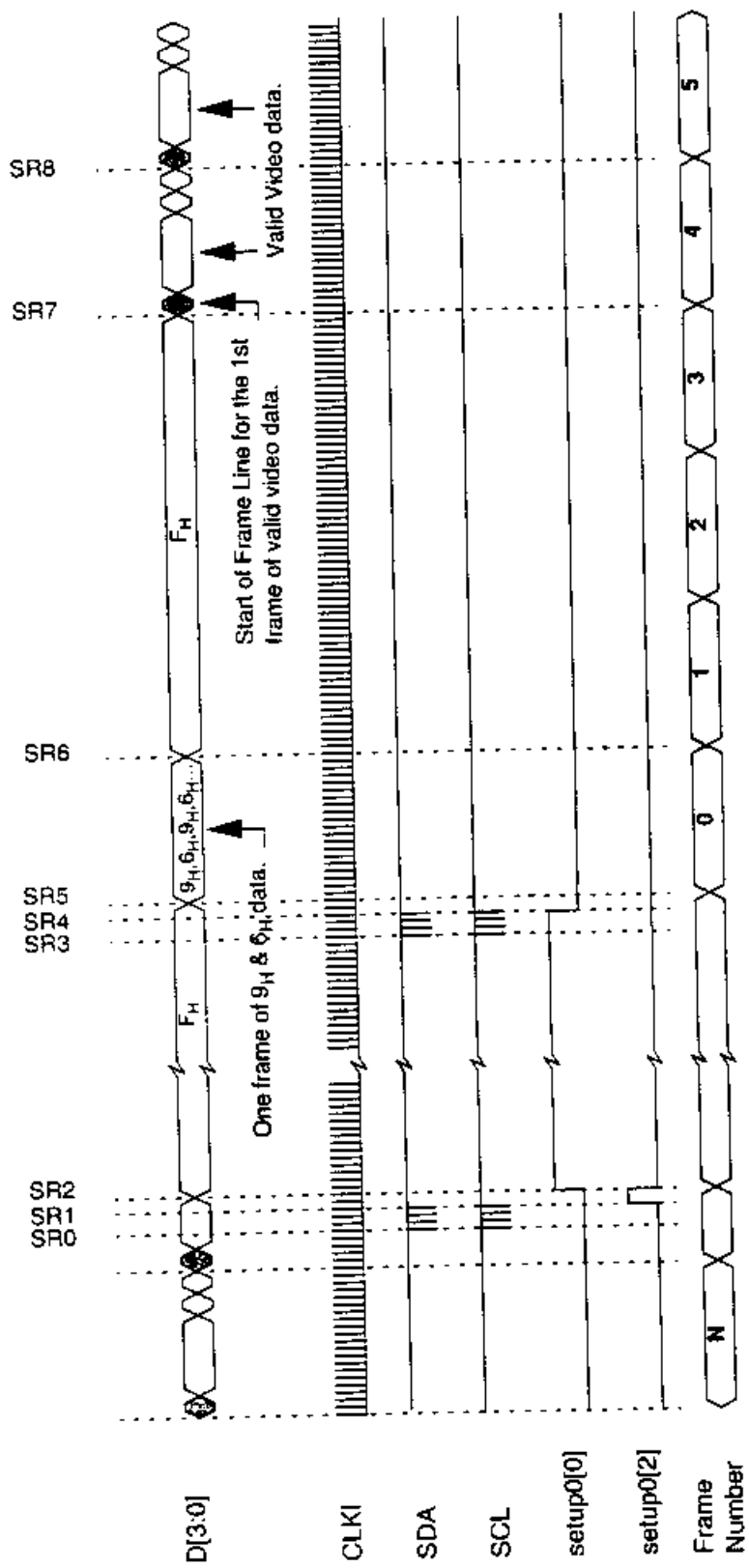
SR0-SR1	"Soft-Reset" Command. At the end of the command the sensor is reset and enters low-power mode.
SR2	The sensor enters low-power mode.
SR3-SR4	"Exit Low Power Mode" Command. Powers-up analogue circuits and initiates the VM5404 sensor's 4-frame start-up sequence
SR5-SR6	1 Frame of alternating 9_H & 6_H data on D[3:0] for the capture hardware to determine the best sampling phase for the nibble data (D[3:0]).
SR7-SR8	4 Frames after the "Exit Low-Power mode" command, the sensor starts outputing valid video data.

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LP0-LP1	"Enter Low Power Mode" Command.
LP2	At end of current frame, D[3:0] is set to F_H and the VM5404 sensor's analogue circuitry is powered down.
LP3-LP4	"Exit Low Power Mode" Command. Powers-up analogue circuits and initiates the VM5404 sensor's 4-frame start-up sequence
LP5-LP6	1 Frame of alternating 9_H & 6_H data on D[3:0] for the capture hardware to determine the best sampling phase for the nibble data (D[3:0]).
LP7-LP8	4 Frames after the "Exit low Power Mode" command, the sensor starts outputing valid video data.

Figure 8 : Entering and Exiting Low Power Mode.

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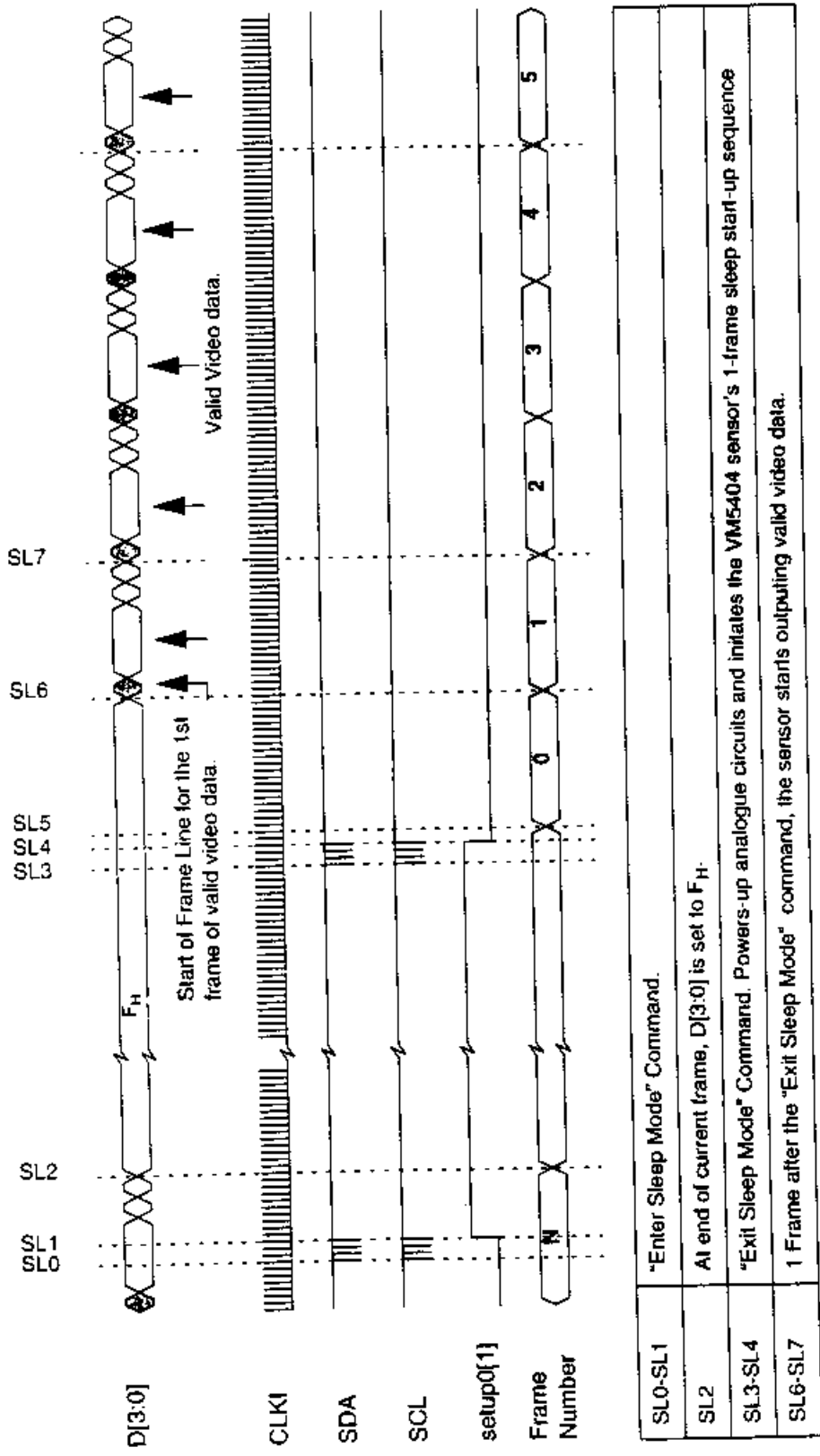
Figure 9 : Entering and Exiting Sleep Mode.

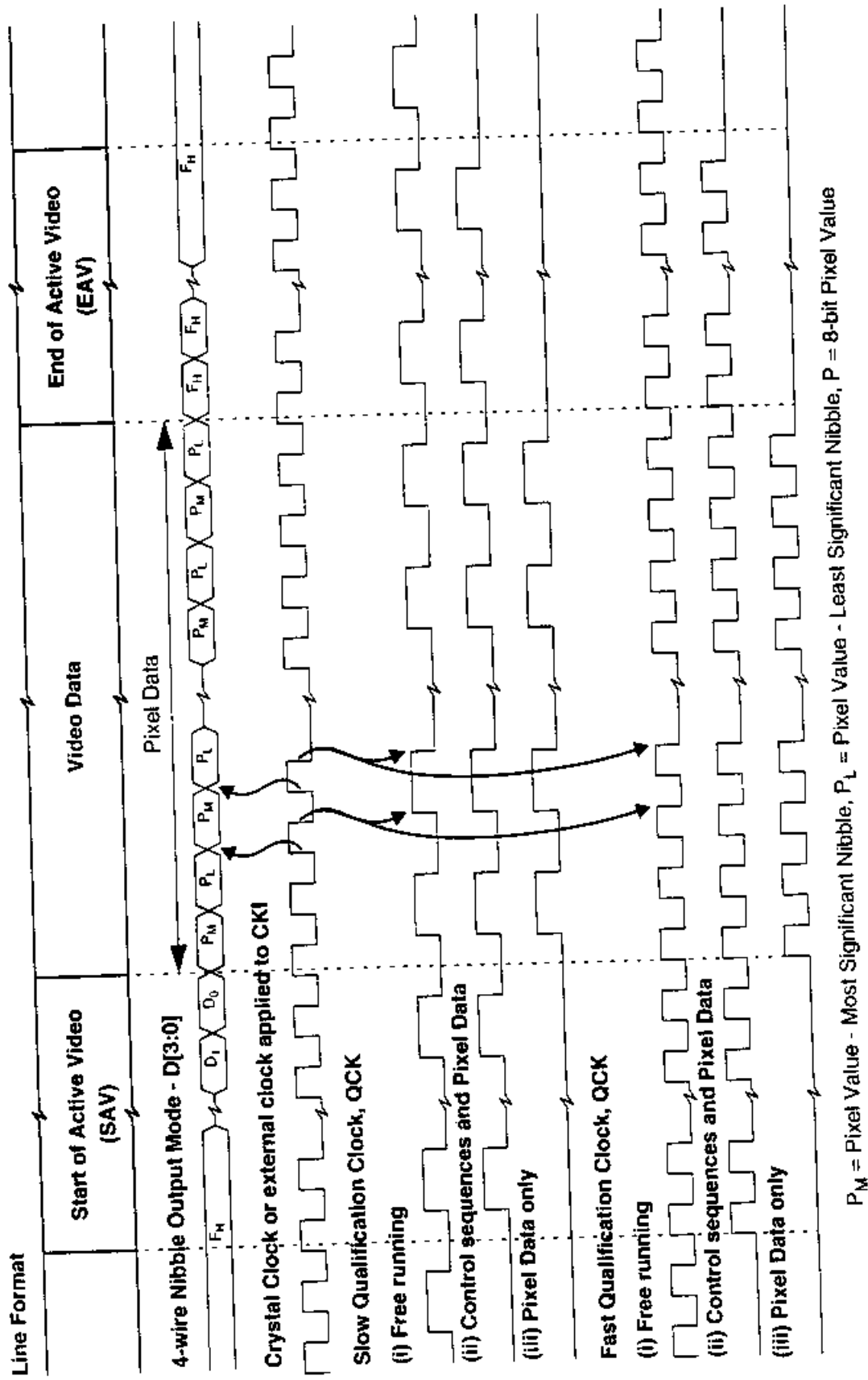| SL0-SL1 | "Enter Sleep Mode" Command. |
SL2	At end of current frame, D[3:0] is set to F_H.
SL3-SL4	"Exit Sleep Mode" Command. Powers-up analogue circuits and initiates the VM5404 sensor's 1-frame sleep start-up sequence
SL6-SL7	1 Frame after the "Exit Sleep Mode" command, the sensor starts outputting valid video data.

Figure 10 : Qualification of Output Data (Border Rows and Columns Enabled).

P_M = Pixel Value - Most Significant Nibble, P_L = Pixel Value - Least Significant Nibble, P = 8-bit Pixel Value

6_H, 9_H, 6_H, ...

4.5.2 Data Qualification Clock, QCK

VV5404 provides a data qualification clock for the output bus There are two frequencies for the qualification clock: one runs at the nibble rate and the other at the pixel readout rate. The falling edge of the fast QCK qualifies every nibble irrespective of whether it is most or least signifcant nibble. For the slow QCK, the rising edge qualifies the most significant nibbles in the output data stream and the falling edge qualifies the least significant nibbles in the output data stream.

There are 4 modes of operation of QCK.

1. Disabled (Always low - (Default)
2. Free running - qualifies the whole of the output data stream.
3. Emmbedded control sequences, status data and pixel data.
4. Pixel Data Only.

The operating mode for QCK is set via the serial interface. The QCK output is tristated when OEB is high. In one of the modes available via the serial interface the slow version of QCK will appear on the QCK pin while the fast version of the same signal will appear on the FST pin.

In the case where the border rows and columns are disabled, there is simply no qualification pulse at that point in time i.e. when pixels 0,1, 354 and 355 are normally output.

The QCK pin can also be configured to output the state of a serial interface register bit. This feature allows the sensor to control external devices, e.g. stepper motors, shutter mechanisms. The configuration details for QCK can be found in sections 5.5.7 and 5.5.8 of this document.

4.5.3 Frame Start Signal, FST

There are 3 modes of operation for the FST pin programmable via the serial interface:

1. Disabled (Always Low- Default).
2. Frame start signal. The FST signal occurs once frame, is high for 356 pixel periods (712 system clock periods) and qualifies the data in the start of frame line.
3. Synchronisation Output Pulse -SNO - Refer to Section 7. on Synchronising multiple cameras.

The FST is tristated when OEB is high.

The FST pin can also be configured to output the state of a serial interface register bit. This feature allows the sensor to control external devices, e.g. stepper motors, shutter mechanisms.

The configuration details for FST can be found in sections 5.5.7 and 5.5.8 of this document.
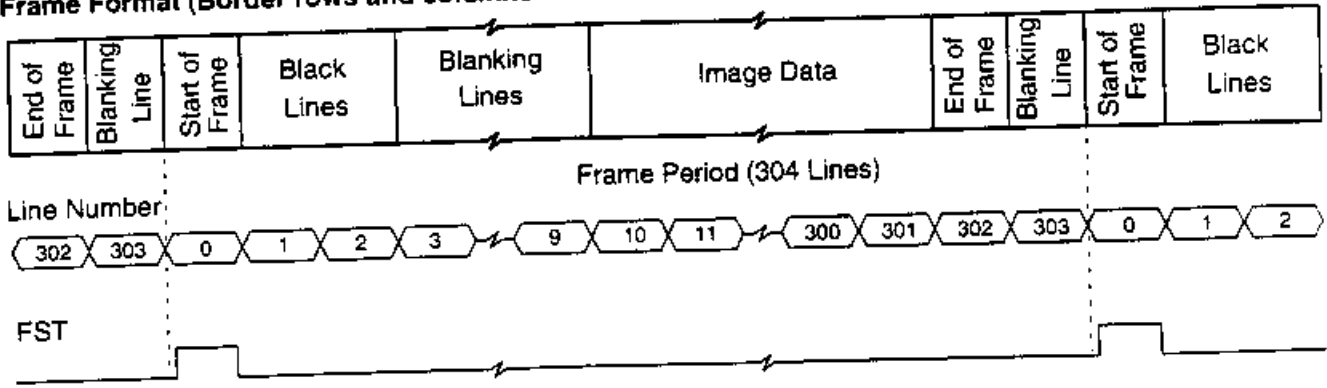
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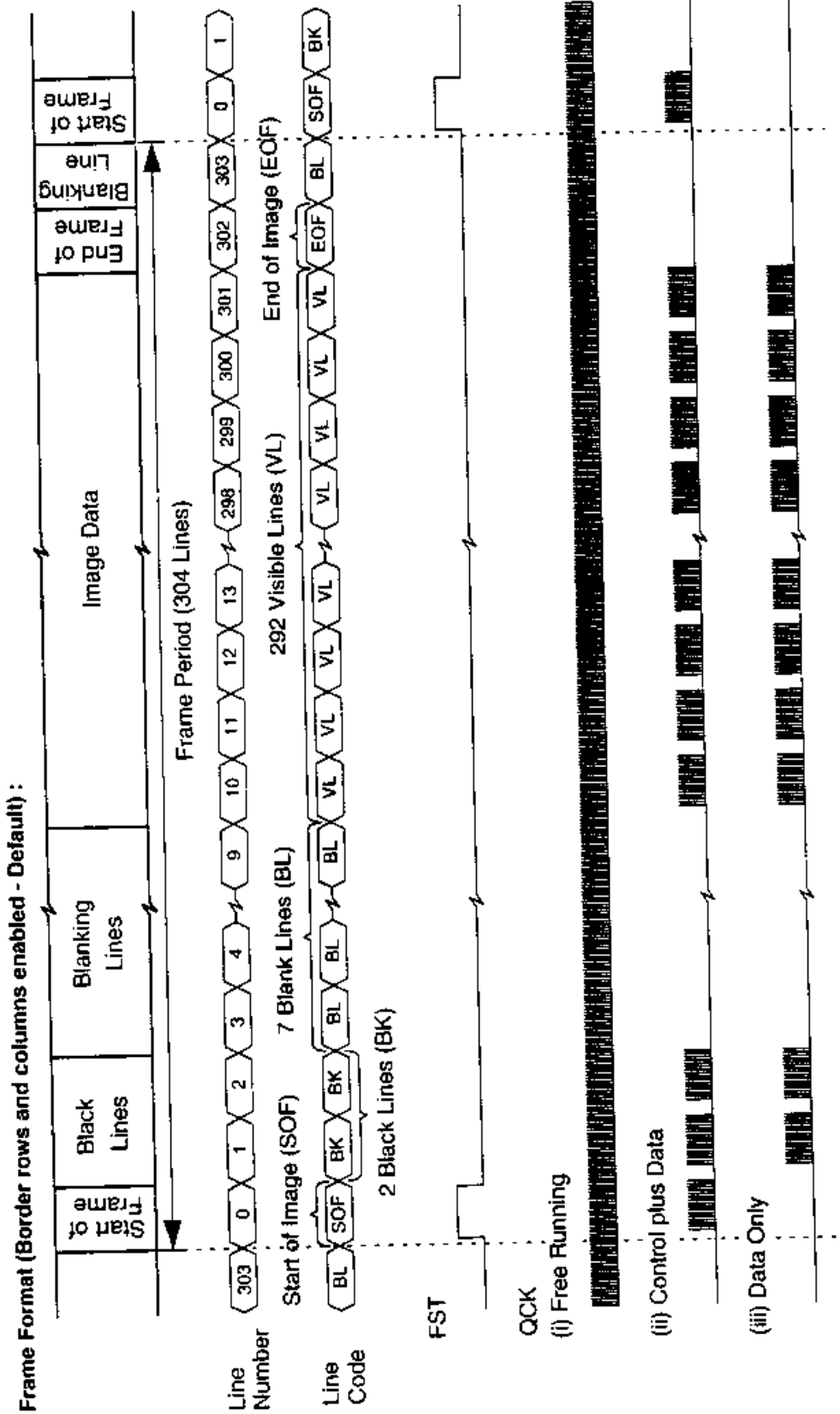
Figure 11 : Frame Level Timings for FST and QCK (Border Rows and Columns Enabled).

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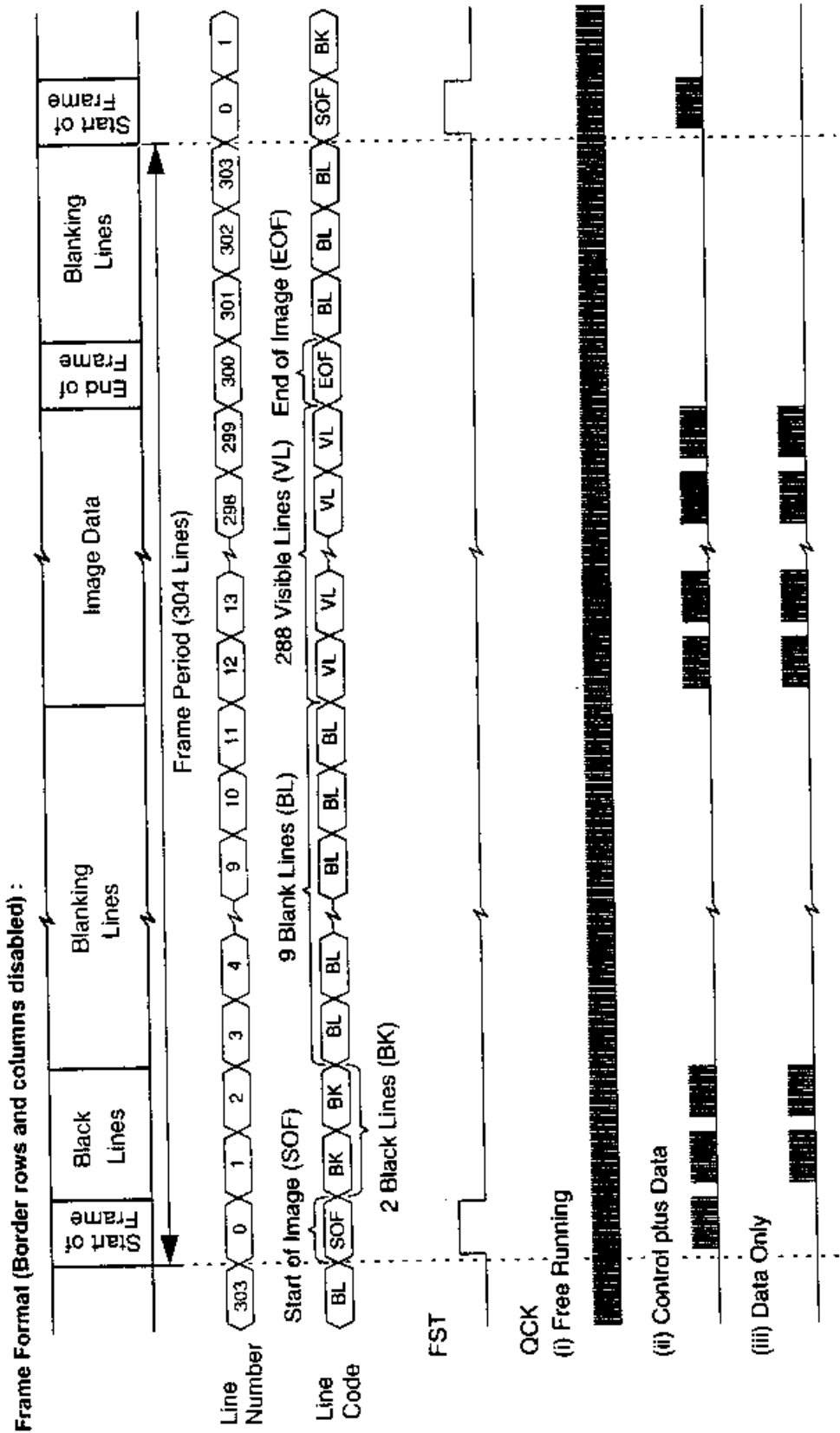
Figure 12 : Frame Level Timings for FST and QCK (Border Rows and Columns Disabled).

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Frame Format (Border rows and columns enabled in example) :

End of Frame	Blanking Line	Start of Frame	Black Lines	Blanking Lines	Image Data	End of Frame	Blanking Line	Start of Frame	Black Lines

Frame Period (304 Lines)

Line Number

302 | 303 | 0 | 1 | 2 | 3 | 9 | 10 | 11 | 300 | 301 | 302 | 303 | 0 | 1 | 2

FST

Start of Frame Line Format :

Line Period (393 Pixel Periods - 30 fps, 471 Pixel Periods - 25 fps)

37 (115) Pixels — 356 Pixels

EAV		SAV	Status Information	EAV

33 (111) Pixels — 4 Pixels

FST
(i) Frame start pulse - qualifies status line information.
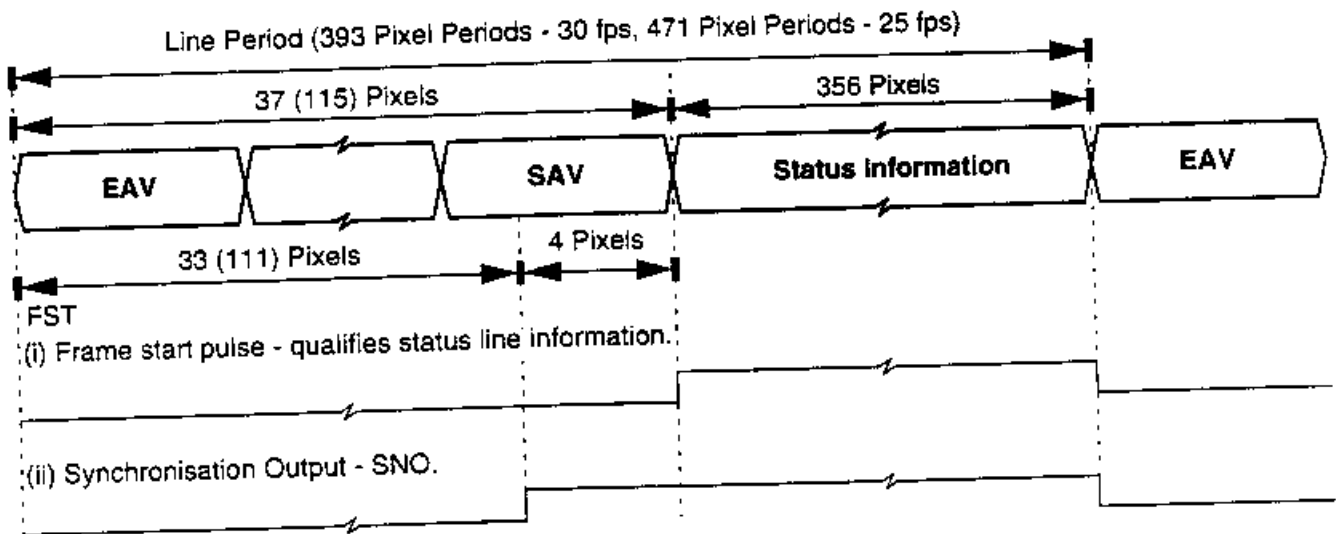
(ii) Synchronisation Output - SNO.

Figure 13 : FST Pin Waveforms.

5. Serial Control Bus

5.1 General Description

Writing configuration information to the video sensor and reading both sensor status and configuration information back from the sensor is performed via the serial interface.

Communication using the serial bus centres around a number of registers internal to the video sensor. These registers store sensor status, set-up, exposure and system information. Most of the registers are read/write allowing the receiving equipment to change their contents. Others (such as the chip id) are read only.

The main features of the serial interface include:

- Variable length read/write messages.
- Indexed addressing of information source or destination within the sensor.
- Automatic update of the index after a read of write message.
- Message abort with negative acknowledge from the master.
- Byte oriented messages.

The contents of all internal registers accessible via the serial control bus are encapsulated in each start-of-field line - see Section 4.3.3.

5.2 Serial Communication Protocol

The capture hardware must perform the role of a communications master and the camera acts as either a slave receiver or transmitter.The communication from host to camera takes the form of 8-bit data with a maximum serial clock frequency of up to 100 kHz. Since the serial clock is generated by the host it determines the data transfer rate. The bus address for the sensor In VV5404 is 20_H and for the serial E^2PROM containing the defect map it is $A0_H$. Data transfer protocol on the bus is shown below.
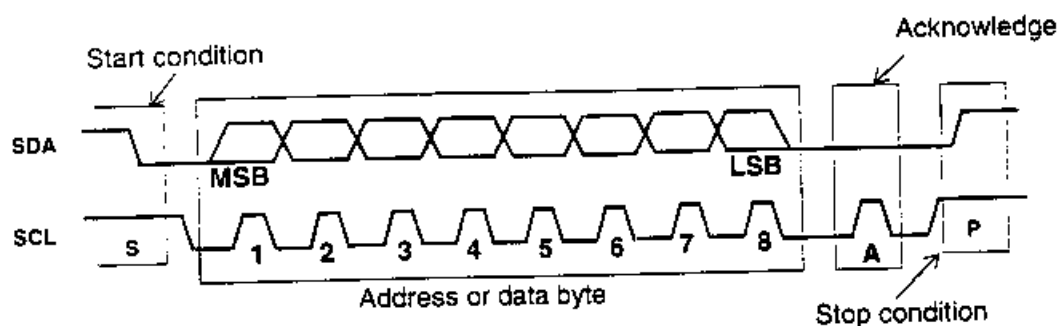

Figure 14 : Serial Interface Data Transfer Protocol

5.3 Data Format

Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit. The internal data is produced by sampling *sda* at a rising edge of *scl.* The external data must be stable during the high period of *scl.* The exceptions to this are *start* (S) or *stop* (P) conditions when *sda* falls or rises respectively, while *scl* is high.

A message contains at least two bytes preceded by a *start* condition and followed by either a *stop* or *repeated start, (Sr),* followed by another message.

The first byte contains the device address byte which includes the data direction *read,* (r), *–write,* (~w), bit. The device address of VV5404 is fixed as $0010\_000\_[lsb]_2$. The lsb of the address byte indicates the

direction of the message. If the lsb is set high then the master will read data from the slave and if the lsb is reset low then the master will write data to the slave. After the *r,-w* bit is sampled, the data direction cannot be changed, until the next address byte with a new *r,-w* bit is received.

The byte following the address byte contains the address of the first data byte (also referred to as the *index*). The serial interface can address up to 128, byte registers. If the msb of the second byte is set the automatic increment feature of the address index is selected.
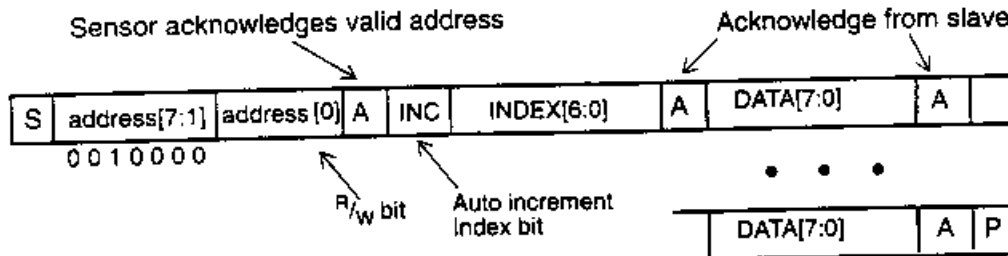

Figure 15 : Serial Interface Data Format

5.4 Message Interpretation

All serial interface communications with the sensor must begin with a *start* condition. If the *start* condition is followed by a valid address byte then further communications can take place. The sensor will acknowledge the receipt of a valid address by driving the *sda* wire low. The state of the *read/-write* bit (lsb of the address byte) is stored and the next byte of data, sampled from *sda*, can be interpreted.

During a write sequence the second byte received is an address index and is used to point to one of the internal registers. The msbit of the following byte is the *index auto increment* flag. If this flag is set then the serial interface will automatically increment the index address by one location after each slave acknowledge. The master can therefore send data bytes continuously to the slave unitl the slave fails to provide an acknowledge or the master terminates the write communication with a *stop* condition or sends a *repeated start, (Sr)*. If the auto increment feature is used the master does *not* have to send indexes to accompany the data bytes.

As data is received by the slave it is written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated. the data is then stored in the internal register addressed by the current index.

During a read message, the current index is read out in the byte following the device address byte. The next byte read from the slave device are the contents of the register addressed by the current index. The contents of this register are then parallel loaded into the serial/parallel register and clocked out of the device by *scl*.

At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device. Although VV5404 is always considered to be a slave device, it acts as a transmitter when the bus master requests a read from the sensor.

At the end of a sequence of incremental reads or writes, the terminal index value in the register will be one *greater* the last location read from or written to. A subsequent read will use this index to begin retrieving data from the internal registers.

A message can only be terminated by the bus master, either by issuing a stop condition, a repeated start condition or by a negative acknowledge after reading a complete byte during a read operation.

5.5 The Programmers Model

There are 128, 8-bit registers within the camera, accessible by the user via the serial interface. They are grouped according to function with each group occupying a 16-byte page of the location address space. There are eight such groups. The primary categories are given below:

- Status Registers (Read Only).
- Setup registers with bit significant functions.
- Exposure parameters that influence output image brightness.
- System functions and analogue test bit significant registers.

Any internal register that can be written to can also be read from. There are a number of read only registers that contain device status information, (e.g. design revision details).

Names that end with H or L denote the most or least significant part of the internal register. Note that unused locations in the H byte are packed with zeroes.

Vision sensors that include a 2-wire serial interface are designed with a common address space. If a register parameter is unused in a design, but has been allocated an address in the generic design model, the location is referred to as *reserved*. If the user attempts to read from any of these *reserved* locations a default byte will be read back. In VV5404 this data is the LSByte of the device status word, address 000_0000. A write instruction to a reserved (but unused) location is illegal and would not be successful as the device would not allocate an internal register to the data word contained in the instruction.

A detailed description of each register follows. The address indexes are shown as binary numbers in brackets [ ].

	Index	Name	Length	R/W	Default	Comments
Status	000_0000	deviceH	8	RO	$0001\ 1001_2$	Chip identification number including revision indicator
	000_0001	deviceL	8	RO	$0100\ 0000_2$	
	000_0010	status0	8	RO	$0000\ 1000_2$	
	000_0011	line_countH	8	RO		Current line counter MSB value
	000_0100	line_countL	8	RO		Current line counter LSB value
	000_0101	unused				
	000_011x	unused				
	000_1xxx	unused				
Setup	001_0000	setup0	8	R/W	$0001\ 0001_2$	
	001_0001	setup1	8	R/W	$1100\ 0001_2$	
	001_0010	setup2	8	R/W	31	Contains pixel counter reset value used by external synch
	001_0011	reserved				
	001_0100	setup4	8	R/W	0	FST and QCK mode selects
	001_0101	setup5	8	R/W	0	FST and QCK mapping mode.
	001_011x	unused				
	001_1xxx	unused				

Table 7 : Serial Interface Address Map.

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	Index	Name	Length	R/W	Default	Comments
Exposure	010_0000	fineH	8	R/W	0	Fine exposure.
	010_0001	fineL	8	R/W		
	010_0010	coarseH	8	R/W	302	Coarse exposure
	010_0011	coarseL	8	R/W		
	010_0100	gain	3	R/W	0	ADC Pre-amp gain Setting
	010_0101	clk_div	2	R/W	0	Clock division
	010_0110	unused				
	010_0111	unused				
	010_1xxx	unused				
System	111_0000	bcal_window	8	R/W	0	
	111_0001	bcal0	8	R/W	128	Black calibration DAC0
	111_0010	bcal1	8	R/W	128	Black calibration DAC1
	111_0011	unused				
	111_0100	tms0	8	R/W	$0000\ 0000_2$	Test Mode Select Register
	111_0101	cr0	8	R/W	$0000\ 0000_2$	Analogue Control Register 0
	111_0110	cr1	8	R/W	$0000\ 0000_2$	Analogue Control Register 1
	111_0111	as0	8	R/W	$0100\ 0100_2$	ADC Setup Register
	111_1000	at0	8	R/W	$0000\ 0000_2$	Analogue Test Register
	111_1001	unused				
	111_101x	unused				
	111_11xx	unused				

Table 7 : Serial Interface Address Map.

5.5.1 Status0 [000_0010_2]

Bit	Function	Default	Comment
0	Exposure value update pending	0	Exposure sent but not yet consumed by the exposure controller
1	Gain value update pending	0	Gain value sent but not yet consumed by the exposure controller
2	Clock divisor update pending	0	Clock divisor sent but not yet consumed by the exposure controller
3	Black cal fail flag	0	If the black calibration has failed this flag will be raised. It will stay active until the last line of the next *successful* black calibration.
4	Odd/even frame	1	The flag will toggle state on alternate frames
7:5	Unused	000	

Table 8 : Status0 [000_0010_2]

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5.5.2 Line_count_H [000_0011$_2$] & Line_count_L [000_0100$_2$]

Register Index	Bits	Function	Default	Comment
000_0011$_2$	7:0	Current line count MSB	-	Displays current line count
000_0100$_2$	7:0	Current line count LSB	-	

Table 9 : Current Line Counter Value.

5.5.3 Setup0 [001_0000$_2$]

Bit	Function	Default	Comment
0	Low Power Mode: Off/On	1	Powers down the sensor array. The ouput databus goes to F$_H$. On power-up the sensor enters low power mode.
1	Sleep Mode: Off/On	0	Puts the sensor array into reset. The ouput databus goes to F$_H$.
2	Soft Reset Off/On	0	Seting this bit resets the sensor to its power-up deflauts. This bit is also reset.
3	Frame Rate select: 25 fps or **30 fps**	1	
4	Tri-state output data bus **Outputs Enabled**/Tristate	0	On power up the data output pads D[3:0] are enabled by default.
7:5	unused		

Table 10 : Setup0 [001_0000$_2$]

5.5.4 Setup1 [001_0001$_2$]

Bit	Function	Default	Comment
1:0	Black calibration mode selection	10	Black calibration trigger selection. Default setting bases decision on result of monitor test. See table below
2	reserved		
3	Enable immediate clock division update. **Off**/On	0	Allow manual change to clock division to be applied immediately
4	Enable immediate gain update. **Off**/On	0	Allow manual change to gain to be applied immediately
5	Enable additional black lines (lines 3-9) **Off**/On	0	If enabled this bit will also enable the line immediately following the end of frame line
6	Border rows and columns: Masked or **Output**	1	These extra pixels/rows are used in colour processing

Table 11 : Setup1 [001_0001$_2$]

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Black Cal Mode[1]	Black Cal Mode[0]	Comment
0	0	No black calibration
0	1	**Always** trigger black calibration
1	0	Black calibration triggered by a **failed** monitor test
1	1	Trigger black calibration only if the gain setting changes

Table 12 : Black Calibration Mode

If the gain change trigger option has been selected then care should be taken when writing the new gain value *if* the *immediate gain update* option has been selected. It is strongly advised that the user should *not* write a new gain value between line 0 (the status line) and line 9 (the last black calibration line). If the gain values are written in a timed manner then no restriction applies.

5.5.5 Setup2 [001_0010$_2$]

Bit	Function	Default	Comment
5:0	Pixel counter reset value	31	During synchronisation the pixel counter can be reset to the known value or offset by up to 63 pck's into the line count sequence.
7:6	Unused		

Table 13 : Setup2[001_0010$_2$]

5.5.6 Setup4 [001_0100$_2$]

Bit	Function	Default	Comment
1:0	FST/QCK pin modes	0	Selection of FST, QCK pin data
3:2	QCK modes	0	When to output QCK
5:4	reserved	0	reserved for LST modes in other sensors
7:6	FST modes	0	

Table 14 : Setup4[001_0100$_2$]

FST/QCK pin mode[1:0]		FST pin	QCK pin
0	0	FST	Slow QCK
0	1	FST	Fast QCK
1	0	Fast QCK	Slow QCK

Table 15 : FST/QCK Pin Selection

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FST/QCK pin mode[1:0]		FST pin	QCK pin
1	1	Invert of Fast QCK	Fast QCK

Table 15 : FST/QCK Pin Selection

QCK mode[1:0]		QCK state
0	0	Off
0	1	Free Running
1	0	Valid during data and control period of line
1	1	Valid only during data period of line

Table 16 : QCK Modes

FST mode[1:0]		FST state
0	0	Off
0	1	On - qualifies the status line
1	0	FST takes on the function of synchronisation output (SNO)
1	1	Unallocated

Table 17 : FST Modes

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5.5.7 Exposure Control Registers [010_0000$_2$] - [010_1001$_2$]

There is a set of programmable registers which controls the sensitivity of the sensor. The registers are as follows:

1. Fine exposure.
2. Coarse exposure time.
3. Gain.
4. Clock division.

The gain parameter does not affect the integration period rather it amplifies the video signal at the output stage of the sensor core.

Note: The external exposure (coarse, fine, clock division or gain) values do not take effect immediately. Data from the serial interface is read by the exposure algorithm at the start of a video frame. If the user reads an exposure value via the serial interface then the value reported will be the data as yet unconsumed by the exposure algorithm, because the serial interface logic locally stores all the data written to the sensor.

Between writing the exposure data and the point at which the data is consumed by the exposure logic, bit 0 of the status register is set. The gain value is updated a frame later than the coarse, fine and clock division parameters, since the gain is applied directly at the video output stage and does not require the long set up time of the coarse and fine exposure and the clock division.

To eliminate the possibility of the sensor array seeing only part of the new exposure and gain setting, if the serial interface communications extends over a frame boundary, the internal re-timing of exposure and gain data is disabled while writing data to any location in the Exposure page of the serial interface register map. Thus if the 5 bytes of exposure and gain data is sent as an auto-increment sequence, it is not possible for the sensor to consume only part of the new exposure and gain data.

The range of some parameter values is limited and any value programmed out-with this range will be clipped to the maximum allowed.

Register Index	Bits	Function	Default	Comment
010_0000$_2$	7:0	Fine MSB exposure value	0	Maximum mode dependent: 360 (30fps) / 438 (25 fps)
010_0001$_2$	7:0	Fine LSB exposure value		
010_0010$_2$	7:0	Coarse MSB exposure value	302	Maximum: 302
010_0011$_2$	7:0	Coarse LSB exposure value		
010_0100$_2$	2:0	Gain value	0	000 : Gain = 1 001 : Gain = 2 011 : Gain = 4 111 : Gain = 8
010_0101$_2$	1:0	Clock divisor value	0	00 : Pixel clock = CLKI clock/2 01 : Pixel clock = CLKI clock/4 10 : Pixel clock = CLKI clock/8 11 : Pixel clock = CLKI clock/16

Table 18 : Exposure, Clock Rate and Gain Registers

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5.5.8 Black Calibration Registers [111_0000$_2$] - [111_0010$_2$]

The sensor is equipped with an automatic function that continually monitors the output black level and calibrates if it has moved out of programmable range. The user is advised to disable the automatic function before attempting to write any of these parameters.

Register Index	Bits	Function	Default	Comment
111_0000$_2$	3:0	bcal_window	0	Black Level Monitor/Calibration Window Sizes
111_0001$_2$	7:0	bcal0	128	DAC B0 value
111_0010$_2$	7:0	bcal1	128	DAC B0 value

Table 19 : Black Calibration Registers

Bit	Function	Default	Comment
1:0	bcal_win	0	Black Calibration monitor window size
2	Monitor window size set by serial interface communication Yes/No	0	Allow the serial interface to set the Black Calibration monitor window size directly.
3	Narrow Black Cal target window Yes/No	0	By default the target window size for the Black Calibration (calibration phase) is set to the widest position
7:4	used	0	

Table 20 : Black Level Monitor/Calbration Window Sizes [001_0100$_2$]

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5.6 Types of messages

This section gives guidelines on the basic operations to read data from and write data to the serial interface.

The serial interface supports variable length messages. A message may contain no data bytes, one data byte or many data bytes. This data can be written to or read from common or different locations within the sensor. The range of instructions available are detailed below.

- Write no data byte, only sets the index for a subsequent read message.
- Single location multiple data write or read for monitoring (real time control)
- Multiple location, multiple data read or write for fast information transfers.

Examples of these operations are given below. A full description of the internal registers is given in the previous section. For all examples the slave address used is 32_{10} for writing and 33_{10} for reading. The write address includes the read/write bit (the lsb) set to zero while this bit is set in the read address.

5.6.1 Single location, single data write.

When a random value is written to the sensor, the message will look like this:
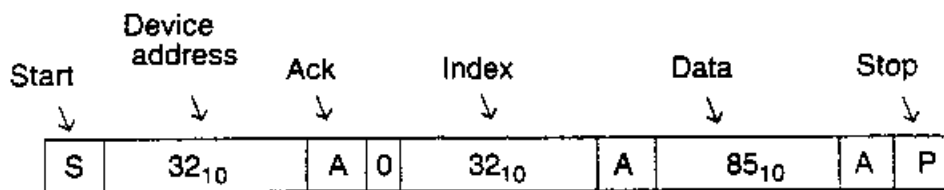
Start	Device address	Ack		Index		Data		Stop
S	32_{10}	A	0	32_{10}	A	85_{10}	A	P

Figure 16 : Single location, single write.

In this example, the *fineH* exposure register (index = 32_{10}) is set to 85_{10}. The r/w bit is set to zero for writing and the *inc* bit (msbit of the index byte) is set to zero to disable automatic increment of the index after writing the value. The address index is preserved and may be used by a subsequent read. The write message is terminated with a stop condition from the master.

5.6.2 Single location, single data read.

A read message always contains the index used to get the first byte.
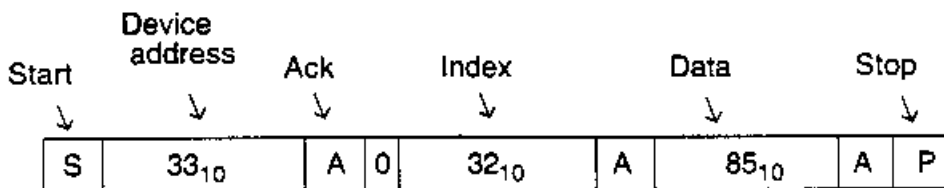
Start	Device address	Ack		Index		Data		Stop
S	33_{10}	A	0	32_{10}	A	85_{10}	A	P

Figure 17 : Single location, single read.

This example assumes that a write message has already taken place and the residual index value is 32_{10}. A value of 85_{10} is read from the *fineH* exposure register. Note that the read message is terminated with a negative acknowledge ($\overline{A}$) from the master: it is not guaranteed that the master will be able to issue a stop condition at any other time during a read message. This is because if the data sent by the slave is all zeros, the *sda* line cannot rise, which is part of the stop condition.

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5.6.3 No data write followed by same location read.

When a location is to be read, but the value of the stored index is not known, a write message with no data byte must be written first, specifying the index. The read message then completes the message sequence. To avoid relinquishing the serial to bus to another master a repeated start condition is asserted between the write and read messages. In this example, the *gain* value (index = 36_{10}) is read as 15_{10}:
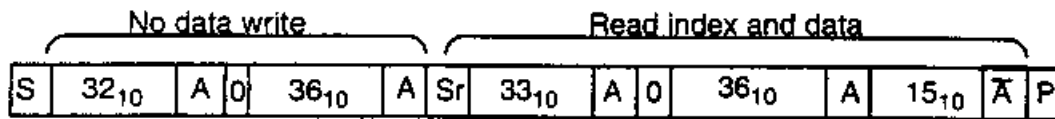
S	32_{10}	A	0	36_{10}	A	Sr	33_{10}	A	0	36_{10}	A	15_{10}	$\overline{A}$	P

No data write / Read index and data

Figure 18 : No data write followed by same location read.

As mentioned in the previous example, the read message is terminated with a negative acknowledge ($\overline{A}$) from the master.

5.6.4 Same location multiple data write.

It may be desirable to write a succession of data to a common location. This is useful when the status of a bit,(e.g. requesting a new black calibration), must be toggled.

The message sequence indexes *setup1* register. If bit 1 is toggled low, high low this will initiate a fresh black calibration. This is achieved by writing three consecutive data bytes to the sensor. There is no requirement to re-send the register index before each data byte.
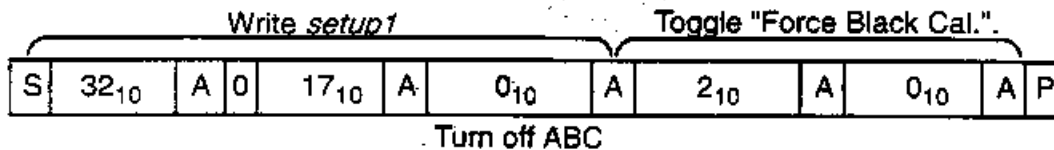
S	32_{10}	A	0	17_{10}	A	0_{10}	A	2_{10}	A	0_{10}	A	P

Write *setup1* / Toggle "Force Black Cal.".

Turn off ABC

Figure 19 : Same location multiple data write.

5.6.5 Same location multiple data read

When an exposure related value (*fineH, fineL, coarseH, coarse L, gain or clk_div*) is written, it takes effect on the output at the beginning of the next video frame, (remember that the application of the *gain* value is a frame later than the other exposure parameters). To signal the consumption of the written value, a flag is set when any of the exposure or gain registers are written and is reset at the start of the next frame. This flag appears in *status0* register and may be monitored by the bus master. To speed up reading from this location, the sensor will repeatedly transmit the current value of the register, as long as the master acknowledges each byte read.

In the next example, a *fineH* exposure value of 0 is written, the status register is addressed (no data byte) and then constantly read until the master terminates the read message.
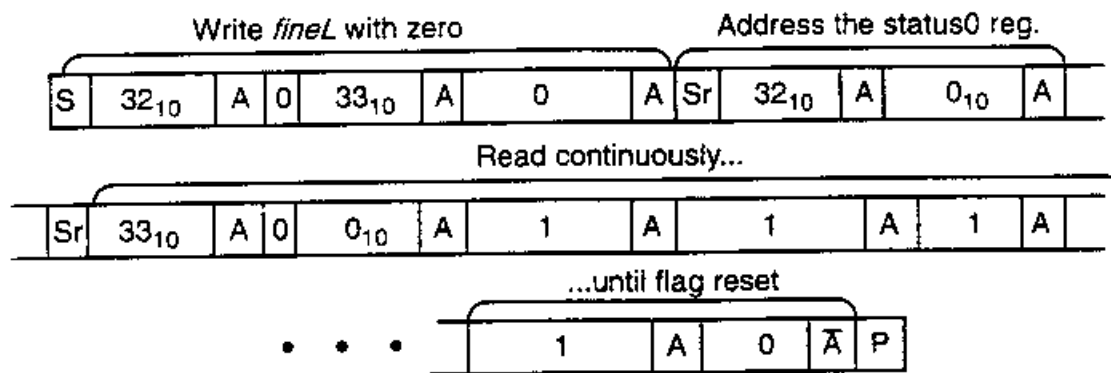
Write *fineL* with zero							Address the status0 reg.					
S	32_{10}	A	0	33_{10}	A	0	A	Sr	32_{10}	A	0_{10}	A

Read continuously...											
Sr	33_{10}	A	0	0_{10}	A	1	A	1	A	1	A

...until flag reset				
• • •	1	A	0	$\overline{A}$	P

Figure 20 : Same location multiple data read.

5.6.6 Multiple location write

If the automatic increment bit is set,(msb of the index byte), then it is possible to write data bytes to consecutive adjacent internal registers without having to send explicit indexes prior to sending each data byte. An autoincrement write to the black calibration DAC registers with their default values is shown in the following example.
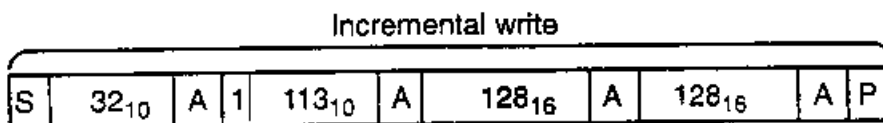
Incremental write									
S	32_{10}	A	1	113_{10}	A	128_{16}	A	128_{16}	A	P

Figure 21 : Multiple location write.

5.6.7 Multiple location read

In the same manner, multiple locations can be read with a single read message. In this example the index is written first, to ensure the exposure related registers are addressed and then all six are read
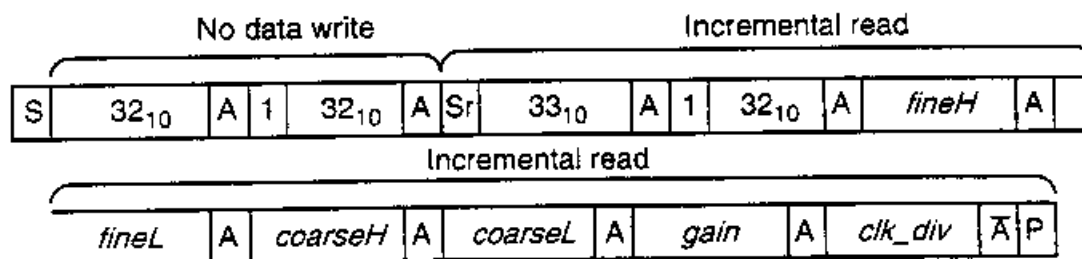
No data write						Incremental read							
S	32_{10}	A	1	32_{10}	A	Sr	33_{10}	A	1	32_{10}	A	*fineH*	A

Incremental read									
fineL	A	*coarseH*	A	*coarseL*	A	*gain*	A	*clk_div*	$\overline{A}$	P

Figure 22 : Multiple location read.

Note that a stop condition is not required after the negative acknowledge from the master.

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5.7   Serial Interface Timing

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	fscl	0	100	kHz
Bus free time between a *stop* and a *start*	tbuf	***	-	us
Hold time for a repeated *start*	thd;sta	***	-	us
LOW period of SCL	tlow	***	-	us
HIGH period of SCL	thigh	***	-	us
Set-up time for a repeated *start*	tsu;sta	***	-	us
Data hold time	thd;dat	***	-	us
Data Set-up time	tsu;dat	***	-	ns
Rise time of SCL, SDA	tr	-	***	ns
Fall time of SCL, SDA	tf	-	***	ns
Set-up time for a *stop*	tsu;sto	***	-	us
Capacitive load of each bus line (SCL, SDA)	Cb	-	***	pF

Table 21 : Serial Interface Timing Characteristics
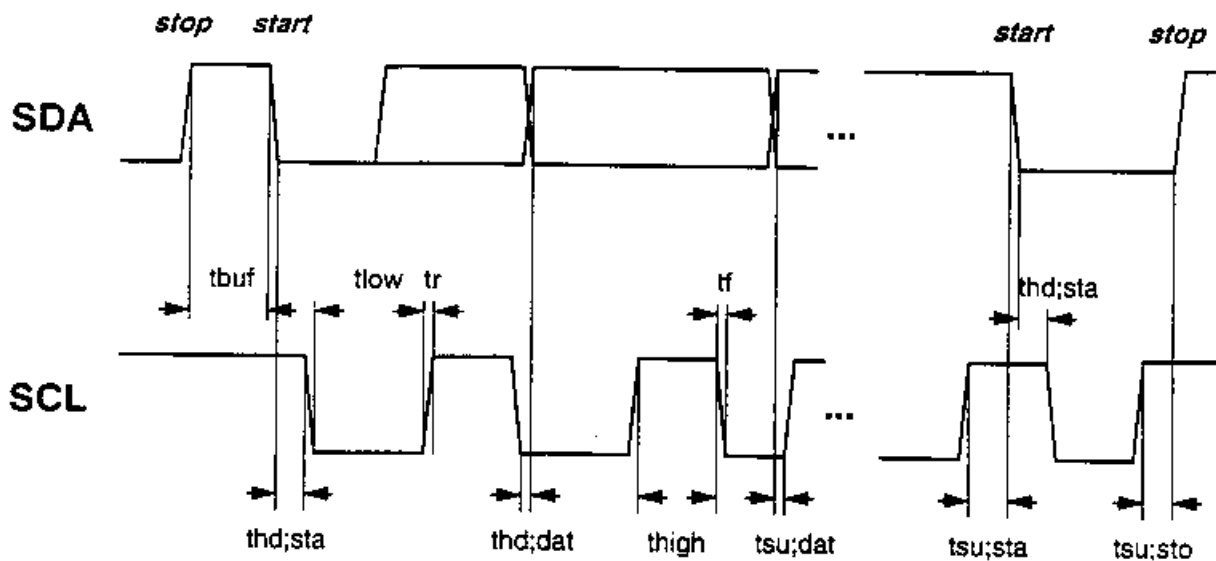
all values referred to the minimum input level (high) = 3.5V, and maximum input level (low) = 1.5V

Figure 23 : Serial Interface Timing Characteristics

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6. Clock Signal

VV5404 generates a system clock when a quartz crystal or ceramic resonator circuit is connected to the CLKI and CLKO pins. The device can also be driven directly from an external clock source driving CLK.

If CLKI is generated for the video sensor by the receiving device it must be active during serial interface coummunications for at least 16 clock cycles before the serial comummications start bit and for at least 16 cycles after the serial comummunications stop bit.

The synchronisation input, SIN, synchronises the clock divider logic in addition to the main clock generation and the video timing control block.

R1 = 1 MΩ   C1 = C2 = 47 pF
R2 = 510 Ω   X1 = 14.31818 MHz
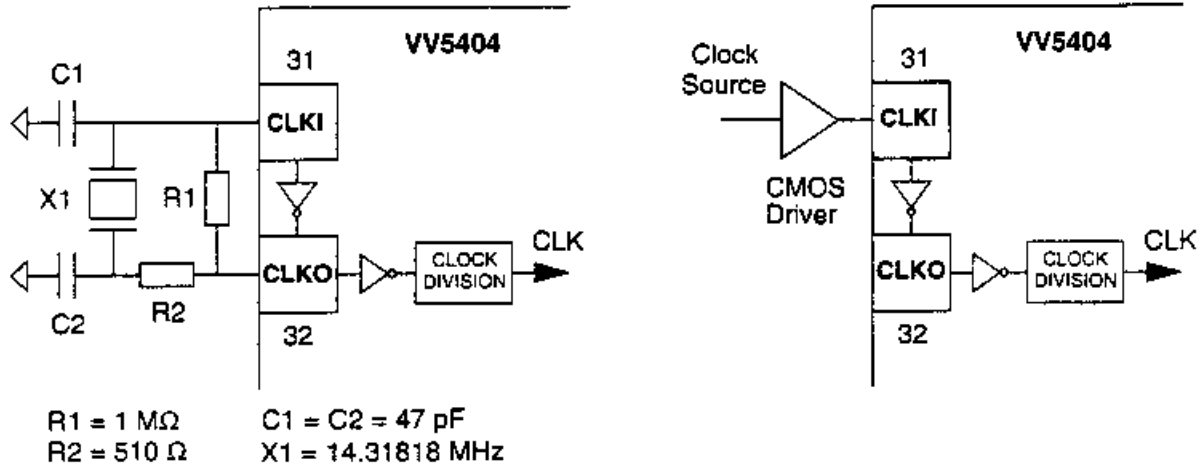
Figure 24 : Camera Clock Sources

For greater flexibility the input frequency can be divided by 2, 4, 8 or 16 to select the pixel clock frequency. The clock divisor serial register selects the input clock frequency divisor.

The clock signal must be a square wave with a 50% (+/- 10%) mark:space ratio. Table 22 specifies the maximum and minimum pixel clock frequencies for the module. Table 23 and Table 23 specify the relationship between the input clock, CLKI, and the pixel clock frequency for the different settings of the sensor's internal clock divider.

	MHz
Minimum Pixel Rate	0.44744
Maximum Pixel Rate	3.57954

Table 22 : Maximum and Minimum Pixel Rates

This translates into a maximum input clock frequency of 7.15909 MHz if a clock divisor of 2 is used (the default - Table 23). Thus if a 14.31818 MHz crystal is used, only the 4, 8 and 16 clock divisors should be used (Table 23).

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CLKI (MHz)	Clock Div Reg		Divisor	Pixel Frequency (MHz)	Frame rate (fps)		Comments
	bit 1	bit 0			30 fps	25 fps	
7.15909	0	0	2	3.57954	30.0	25.0	Default
7.15909	0	1	4	1.78977	15.0	12.5	
7.15909	1	0	8	0.89489	7.50	6.25	
7.15909	1	1	16	0.44744	3.75	3.125	

Table 23 : Clock Divisors for an externally generated clock signal.

CLKI (MHz)	Clock Div Reg		Divisor	Pixel Frequency (MHz)	Frame rate (fps)		Comments
	bit 1	bit 0			30 fps	25 fps	
14.31818	0	0	2	7.15909			Not Valid
14.31818	0	1	4	3.57954	30.0	25.0	
14.31818	1	0	8	1.78977	15.0	12.5	
14.31818	1	1	16	0.89489	7.50	6.25	

Table 24 : Clock Divisors for a 14.31818 MHz Crystal.

7. General

7.1 Signal Levels

The signalling sense of the voltage appearing across the digital signal conductors follows standard CMOS levels as follows:
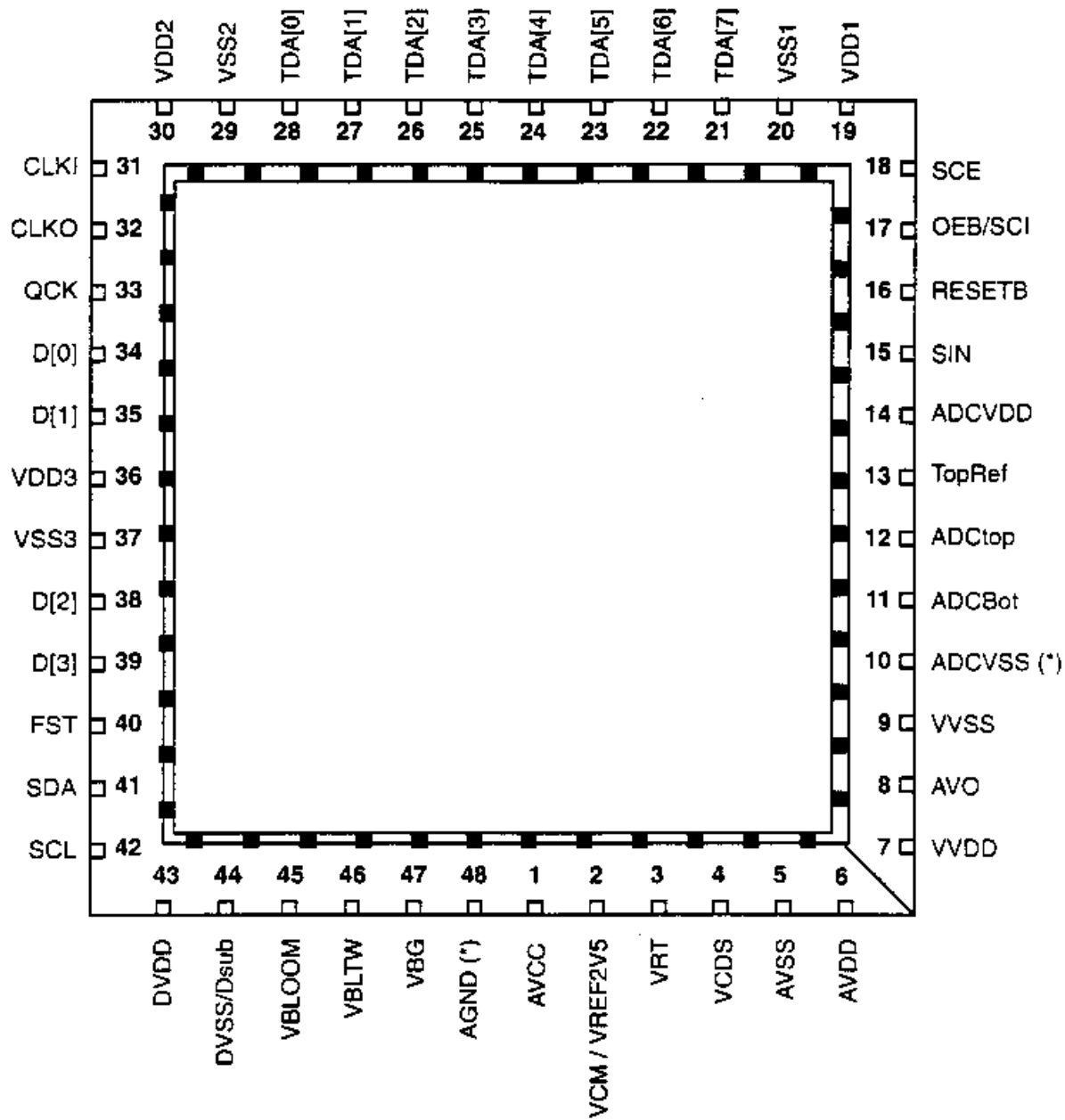
A signal line shall be at most 0.2 x Vdd for a binary 0.

A signal line shall be at least 0.8 x Vdd for a binary 1.

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8. Pinout

8.1 Bonding Diagram

48 pin LCC

(*) - Paddle Connections

Die Size = (7.4530 + 0.220 mm) x (6.2142 + 0.270 mm)

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8.2 Signal Names

| Pin	Name	Type	Description
			POWER SUPPLIES
1	AVCC	PWR	Core analogue power and reference supplies.
48	AGND	GND	Core analogue ground and reference supplies.
43	DVDD	PWR	Core digital power.
44	DVSS/Dsub	GND	Core digital ground.
6	AVDD	PWR	Output stage power.
5	AVSS	GND	Output stage ground.
7	VVDD	PWR	Analogue output buffer power.
9	VVSS	GND	Analogue output buffer ground.
14	ADCVDD	PWR	ADC power.
10	ADCVSS	GND	ADC ground.
19	VDD1	PWR	Digital padring & logic power.
30	VDD2	PWR	Digital padring & logic power.
36	VDD3	PWR	Digital padring & logic power.
20	VSS1	GND	Digital padring & logic ground.
29	VSS2	GND	Digital padring & logic ground.
37	VSS3	GND	Digital padring & logic ground.
			ANALOGUE SIGNALS
45	VBLOOM	OA	Anti-blooming pixel reset voltage
46	VBLTW	OA	Bitline test white level reference
47	VBG	OA	Internally generated bandgap reference voltage 1.22V
2	VCM/ VREF2V5	OA	Common-mode input for OSA and Internally generated 2.5 V reference voltage.
3	VRT	IA	Pixel reset voltage
4	VCDSH	IA	
8	AVO	OA	Analogue output
11	ADCbot	IA	Bottom voltage reference for ADC
12	ADCtop	IA	Top voltage reference for ADC
13	TopRef	OA	Internally generally top voltage reference for ADC

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Pin	Name	Type	Description
DIGITAL CONTROL SIGNALS			
18	SCE	ID↓	Scan Test Enable
15	SIN	ID↓	Frame timing reset (soft reset).
16	RESETB	ID↑	System Reset. Active Low.
SERIAL INTERFACE			
42	SCL	ID↑	Serial bus clock (input only).
41	SDA	BI↑	Serial bus data (bidirectional, open drain).
DIGITAL VIDEO INTERFACE			
39 38 35 34	D[3] D[2] D[1] D[0]]	ODT	Tristateable 4-wire output data bus. D[3] is the most significant bit.
33	QCK	ODT	Tristateable data qualification clock.
40	FST	ODT	Tristateable Frame start signal.
17	OEB/SCI	ID↓	Digital output (tristate) enable. (Also serves as scan test input when SCE is high)
SYSTEM CLOCKS			
31	CLKI	ID	Oscillator input.
32	CLKO	OD	Oscillator output.

Key			
A	Analogue Input	D	Digital Input
OA	Analogue Output	ID↑	Digital input with internal pull-up
BI	Bidirectional	ID↓	Digital input with internal pull-down
BI↑	Bidirectional with internal pull-up	OD	Digital Output
BI↓	Bidirectional with internal pull-down	ODT	Tristateable Digital Output

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9. VV5404 Module Schematic Diagram

9.1 Internal ADC
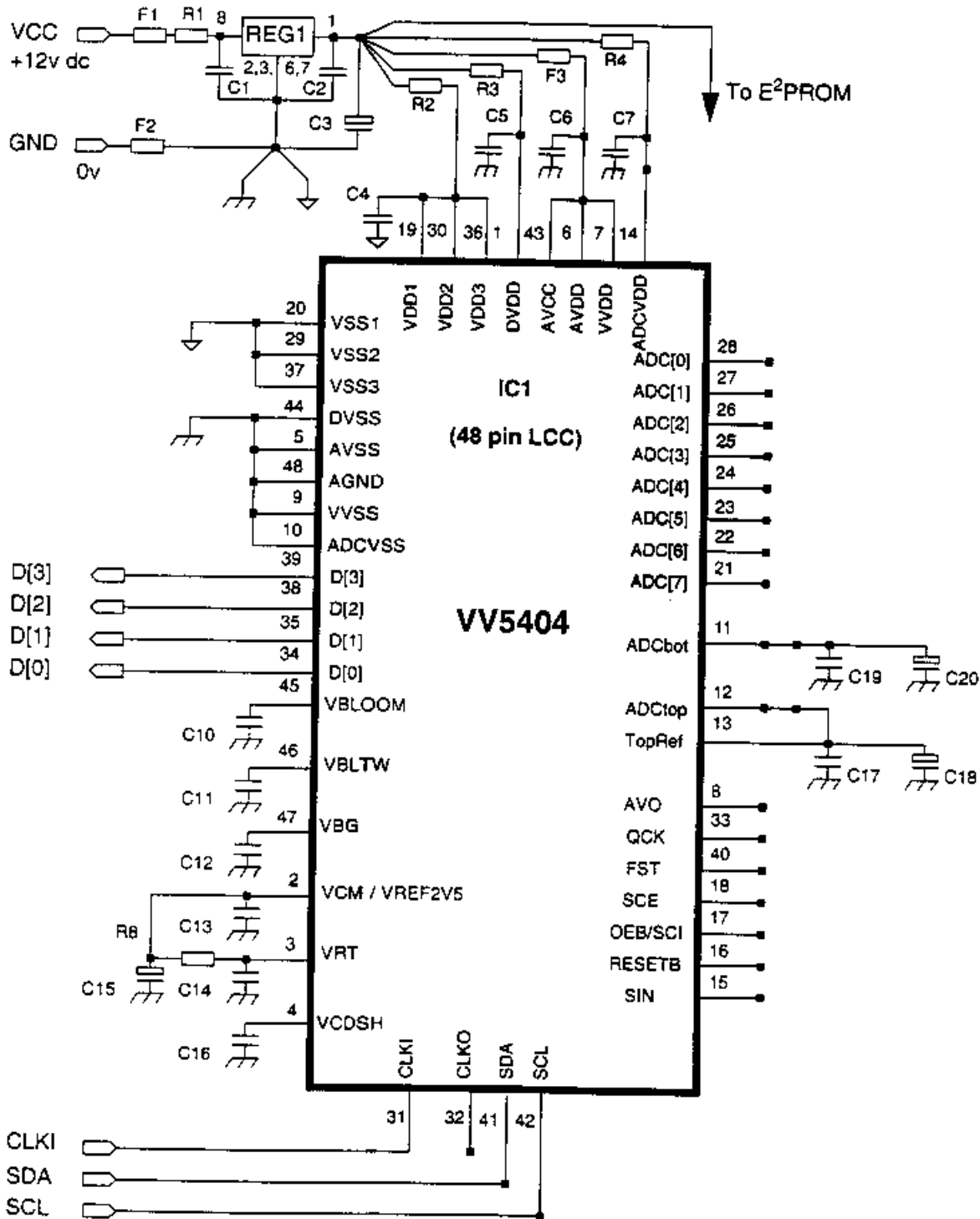
9.2 Module Component List

Component	Part No. / Provisional Value	Rating / Notes
IC1	VVL-404A	VVL camera chip (48 pin LCC)
IC2	AT24C01A	SOIC Surface Mount (8 pin)
IC3	LM1175/AD775	SOIC Surface Mount (24 pin)
REG1	TBD	-
C1,C2	0.2 μF	
C3	10.0 μF	6V tant.
C4 - C13, C16 · C17, C19	0.1 μF	
C14	0 (0.1 μF)*	Populate only if R8* shorted.
C15	4.7 μF	6V tant
C18	10.0 μF	6V tant
C20	4.7 μF	6V tant
C21, C22	1.0 nF	Prevents data breakthrough on the Serial Interface. Vary to acheive optimum speed/noise tradeoff.
R1	TDB	
R2 - R5	10 Ω	
R6, R7	4.7 kΩ	
R8 *	33 (0)*	
F1		
F2		
F3		
Connector	TBD by Supplier	

Table 25 : PCB Component List

Notes:
1. Use surface mount components throughout.
2. All ceramic capacitors are type COG.
3. Keep nodes Supply and Ground pins low impedance and independent.
4. Keep circuit components close to chip pins (especially de-coupling capacitors).
5. Experiment with supply ferrites and resistors to achieve best Noise Rejection
6. EMC precautions will be required on D[3:0] if driving a long cable.

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Ordering Information

Part Number	Package	Blemish Specification
VV5404	48 LCC (APEC)	Standard

48 Pin LCC (APEC) Package Outline

The optical array is centred within the package to a tolerance of +/- 0.2 mm

Tolerances on package dimensions +/-12%

All dimensions in millimetres

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