

Quad 2-input AND gate

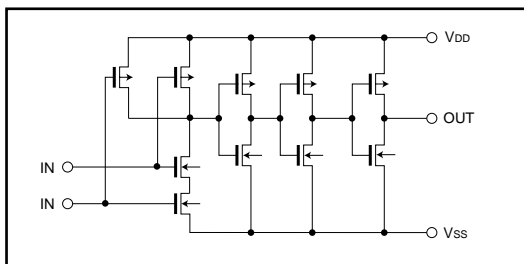
BU4081B / BU4081BF / BU4081BFV

The BU4081B, BU4081BF, and BU4081BFV are dual-input positive-logic AND gates with four circuits mounted on a single chip. An inverter-type buffer is added to the gate output, improving input / output transmission speed, and an increased load capacitance suppresses fluctuation in transmission time to a minimum.

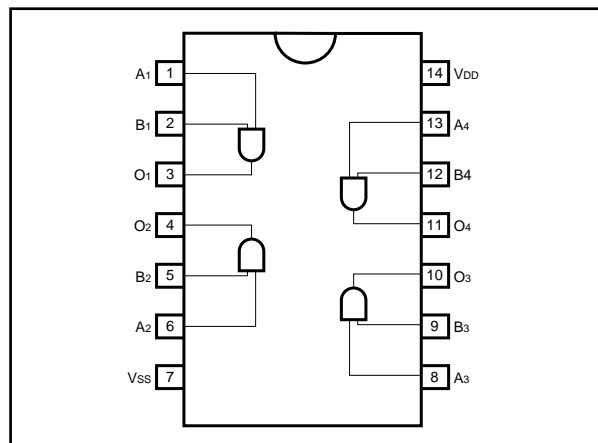
●Features

- 1) Low power dissipation.
- 2) Wide range of operating power supply voltages.
- 3) High input impedance.
- 4) High fan-out.
- 5) Direct drive of 2 L-TTL inputs and 1 LS-TTL input.

●Logic circuit diagram



●Block diagram



●Absolute maximum ratings ($T_a = 25^\circ\text{C}, V_{SS} = 0\text{V}$)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	$-0.3 \sim +18$	V
Power dissipation	P_d	1000 (DIP), 450 (SOP), 350 (SSOP)	mW
Operating temperature	T_{opr}	$-40 \sim +85$	$^\circ\text{C}$
Storage temperature	T_{stg}	$-55 \sim +150$	$^\circ\text{C}$
Input voltage	V_{IN}	$-0.3 \sim V_{DD} + 0.3$	V
I / O pin current	$I_{I/O}$	± 10	mA

●Electrical characteristics (unless otherwise noted, $V_{SS} = 0\text{V}, T_a = 25^\circ\text{C}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V_{DD} (V)	Conditions	Measurement circuit
Input high level voltage	V_{IH}	3.5	—	—	V	5	—	Fig.1
		7.0	—	—		10		
		11.0	—	—		15		
Input low level voltage	V_{IL}	—	—	1.5	V	5	—	Fig.1
		—	—	3.0		10		
		—	—	4.0		15		
Input high level current	I_{IH}	—	—	0.3	μA	15	$V_{IH} = 15\text{V}$	Fig.1
Input low level current	I_{IL}	—	—	-0.3	μA	15	$V_{IL} = 0\text{V}$	Fig.1
Output high level voltage	V_{OH}	4.95	—	—	V	5	$I_o = 0\text{mA}$	Fig.1
		9.95	—	—		10		
		14.95	—	—		15		
Output low level voltage	V_{OL}	—	—	0.05	V	5	$I_o = 0\text{mA}$	Fig.1
		—	—	0.05		10		
		—	—	0.05		15		
Output high level current	I_{OH}	-0.16	—	—	mA	5	$V_{OH} = 4.6\text{V}$	Fig.1
		-0.4	—	—		10	$V_{OH} = 9.5\text{V}$	
		-1.2	—	—		15	$V_{OH} = 13.5\text{V}$	
Output low level current	I_{OL}	0.44	—	—	mA	5	$V_{OL} = 0.4\text{V}$	Fig.1
		1.1	—	—		10	$V_{OL} = 0.5\text{V}$	
		3.0	—	—		15	$V_{OL} = 1.5\text{V}$	
Static current dissipation	I_{DD}	—	—	1	μA	5	$V_i = V_{DD}$ or GND	—
		—	—	2		10		
		—	—	4		15		

Switching characteristics (unless otherwise noted, $V_{SS} = 0V$, $T_a = 25^\circ C$, $C_L = 50pF$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V _{DD} (V)	Conditions	Measurement circuit
						5		
Output rise time	t _{RLH}	—	180	—	ns	5	—	Fig.2
		—	90	—		10		
		—	65	—		15		
Output fall time	t _{rHL}	—	100	—	ns	5	—	Fig.2
		—	50	—		10		
		—	40	—		15		
“L” to “H” Propagation delay time	t _{PLH}	—	160	—	ns	5	—	Fig.2
		—	65	—		10		
		—	50	—		15		
“H” to “L” Propagation delay time	t _{PHL}	—	160	—	ns	5	—	Fig.2
		—	65	—		10		
		—	50	—		15		
Input capacitance	C _{IN}	—	5	—	pF	—	—	—

● Measurement circuits

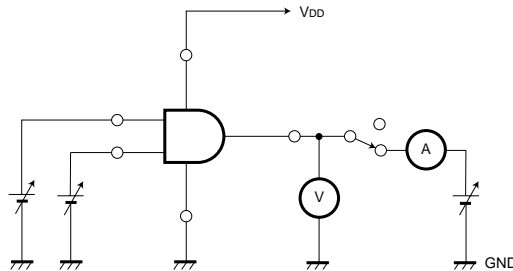


Fig. 1 DC characteristics

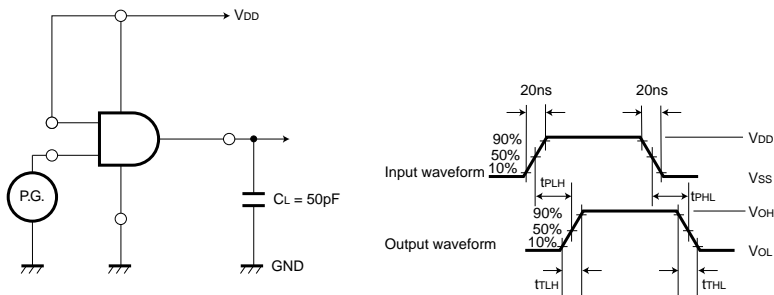


Fig. 2 Switching characteristics

●Electrical characteristic curve

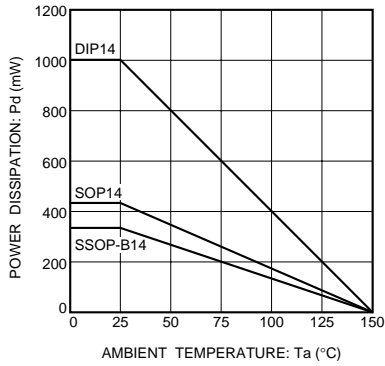


Fig. 3 Power dissipation vs. Ta

●External dimensions (Units: mm)

