

April 1995

Features

- 20A, 400V and 500V
- $V_{CE(ON)}$ 2.5V Max.
- T_{FALL} 1 μ s, 0.5 μ s
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance
- Anti-Parallel Diode

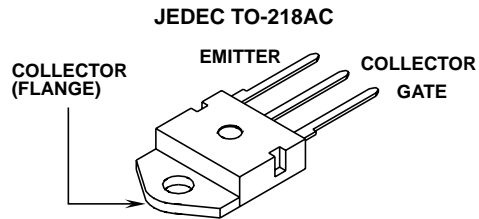
Applications

- Power Supplies
- Motor Drives
- Protective Circuits

Description

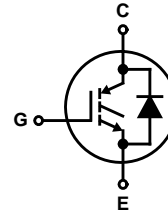
The HGTH20N40C1D, HGTH20N40E1D, HGTH20N50C1D, and HGTH20N50E1D are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high voltage, low on-dissipation applications such as switching regulators and motor drivers. They feature a discrete anti-parallel diode that shunts current around the IGBT in the reverse direction without introducing carriers into the depletion region. These types can be operated directly from low power integrated circuits.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTH20N40C1D	TO-218AC	G20N40C1D
HGTH20N40E1D	TO-218AC	G20N40E1D
HGTH20N50C1D	TO-218AC	G20N50C1D
HGTH20N50E1D	TO-218AC	G20N50E1D

NOTE: When ordering, use the entire part number.

Absolute Maximum Ratings $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

	HGTH20N40C1D HGTH20N40E1D	HGTH20N50C1D HGTH20N50E1D	UNITS
Collector-Emitter Voltage	400	500	V
Collector-Gate Voltage $R_{GE} = 1M\Omega$	400	500	V
Gate-Emitter Voltage	± 20	± 20	V
Collector Current Continuous	20	20	A
Collector Current Pulsed	35	35	A
Diode Forward Current Continuous at $T_C = +25^\circ\text{C}$	35	35	A
at $T_J = +90^\circ\text{C}$	20	20	A
Power Dissipation Total at $T_C = +25^\circ\text{C}$	100	100	W
Power Dissipation Derating $T_C > +25^\circ\text{C}$	0.8	0.8	W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	-55 to +150	-55 to +150	$^\circ\text{C}$

INTERSIL CORPORATION IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

Specifications HGTH20N40C1D, HGTH20N40E1D, HGTH20N50C1D, HGTH20N50E1D

Electrical Specifications $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS	
			HGTH20N40C1D, HGTH20N40E1D		HGTH20N50C1D, HGTH20N50E1D			
			MIN	MAX	MIN	MAX		
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 1\text{mA}, V_{GE} = 0$	400	-	500	-	V	
Gate Threshold Voltage	$V_{GE(TH)}$	$V_{GE} = V_{CE}, I_C = 1\text{mA}$	2.0	4.5	2.0	4.5	V	
Zero Gate Voltage Collector Current	I_{CES}	$V_{CE} = 400\text{V}, T_C = +25^\circ\text{C}$	-	250	-	-	μA	
		$V_{CE} = 500\text{V}, T_C = +25^\circ\text{C}$	-	-	-	250	μA	
		$V_{CE} = 400\text{V}, T_C = +125^\circ\text{C}$	-	1000	-	-	μA	
		$V_{CE} = 500\text{V}, T_C = +125^\circ\text{C}$	-	-	-	1000	μA	
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20\text{V}, V_{CE} = 0$	-	100	-	100	nA	
Collector-Emitter On Voltage	$V_{CE(ON)}$	$I_C = 20\text{A}, V_{GE} = 10\text{V}$	-	2.5	-	2.5	V	
		$I_C = 35\text{A}, V_{GE} = 20\text{V}$	-	3.2	-	3.2	V	
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = 10\text{A}, V_{CE} = 10\text{V}$	-	6 (Typ)	-	6 (Typ)	V	
On-State Gate Charge	$Q_{G(ON)}$	$I_C = 10\text{A}, V_{CE} = 10\text{V}$	-	33 (Typ)	-	33 (Typ)	nC	
Turn-On Delay Time	$t_{D(ON)I}$	$I_C = 20\text{A}, V_{CE(CLIP)} = 300\text{V},$ $L = 25\mu\text{H}, T_J = +100^\circ\text{C},$ $V_{GE} = 10\text{V}, R_G = 25\Omega$	-	50	-	50	ns	
Rise Time	t_{RI}		-	50	-	50	ns	
Turn-Off Delay Time	$t_{D(OFF)I}$		-	400	-	400	ns	
Fall Time	t_{FI}		40E1D, 50E1D	680 (Typ)	1000	680 (Typ)	1000	ns
			40C1D, 50C1D	400 (Typ)	500	400 (Typ)	500	ns
Turn-Off Energy Loss per Cycle (Off Switching Dissipation = $W_{OFF} \times$ Frequency)	W_{OFF}	40E1D, 50E1D	1810 (Typ)				μJ	
		40C1D, 50C1D	1070 (Typ)				μJ	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	1.25	-	1.25	$^\circ\text{C/W}$	
Diode Forward Voltage	V_{EC}	$I_{EC} = 20\text{A}$	-	2	-	2	V	
Diode Reverse Recovery Time	t_{RR}	$I_{EC} = 20\text{A}, dI_{EC}/dt = 100\text{A}/\mu\text{s}$	-	100	-	100	ns	

Typical Performance Curves

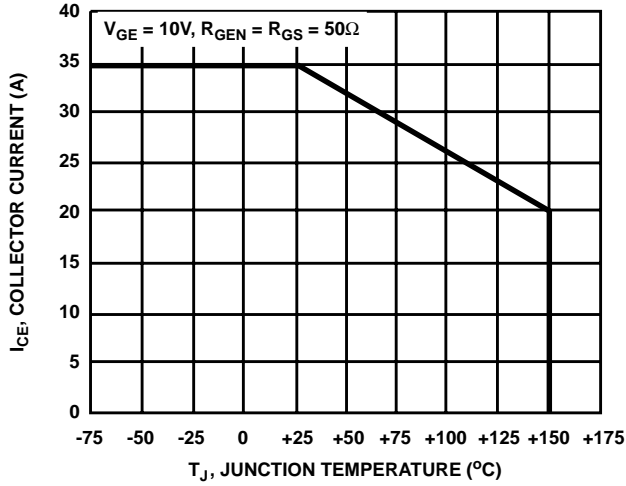


FIGURE 1. MAX. SWITCHING CURRENT LEVEL. $R_G = 50\Omega$, $V_{GE} = 0V$ ARE THE MIN. ALLOWABLE VALUES

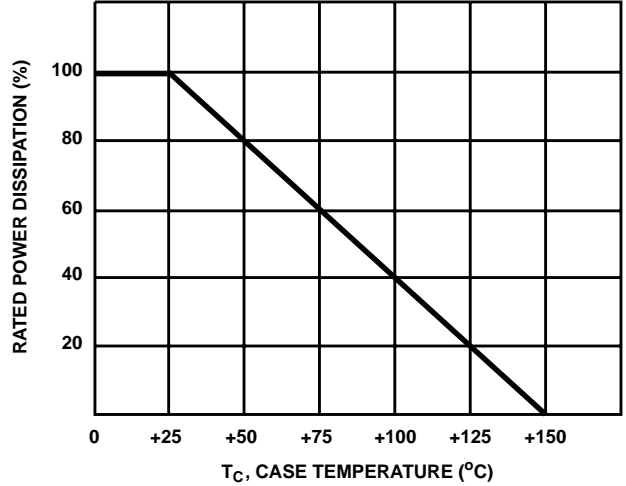


FIGURE 2. POWER DISSIPATION vs TEMPERATURE DERATING CURVE

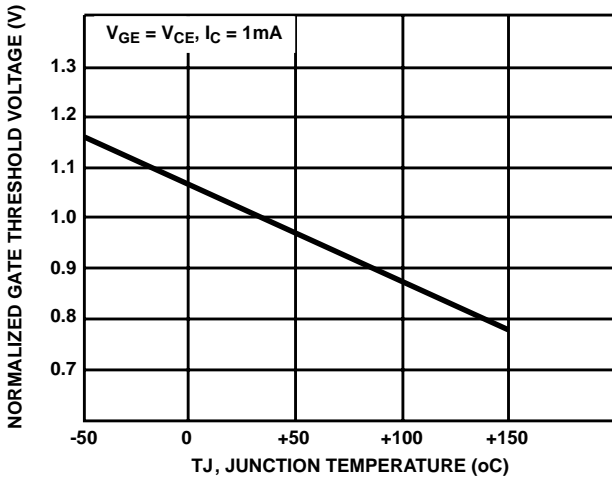


FIGURE 3. TYPICAL NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

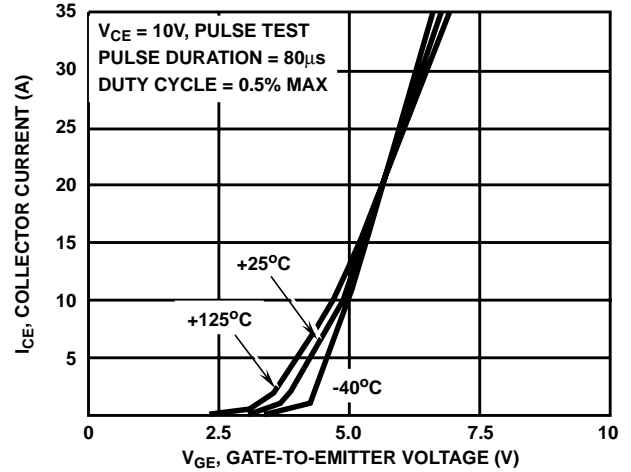


FIGURE 4. TYPICAL TRANSFER CHARACTERISTICS

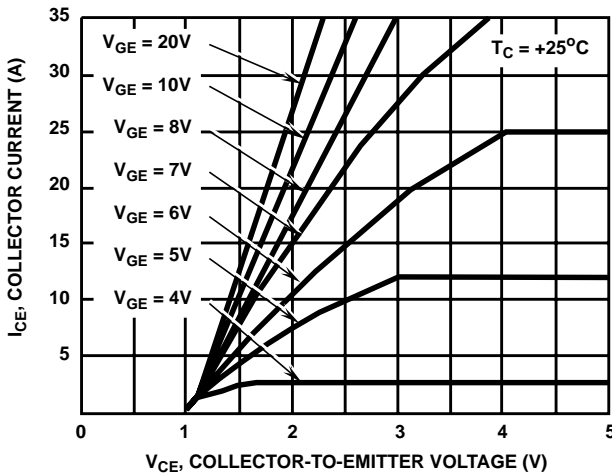


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

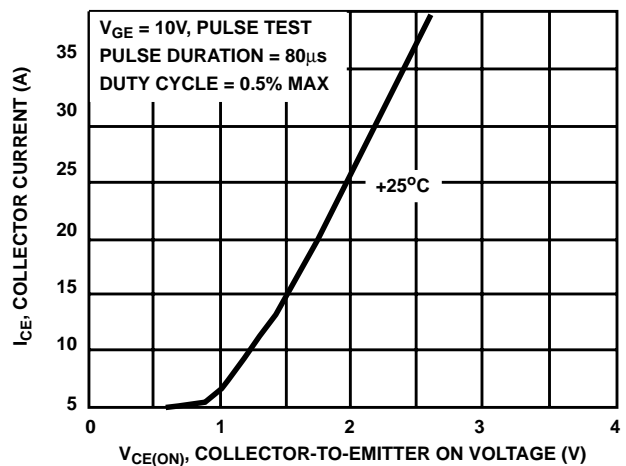


FIGURE 6. TYPICAL COLLECTOR-TO-EMITTER ON-VOLTAGE vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

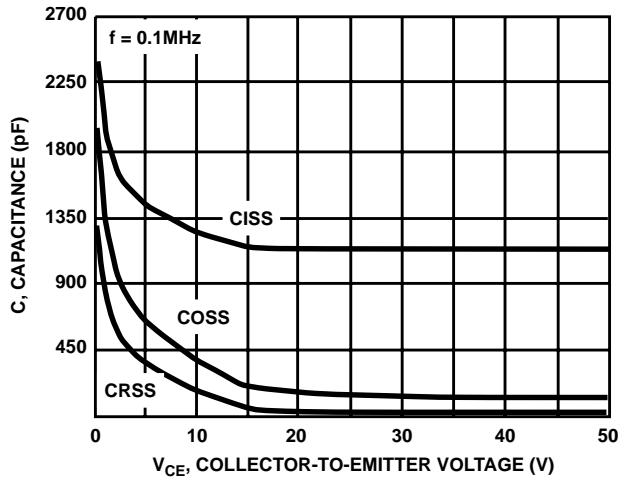


FIGURE 7. CAPACITANCE vs COLLECTOR-TO-EMITTER VOLTAGE

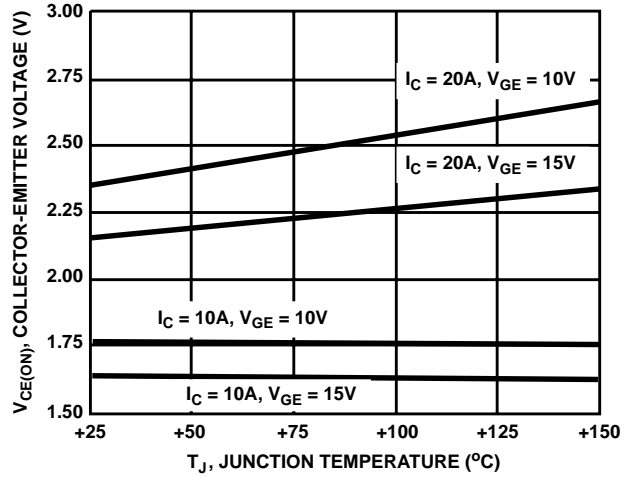


FIGURE 8. TYPICAL $V_{CE(ON)}$ vs TEMPERATURE

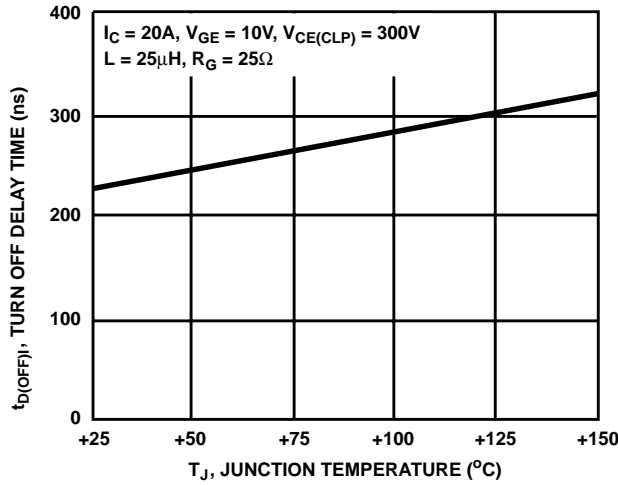


FIGURE 9. TYPICAL TURN-OFF DELAY TIME

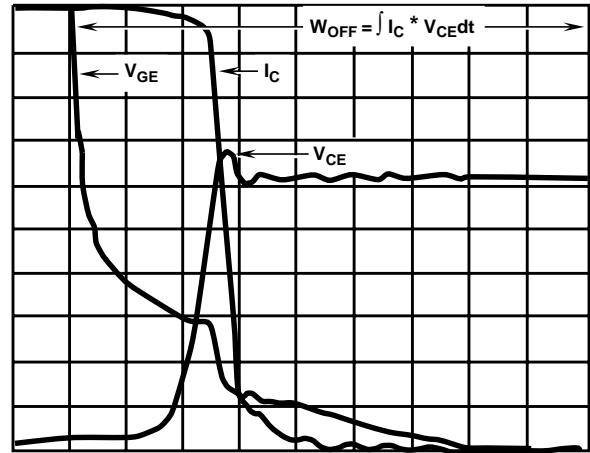


FIGURE 10. TYPICAL INDUCTIVE SWITCHING WAVEFORMS

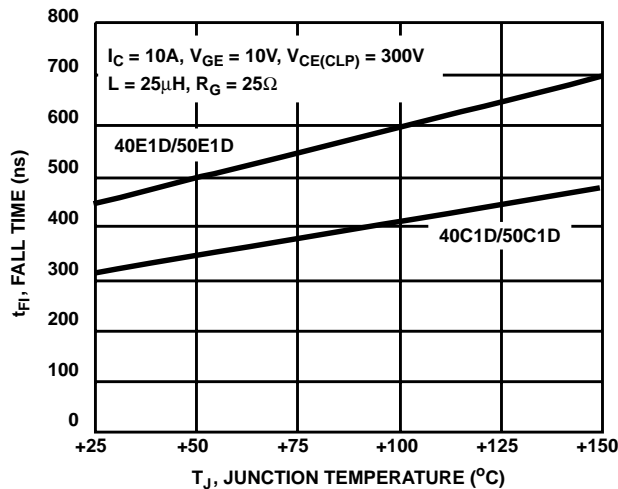


FIGURE 11. TYPICAL FALL TIME ($I_C = 10A$)

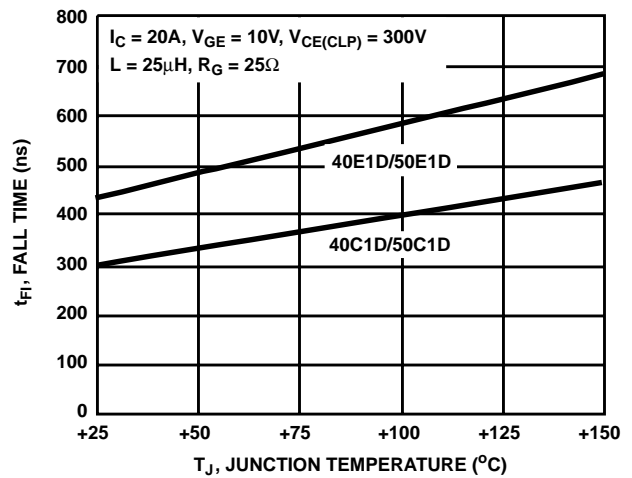


FIGURE 12. TYPICAL FALL TIME ($I_C = 20A$)

Typical Performance Curves (Continued)

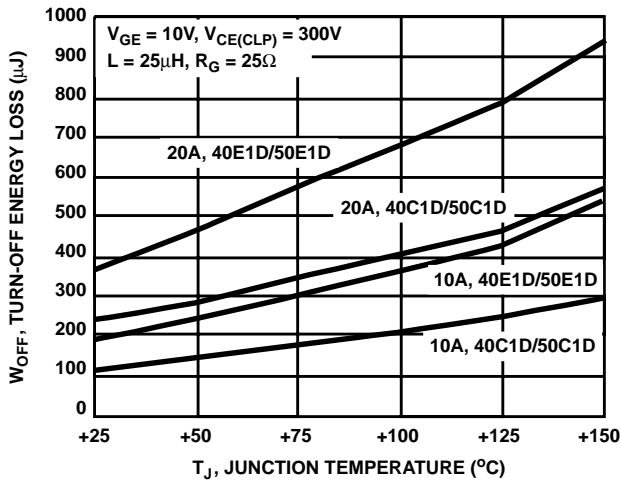
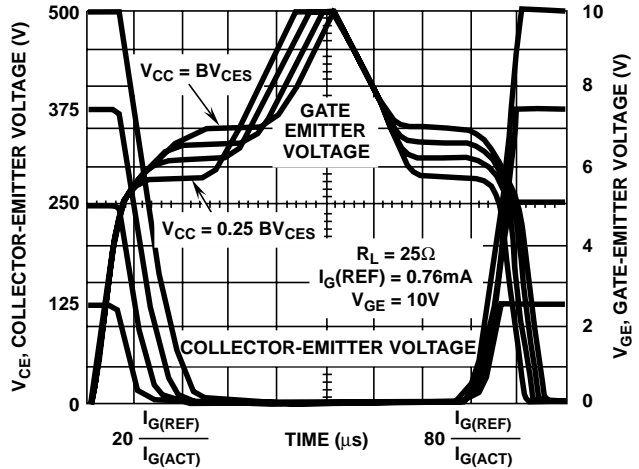


FIGURE 13. TYPICAL CLAMPED INDUCTIVE TURN-OFF SWITCHING LOSS/CYCLE



NOTE: For Turn-Off gate currents in excess of 3mA, V_{CE} Turn-Off is not accurately represented by this normalization.

FIGURE 14. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT (REFER TO APPLICATION NOTES AN7254 AND AN7260)

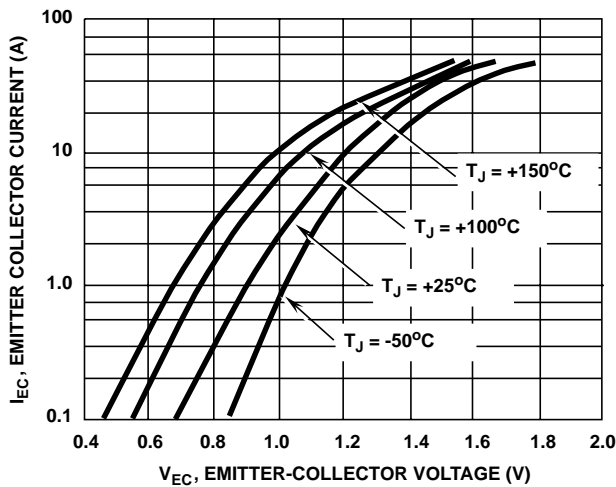


FIGURE 15. TYPICAL DIODE EMITTER-COLLECTOR VOLTAGE vs CURRENT

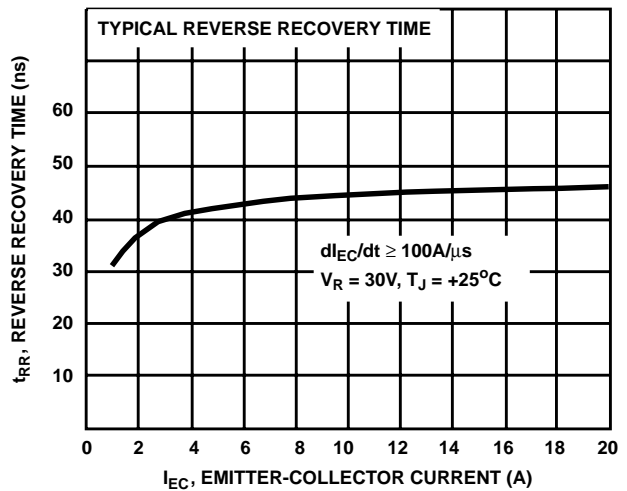


FIGURE 16. TYPICAL DIODE REVERSE RECOVERY TIME

Test Circuit

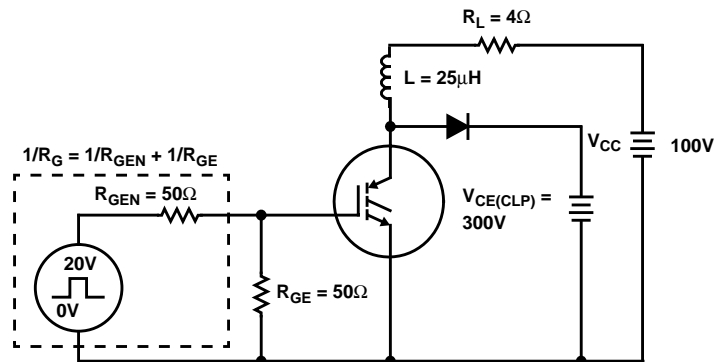


FIGURE 17. INDUCTIVE SWITCHING TEST CIRCUIT

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