

FEATURES

- Optimized for Off-Line Operation
- Maximum Duty Ratio 44% (typ.)
- Maximum Clock Frequency Above 1 MHz
- Frequency Reduction for Improved Overcurrent Protection
- Low Standby Current for Current-Fed Start-Up
- Current-Mode or Voltage-Mode Control
- Internal User-Adjustable Slope Compensation
- Functionally Integrated & Simplified 5-pin Design

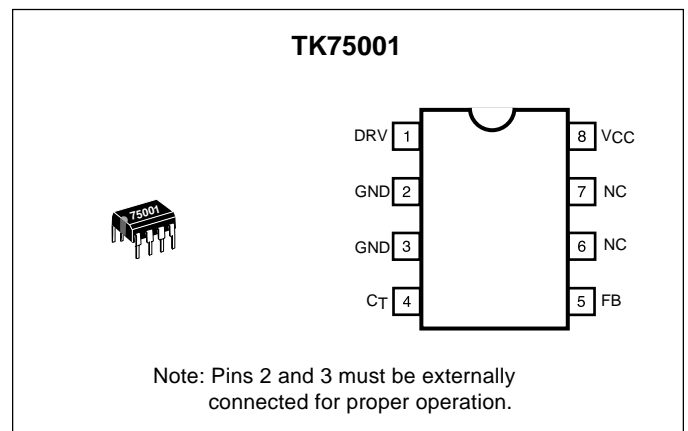
DESCRIPTION

The TK75001 is a simplified primary side controller optimized for off-line switching power supplies. It is suitable for both voltage-mode and current-mode control and has advanced features not available in controllers with a higher pin count. The key to full functionality in a 5-pin design is that the current signal and the error signal are added together and fed into the feedback pin. A sawtooth current flowing out of the feedback pin provides a slope compensation ramp (in current-mode applications) or a PWM ramp (in voltage-mode applications), in proportion to the resistance terminating that pin. If the sum of the current sense signal, error signal and ramp signal exceeds the Overcurrent Detector threshold indicating that the Current Control Detector has lost control of the switch current, the charging current of the timing capacitor will be reduced to about 25% for the remainder of the clock period. The reduced charging current causes no more than a one-third reduction in switching frequency, effectively preventing short-circuit current runaway.

The TK75001 is available in an 8-pin DIP package.

APPLICATIONS

- Off-Line Power Supplies
- Industrial Power Supplies
- Telecom Power Supplies
- Off-Line Battery Chargers



ORDERING INFORMATION

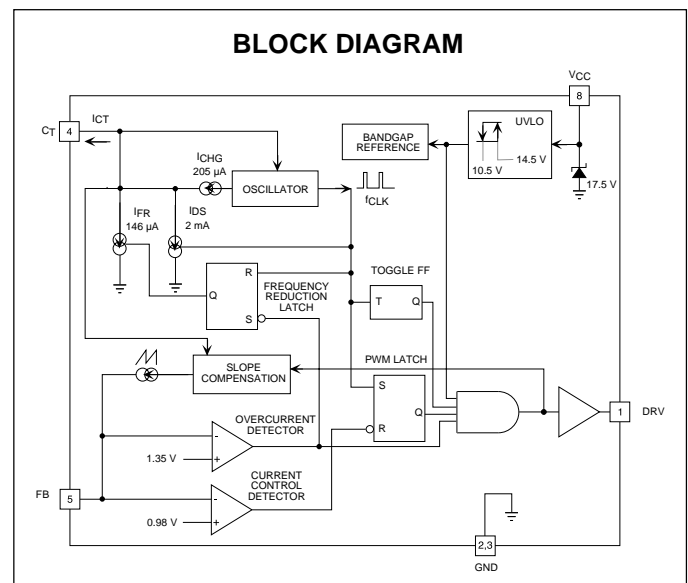
TK75001D □□□

└─ Tape/Reel Code

└─ Temperature Code

TEMP. CODE (OPTIONAL)
I: -40 to +85 °C

TAPE/REEL CODE
MG: Magazine



TK75001

ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---------------|---|----------------|
| Supply Voltage (Low Impedance Source) | 16 V | Junction Temperature | 150 °C |
| Supply Voltage ($I_{CC} < 30$ mA) | Self Limiting | Storage Temperature Range | -55 to +150 °C |
| Power Dissipation (Note 1) | 825 mW | Operating Temperature Range | -20 to +80 °C |
| Output Energy (Capacitive Load) | 5 μ J | Extended Temperature Range | -40 to +85 °C |
| C_T and FB Pins | 16 V | Lead Soldering Temperature (10 s) | 235 °C |

TK75001 ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{CC} = 13$ V, $C_{CC} = 4.7$ μ F, $C_T = 800$ pF, $C_{DRV} = 1000$ pF, $T_A = T_j =$ Full Operating Temperature Range.
 Typical numbers apply at $T_A = 25$ °C, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--|---|-------|-------|-------|---------|
| $I_{CC(START)}$ | Start-up Supply Current | Current Source to V_{CC} Pin | | 0.5 | 1.0 | mA |
| $I_{CC(ON)}$ | Operating Supply Current | | | 14.5 | 19.0 | mA |
| $V_{CC(ON)}$ | UVLO Voltage ON | V_{CC} Sweeps Upward, (Note 3) | 12.5 | 14.5 | 16.0 | V |
| $V_{CC(OFF)}$ | UVLO Voltage OFF | V_{CC} Sweeps Downward | 9.0 | 10.5 | 12.0 | V |
| V_{HYST} | UVLO Hysteresis | | 2.8 | 4.0 | | V |
| $V_{CC(CLAMP)}$ | Internal Clamp Voltage | $I_{CC} = 25$ mA, (Note 3) | 16.0 | 17.5 | 19.0 | V |
| OSCILLATOR SECTION (C_T PIN) | | | | | | |
| f_{DRV} | Frequency at DRV Pin | $T_A = T_j = 25$ °C | 44 | 50 | 56 | kHz |
| | | $T_A = T_j =$ Full Range (-20 to 80 °C) | 37 | | 63 | kHz |
| $V_{CT(PK)}$ | Peak Voltage | | 2.5 | 3.2 | 3.9 | V |
| $V_{CT(VL)}$ | Valley Voltage | | | 1.1 | | V |
| $I_{CT(DIS)}$ | Discharge Current | | 1.0 | 1.8 | 3.0 | mA |
| $C_{T(MAX)}$ | Maximum Timing Capacitance | | 4.7 | | | nF |
| CURRENT DETECTOR, FEEDBACK AND FREQUENCY REDUCTION SECTIONS (FB PIN) | | | | | | |
| V_{CCD} | Current Control Detector Reference Voltage | $T_A = T_j = 25$ °C | 0.950 | 0.980 | 1.010 | V |
| | | $T_A = T_j =$ Full Range (-20 to 80 °C) | 0.925 | | 1.035 | V |
| V_{OCD} | Overcurrent Detector Reference Voltage | $T_A = T_j = 25$ °C | 1.320 | 1.350 | 1.380 | V |
| | | $T_A = T_j =$ Full Range (-20 to 80 °C) | 1.305 | | 1.395 | V |
| $t_{FB,OC,PD}$ | Propogation Delay to DRV Pin | V_{FB} Steps from 0 to 2 V | | 60 | 130 | ns |
| $t_{FB,CC,PD}$ | Propogation Delay to DRV Pin | V_{FB} Steps from 0 to 1.20 V, (Note 4) | | 80 | 180 | ns |
| $i_{SC(PK)}$ | Slope Compensation Peak Current | $V_{CT} = V_{CT(PK)}$, $T_A = T_j = 25$ °C, (Note 2) | -245 | -200 | -155 | μ A |
| $i_{SC(VL)}$ | Slope Compensation Valley Current | $V_{CT} = V_{CT(VL)}$, $T_A = T_j = 25$ °C, (Note 2) | -65 | -40 | -15 | μ A |
| $i_{SC(PK-VL)}$ | Slope Compensation Peak to Valley | $V_{CT} = V_{CT(VL)}$, $T_A = T_j = 25$ °C, (Note 2) | -200 | -160 | -120 | μ A |

TK75001 ELECTRICAL CHARACTERISTICS (CONT.)

Test Conditions: $V_{CC} = 13\text{ V}$, $C_{CC} = 4.7\ \mu\text{F}$, $C_T = 800\ \text{pF}$, $C_{DRV} = 1000\ \text{pF}$, $T_A = T_j = \text{Full Operating Temperature Range}$.
 Typical numbers apply at $T_A = 25\ ^\circ\text{C}$, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------------------|--|------|------|------|-------|
| FREQUENCY REDUCER (OVERCURRENT PROTECTION TIMING) | | | | | | |
| $f_{DRV(FR)} / f_{DRV}$ | Frequency Reduction Ratio | $V_{FB} = 1.2\ \text{V}, 1.6\ \text{V}$ | 35 | 46 | 55 | % |
| OUTPUT SECTION (DRV PIN) | | | | | | |
| $D_{DRV(MAX)}$ | Maximim Duty Ratio | | 40 | 44 | 48 | % |
| $t_{DRV(RISE)}$ | Rise Time | 1000 pF load, $V_{CC} = 15\ \text{V}$ | | 25 | 75 | ns |
| $t_{DRV(FALL)}$ | Fall Time | 1000 pF load, $V_{CC} = 15\ \text{V}$ | | 25 | 75 | ns |
| $V_{DRV(HIGH)}$ | Output Voltage HIGH | $I_{DRV} = -40\ \text{mA}$ | 10.1 | 11.0 | | V |
| | | $I_{DRV} = -100\ \text{mA}$ | 10.0 | 10.8 | | V |
| $V_{DRV(LOW)}$ | Output Voltage LOW | $I_{DRV} = 40\ \text{mA}$ | | 0.1 | 0.25 | V |
| | | $I_{DRV} = 100\ \text{mA}$ | | 0.2 | 0.50 | V |
| | | $I_{DRV} = 5\ \text{mA}, V_{CC} = 9\ \text{V}$ | | 1.0 | 1.50 | V |

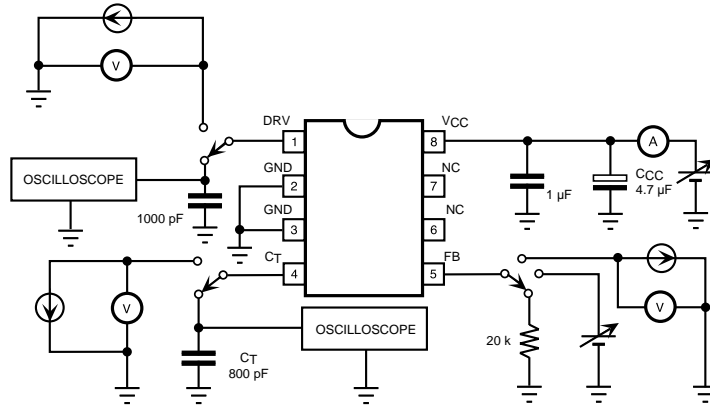
Note 1: Power dissipation is 825 mW when mounted. Derate at 6.6 mW/°C for operation above 25 °C.

Note 2: For temperature dependence refer to "Slope Compensation Peak Current vs. Temperature" graph.

Note 3: The UVLO "on" voltage is guaranteed to be below the internal clamp voltage.

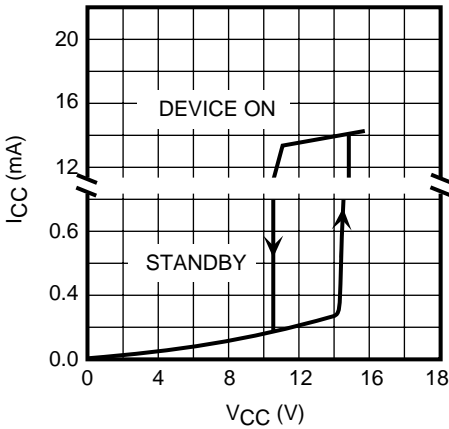
Note 4: Guaranteed by design; not 100% tested.

TEST CIRCUIT

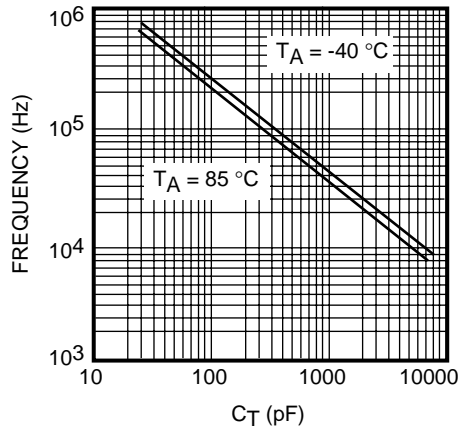


TYPICAL PERFORMANCE CHARACTERISTICS

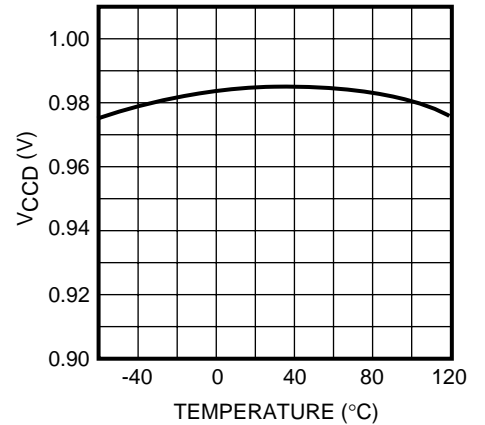
SUPPLY CURRENT vs. SUPPLY VOLTAGE



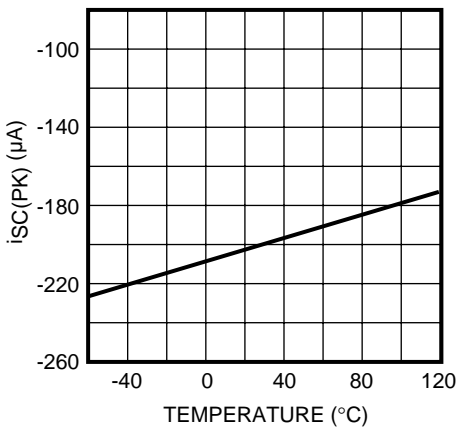
FREQUENCY AT DRV PIN vs. TIMING CAPACITANCE



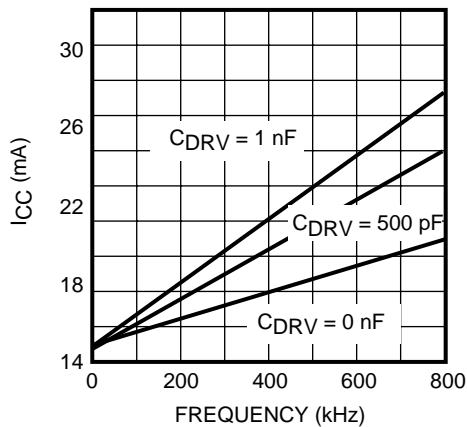
CURRENT CONTROL REFERENCE vs. TEMPERATURE



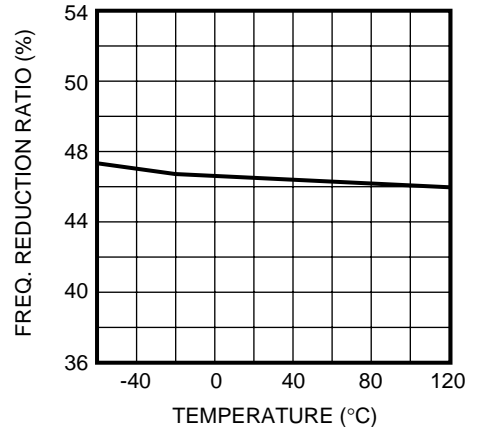
SLOPE COMPENSATION PEAK CURRENT vs. TEMPERATURE

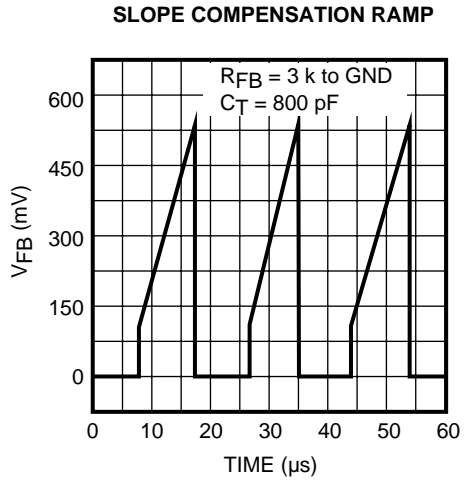


INPUT CURRENT vs. FREQUENCY AT DRV



FREQUENCY REDUCTION RATIO vs. TEMPERATURE



TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

THEORY OF OPERATION

The TK75001 is intended for use as a primary-side Pulse Width Modulator (PWM) controller. The many features integrated into a simple 5-pin design allow it to be easily configured for voltage-mode or current-mode control, fixed-frequency or fixed-off-time operation, off-line bootstrapping, and direct drive of a power MOSFET. The polarity of the feedback signal allows for simpler interface with a TL431-derived error signal (see "Applications Information" section).

The most noteworthy integrated feature in the TK75001 is the way in which the feedback control pin is configured to receive the error signal and the current signal for current-mode control. Rather than receiving both inputs into a comparator, a single input receives both signals summed together and compares them against a fixed internal reference. This yields two desirable effects: 1) a current-limit threshold is automatically established, and 2) the required error-signal polarity is the inverse of that of a standard two-input current-mode control system. Generally, the signal summation requires no additional external components and the required error-signal polarity is simpler to achieve.

Two other functions are integrated into the feedback pin. A current ramp, which can be used to establish either the slope-compensation ramp for a current-mode control design or the voltage-comparison ramp for a voltage-mode control design, flows out of the feedback pin. By adjusting the terminating resistance at the feedback pin, the desired ramp magnitude is established. For overcurrent protection, a second fixed-reference comparator monitors the feedback pin. If the feedback pin voltage should reach the second threshold, this indicates that cycle-by-cycle PWM control is not sufficient for maintaining control of the current (i.e., the minimum duty-ratio is too large to achieve volt-second balance in the magnetics). The overcurrent detection comparator latches (for one cycle) a reduction in the source current which feeds the timing capacitor. This has the effect of reducing the switching frequency and thus, effectively, the minimum duty ratio, which is just what is needed to maintain control of the current.

The switching frequency is determined by an internal current source charging an external timing capacitor. The timing capacitor is ramped between internally-fixed thresholds, valley to peak, and then quickly discharged. A fixed off-time control technique can be readily implemented by using a small transistor to keep the timing capacitor discharged during the on-time. When the on-pulse is

terminated, the timing capacitor ramps up to a fixed threshold at a fixed rate to fix the off-time.

The Undervoltage Lockout (UVLO) feature with hysteresis minimizes the start-up current which allows a low-power bootstrap technique to be used for the housekeeping power. The duty ratio of the TK75001 is limited to less than fifty percent by a toggle flip-flop, plus time required to discharge the timing ramp.

PIN DESCRIPTIONS

SUPPLY VOLTAGE PIN (V_{CC})

This pin is connected to the supply voltage. The IC is in a low current (500 μ A typ.) standby mode before the supply voltage exceeds 14.5 V (typ.), which is the upper threshold of the UVLO circuit. The IC switches back to standby mode when the supply voltage drops below 10.5 V (typ.). An internal clamp limits the peak supply voltage to about 17.5 V (typ.). The absolute maximum supply voltage from a low impedance source is 16 V. The device is always guaranteed to turn on before the internal clamp turns on.

GROUND PIN (GND)

This pin provides ground return for the IC.

DRIVE PIN (DRV)

This pin drives the external MOSFET with a totem pole output stage capable of sinking or sourcing a peak current of about 1 A. In standby mode, the drive pin can sink about 5 mA while keeping the drive pin pulled down to about 1 V. The maximum duty cycle of the output signal is typically 44%.

TIMING CAPACITOR PIN (C_T)

The external timing capacitor is connected to the C_T pin. That capacitor is the only component needed for setting the clock frequency. The frequency measured at the C_T pin is twice the frequency measured at the DRV Pin. The maximum recommended clock frequency of the device is 1.6 MHz. At normal operation, during the rising section of the timing-capacitor voltage, a trimmed internal current of 205 μ A flows out from the C_T pin and charges the capacitor. During the falling section of the timing-capacitor voltage an internal current of about 1.8 mA discharges the capacitor. If the voltage at the feedback (FB) pin exceeds 1.35 V (e.g., due to the turnoff delay during a short-circuit at the output of a converter using the IC), the charging current is reduced to about 59 μ A, leading to a 2.17-fold reduction in switching frequency. The frequency reduction is useful for preventing short-circuit current runaway.

FEEDBACK PIN (FB)

The feedback pin receives the sum of three signals: the error signal (from the external error amplifier), the switch current signal and a voltage ramp generated across the terminating resistance by an internal sawtooth-shaped

current with a peak value of about 200 μ A. The error signal is needed for stabilizing the output voltage or current. The switch current signal is needed in current-mode controlled converters and in converters with cycle-by-cycle overload protection. Also, the switch current signal is required for detecting impending short-circuit current runaway, and for initiating a frequency reduction for preventing the runaway. The voltage ramp is needed for slope compensation in current-mode controlled converters, or for pulse-width modulation in voltage-mode controlled converters.

At higher clock frequencies, the bandwidth limitation of the internally-generated sawtooth-shaped current source becomes more apparent. The degree to which ramp bandwidth is tolerable depends on performance requirements at narrow pulse widths. A low impedance at the feedback pin can effectively eliminate the internally-generated ramp effects, and an external ramp can be readily created to attain higher performance at high frequencies, if desired.

DESIGN CONSIDERATIONS

SELECTING A START-UP RESISTOR

Figure 1 shows the typical application of the TK75001 in an off-line flyback power supply (input full-wave bridge and capacitor not shown). The IC starts when the voltage across the capacitor C_{AUX} reaches the UVLO on Voltage $V_{IN(ON)}$ of the IC. The starting resistor R_{ST} can be designed as follows:

$$R_{ST(MAX)} = (V_{IN(MIN)} - V_{CC(ON,MAX)} - 2 \text{ V}) / I_{CC(START, MAX)} \quad (1)$$

At 85 Vrms line voltage, and taking into account the specified maximum values of the UVLO on voltage and the start-up supply current $I_{CC(START)}$, the maximum allowed value of the starting resistor is:

$$R_{ST(MAX)} = (85 \sqrt{2} - 16 - 2) / 1.0 \text{ mA} = 102.2 \text{ k}\Omega \quad (2)$$

A practical choice for the starting resistor is $R_{ST} = 100 \text{ k}\Omega$. The worst-case dissipation of the resistor appears at high line and at the minimum V_{CC} voltage. At 265 Vrms line voltage and 9 V V_{CC} , the dissipation is 2.2 W, so a 3 W resistor should be used. Note that 1.0 mA reflects the worst case $I_{CC(START)}$ at the edge of UVLO release.

SELECTING THE TRANSFORMER TURNS RATIO

During steady-state operations, the auxiliary supply voltage is generated by the auxiliary winding n_3 and the rectifier diode D_3 . In the flyback power supply, neglecting the effect of the leakage inductance of the transformer, the number of turns of the auxiliary winding can be calculated from the following equation:

$$n_3 = n_2 [(V_{AUX} + V_{D3}) / (V_{OUT} + V_{D2})] \quad (3)$$

where V_{D2} and V_{D3} are the forward voltage drops of the output rectifier diode and the auxiliary rectifier diode. The voltage V_{AUX} should be selected such that it stays between the specified worst-case upper and lower limits of the IC,

considering the component tolerances, ripple, and other second-order effects. The upper limit for V_{AUX} is the minimum voltage of the built-in clamp (16 V). The lower limit for V_{AUX} is the maximum UVLO off voltage (12.0 V). It is prudent to choose the mean value of those two voltages (i.e., 14.0 V), as V_{AUX} .

COMPENSATING FOR LEAKAGE INDUCTANCE

The leakage inductance of the flyback transformer causes a voltage overshoot at turn-off of the MOSFET. The magnitude and duration of the overshoot depends on the leakage inductance, the peak current at turn-offs, and the voltage-clamping circuit employed to limit the overshoot.

The overshoot tends to increase the auxiliary voltage. The simplest solution to reduce that increase is to add a resistor R_{AUX} in series with the rectifier diode D_3 . The optimal value of the resistor can be calculated from the subcircuit shown in Figure 2.

The average current flowing in R_{AUX} is equal to the current I_{AUX} drawn by the IC. The following equation can be written from the equality:

$$I_{AUX} = (1 / R_{AUX}) \times [(V_1 - V_{D3} - V_{AUX}) \times (T_1 / T)] + [(V_2 - V_{D3} - V_{AUX}) \times (T_2 / T)] \quad (4)$$

The voltage V_1 can be calculated as follows:

$$V_1 = (V_{OUT} + V_{D2}) \times (n_1 / n_2) + [V_{OVERSHOOT} \times (n_3 / n_2)] \quad (5)$$

where $V_{OVERSHOOT}$ is the additional voltage appearing across the MOSFET due to the leakage inductance.

The voltage V_2 can be calculated as follows:

$$V_2 = (V_{OUT} + V_{D2}) \times (n_3 / n_2) \quad (6)$$

DESIGN CONSIDERATIONS (CONT.)

T_1 is the time required for the leakage inductance of the flyback transformer to completely discharge its stored energy into the voltage clamp. T_1 can be calculated as:

$$T_1 = (I_{PK} \times L_{LEAK}) / V_{OVERSHOOT}$$

(7)

where I_{PK} is the peak current in the MOSFET at turn-off and L_{LEAK} is the inductance of the flyback transformer measured at winding n_1 .

T_2 is the conduction time of the output diode D_2 and T is the switching period.

From Equation 4 the resistance R_{AUX} or the voltage V_{AUX} can be calculated.

Example: calculate the value of R_{AUX} with the following typical values:

| | | |
|----------------------------|---------------------------------|----------------------------|
| $V_{OUT} = 12 \text{ V}$ | $V_{D2} = V_{D3} = 1 \text{ V}$ | $I_{PK} = 1 \text{ A}$ |
| $L_{LEAK} = 2 \mu\text{H}$ | $V_{OVERSHOOT} = 20 \text{ V}$ | $V_{AUX} = 13.5 \text{ V}$ |
| $I_{AUX} = 18 \text{ mA}$ | $T_2 = 2 \mu\text{s}$ | $T = 5 \mu\text{s}$ |
| $n_1 = 31$ | $n_2 = 6$ | $n_3 = 7$ |

Equations 5, 6 and 7 yield $V_1 = 19.7 \text{ V}$, $V_2 = 15.2 \text{ V}$, and $T_1 = 100 \text{ ns}$. Substituting those values into Equation 4 and solving for R_{AUX} yields:

$$R_{AUX} = 20.6 \Omega$$

Rounding the result to the nearest 5% standard value gives $R_{AUX} = 20 \Omega$.

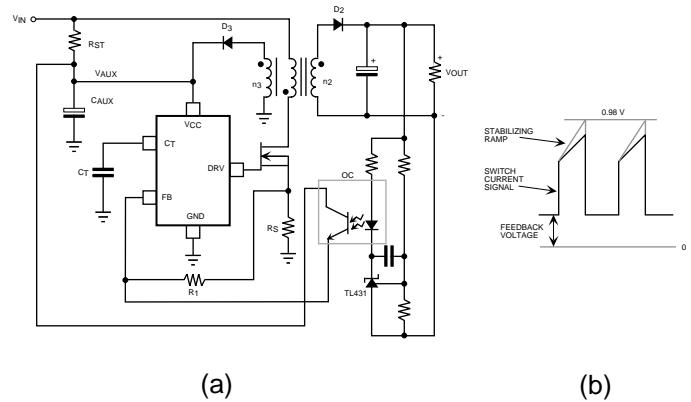


FIGURE 1: TK75001 IN A FLYBACK POWER SUPPLY
(a) SCHEMATIC (b) VOLTAGE AT FEEDBACK PIN

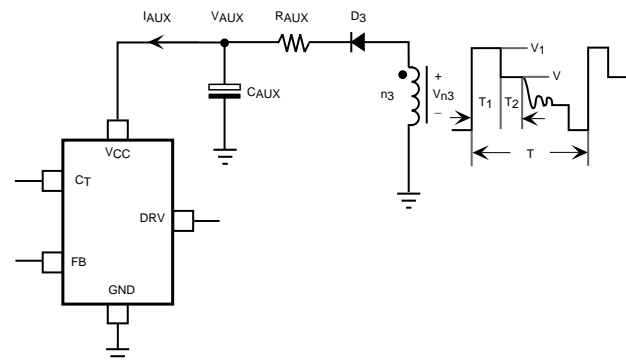


FIGURE 2: SUBCIRCUIT FOR CALCULATING THE VALUE OF R_{AUX}

APPLICATION INFORMATION

SELF-BIASED POWER SUPPLY WITH CONSTANT-FREQUENCY CURRENT-MODE CONTROL

Figure 3(a) shows the TK75001 IC in the typical application: a flyback converter with self-bias and constant-frequency current-mode control. Figure 3(b) shows the FB Pin voltage. In the converter, the voltage-error amplifier (a TL431 shunt regulator IC) is located at the output side and the error signal is transmitted to the input side through the optocoupler OC. Three signals are added together at the FB Pin: 1) the feedback voltage that develops across the resistor R_1 , 2) the switch current signal, and 3) the stabilizing ramp. In each cycle, the MOSFET switch is turned off when the sum of those three signals reaches 0.98 V.

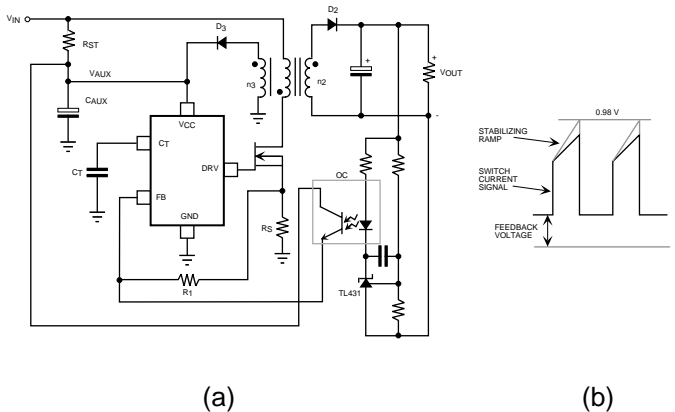


FIGURE 3: TK75001 IN A SELF-BIASED FLYBACK CONVERTER WITH CONSTANT-FREQUENCY VOLTAGE-MODE CONTROL
(a) SCHEMATIC (b) VOLTAGE AT FEEDBACK PIN

POWER SUPPLY WITH CONSTANT-FREQUENCY VOLTAGE-MODE CONTROL AND CYCLE-BY-CYCLE CURRENT LIMIT

Voltage-mode control is free from some of the disadvantages (e.g., subharmonic instability and noise sensitivity) of current-mode control. It is very easy to implement that control method with the TK75001 IC. Figure 4(a) shows the IC in a voltage-mode-controlled flyback converter. Figure 4(b) shows the feedback pin voltage. The only circuit difference between current-mode control and voltage-mode control is in the connection of the resistor R_1 , that terminates the feedback pin. In current-mode control, that resistor is connected to the current-

sense resistor of the converter. In voltage-mode control, that resistor is connected to ground.

In voltage-mode control, overload protection can be realized by adding a simple circuit to the control IC, as shown in the figure. The PNP transistor Q_1 , turns on and pulls up the feedback pin when the switch current times the resistance of the sense R_S reaches the threshold set by the resistive divider R_2 and R_3 and the base-emitter voltage of Q_1 .

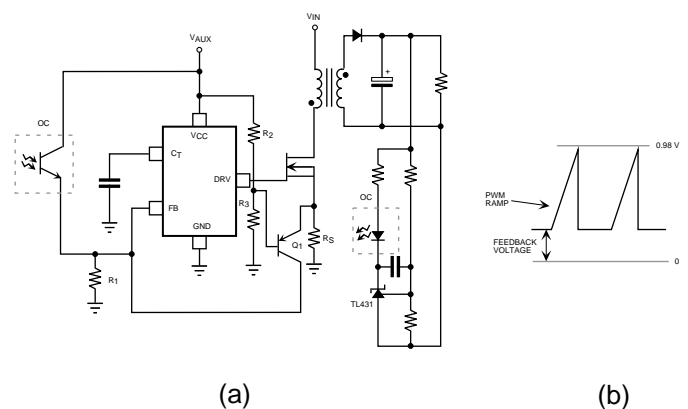


FIGURE 4: TK75001 IN A VOLTAGE-MODE-CONTROLLED CONVERTER WITH ADDITIONAL CYCLE-BY-CYCLE CURRENT LIMIT
(a) SCHEMATIC (b) VOLTAGE AT FEEDBACK PIN

POWER SUPPLY WITH CONSTANT OFF-TIME CURRENT-MODE CONTROL

The advantages of constant off-time current-mode control over constant-frequency current-mode control are: 1) there is no need for a stabilizing ramp, 2) the converter is free from subharmonic instability (i.e., there is no need for slope compensation), and 3) the line voltage variation is automatically canceled in buck-derived converters (e.g., the forward converter). Figure 5 shows the implementation of that control method. As can be seen, a transistor Q_1 must be added to the controller. Figure 6 shows the timing-pin and feedback pin voltages for the TK75001. The transistor Q_1 keeps the timing pin at ground potential during the on-time of the switch. Timing begins when the drive output returns to low and Q_1 is turned off. The off-time for typical charge and discharge currents and peak and valley voltages is:

$$t_{\text{OFF}} = C_T \times 14 \text{ k}\Omega.$$

APPLICATION INFORMATION (CONT.)

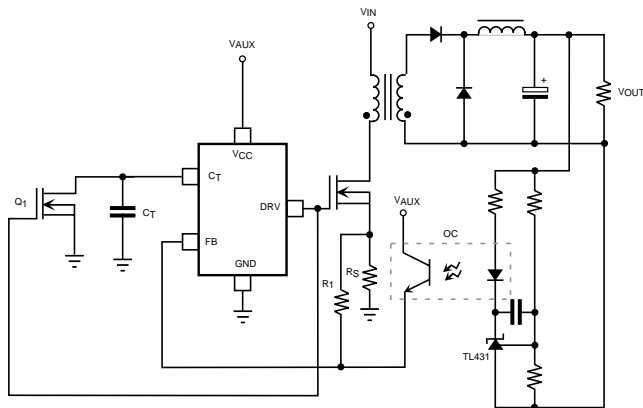


FIGURE 5: TK75001 IN A FORWARD CONVERTER WITH CONSTANT OFF-TIME CURRENT-MODE CONTROL

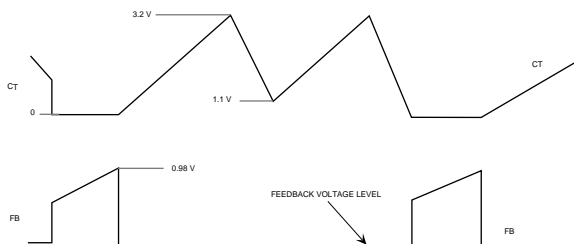


FIGURE 6: TIMING PIN AND FEEDBACK PIN VOLTAGES WITH CONSTANT OFF-TIME CURRENT-MODE CONTROL

TK75001 IN NON-ISOLATED APPLICATIONS

Figure 7 shows a buck-boost converter with a negative input voltage and a positive output voltage, controlled by the TK75001. The Error Amplifier is a TL431 shunt regulator, and a PNP transistor provides interface between the TL431 and the control IC.

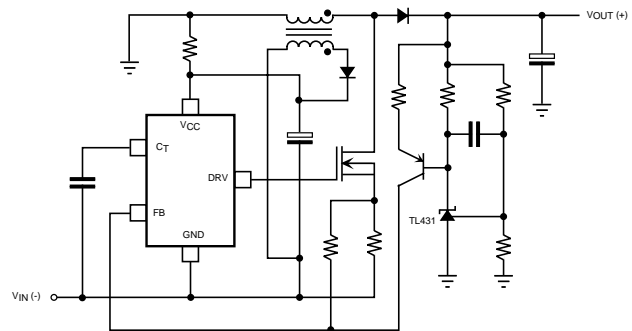


FIGURE 7: NON-ISOLATED NEGATIVE-TO-POSITIVE CONVERTER

APPLICATION INFORMATION (CONT.)

TK75001 OFF-LINE APPLICATION EXAMPLE

Figure 8 shows an off-line, universal input, 12 W power supply. The TK75001 is the controller IC for a flyback converter with self-bias and constant-frequency, current-mode control. The TK75001 drives the MOSFET directly to switch the flyback transformer. Feedback is accomplished by means of a TL431, configured as a secondary side error amplifier and voltage reference, driving an opto-coupler for isolation.

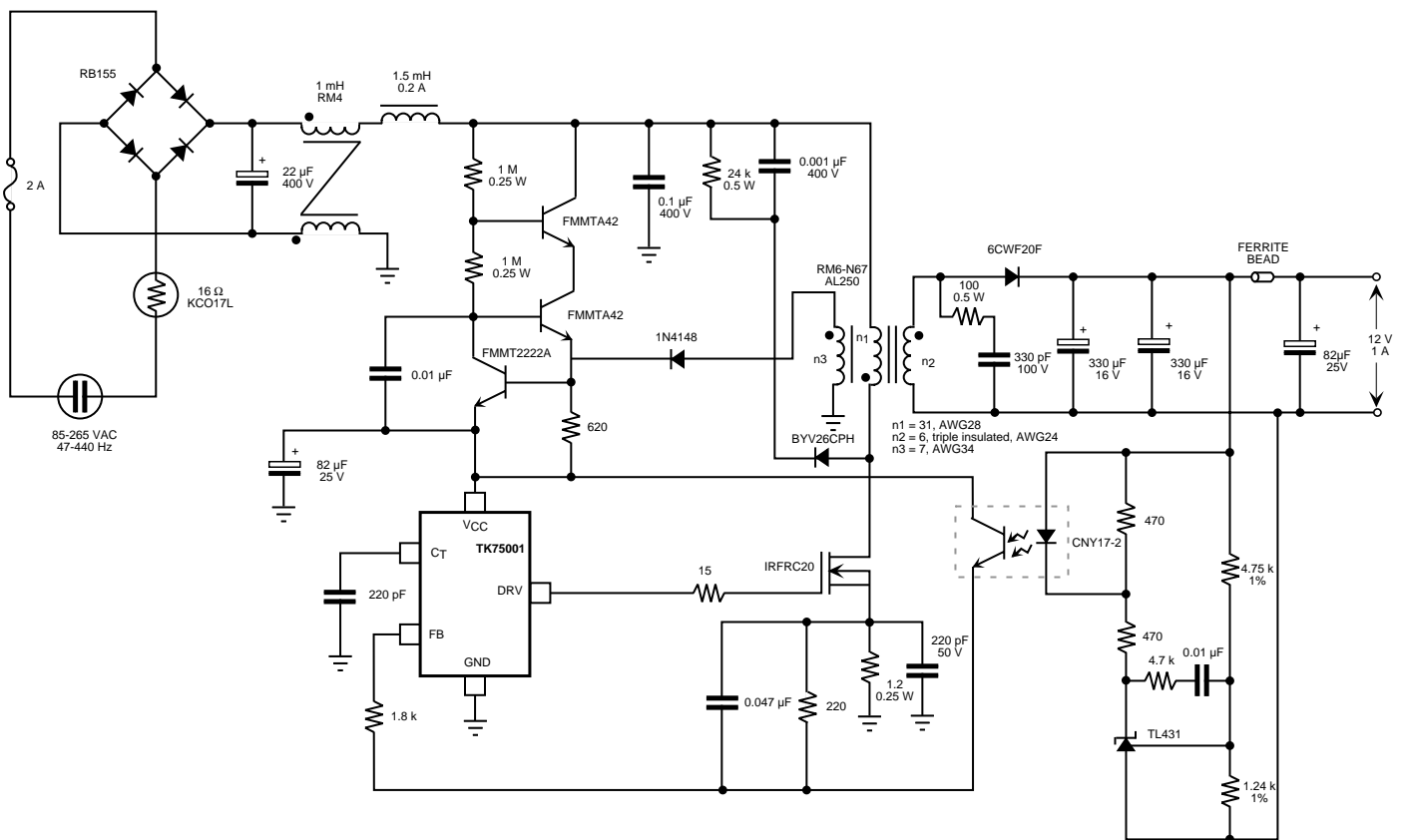
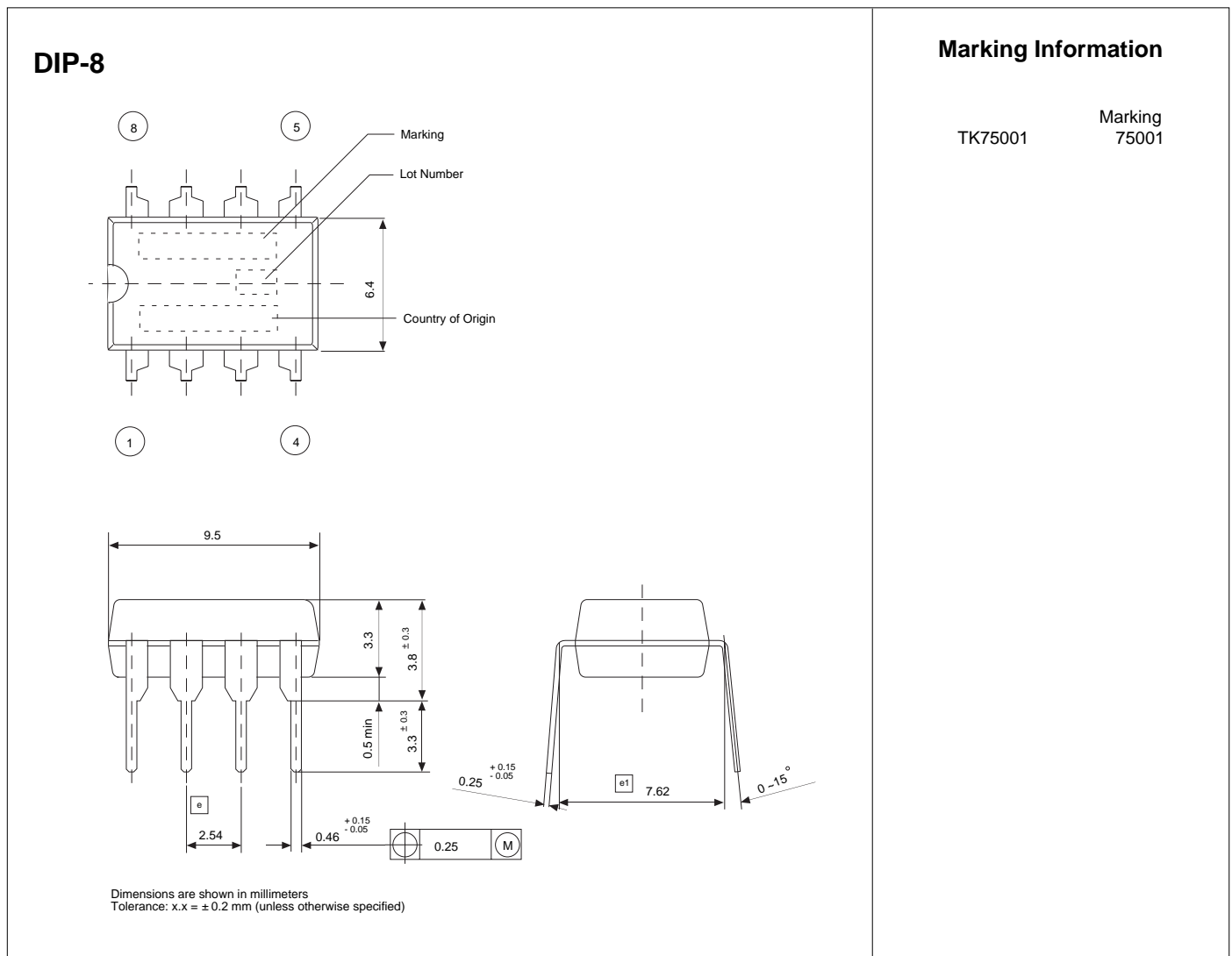


FIGURE 8: OFF-LINE, UNIVERSAL INPUT, 12-WATT POWER SUPPLY

PACKAGE OUTLINE



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