

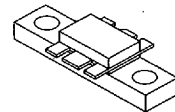
The RF Line UHF Power Transistor

The TP3021 is designed for 24 V common emitter base station amplifiers. Operating in the 820–960 MHz bandwidth, it has been specifically designed for use in analog and digital (GSM) systems as a medium power output device.

- Specified 24 Volts, 960 MHz Characteristics
 - Output Power = 10 Watts
 - Minimum Gain = 10 dB
 - Class AB
 - $I_Q = 60$ mA
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

TP3021

10 W, 960 MHz
UHF POWER
TRANSISTOR
NPN SILICON



CASE 319-07, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	27	Vdc
Collector–Base Voltage	V_{CBO}	48	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	2.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	35 0.35	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	–65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1) at 70°C Case	$R_{\theta JC}$	5.0	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Collector–Emitter Breakdown Voltage ($I_C = 25$ mA, $R_{BE} = 75 \Omega$)	$V_{(BR)CER}$	40	—	—	Vdc
Emitter–Base Breakdown Voltage ($I_C = 5.0$ mAdc)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector–Base Breakdown Voltage ($I_E = 50$ mAdc)	$V_{(BR)CBO}$	48	—	—	Vdc
Collector–Emitter Leakage ($V_{CE} = 26$ V, $R_{BE} = 75 \Omega$)	I_{CER}	—	—	5.0	mA

ON CHARACTERISTICS

DC Current Gain ($I_C = 1.0$ Adc, $V_{CE} = 10$ Vdc)	h_{FE}	15	—	100	—
--	----------	----	---	-----	---

NOTE:

- Thermal resistance is determined under specified RF operating condition.

(continued)

REV 6

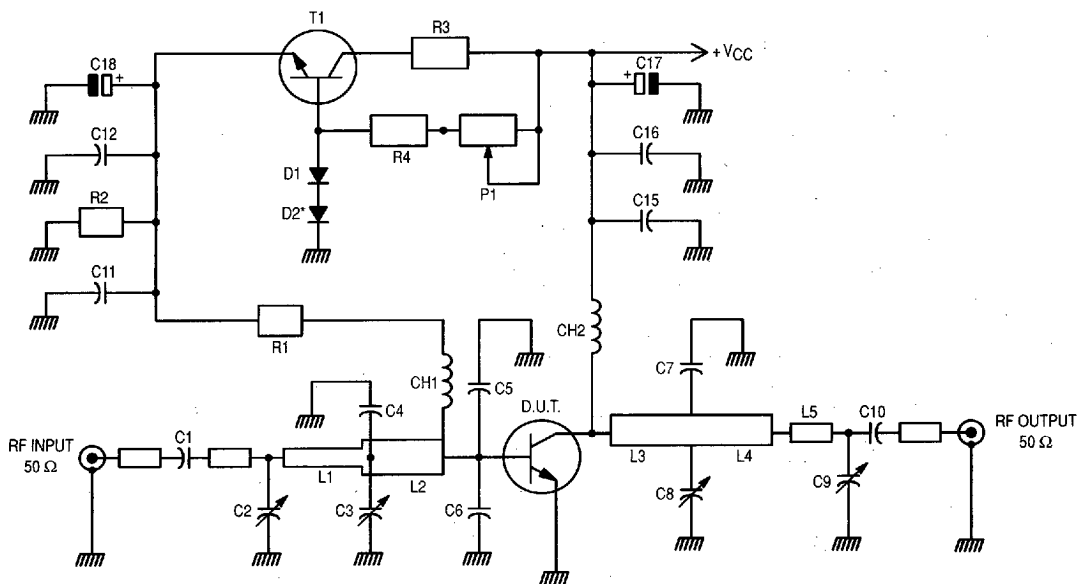
MOTOROLA RF DEVICE DATA

TP3021
2-981

■ 6367254 0107345 286 ■

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 24\text{ V}$, $I_E = 0$, $f = 1.0\text{ MHz}$)	C_{ob}	15	—	25	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain ($V_{CC} = 24\text{ V}$, $P_{out} = 10\text{ W}$, $I_{CQ} = 60\text{ mA}$, $f = 960\text{ MHz}$)	G_p	10	—	—	dB
Load Mismatch ($V_{CC} = 26\text{ V}$, $P_{out} = 10\text{ W}$, $I_{CQ} = 60\text{ mA}$, Load VSWR = 20:1, at all phase angles)	ψ	No Degradation in Output Power Before and After Test			
Collector Efficiency ($V_{CC} = 24\text{ V}$, $P_{out} = 10\text{ W}$, $f = 960\text{ MHz}$)	η_c	50	55	—	%



*D2 is in Physical Contact with RF Transistor

- C1, C10, C11, C15 — Capacitor Chip 0805 330 pF 5%
- C2, C4, C8, C9 — Trimmer Capacitor 0.5–4.0 pF
- C4 — Capacitor Chip 0805 3.9 pF 5%
- C5, C6 — Capacitor Chip 15 pF HQ
- C7 — Chip Resistor 0805 8.2 pF
- C12, C16 — Capacitor Chip 0805 15 nF 5%
- C17, C18 — Capacitor Chip 0805 6.0, 8.0 μF 35 V
- CH1 — Microstrip Line 80 Ω L = 40 mm
- CH2 — Microstrip Line 80 Ω L = 23 mm
- D1, D2 — Diode 1N4148

- L1 — Microstrip Line 50 Ω L = 20 mm
- L2 — Microstrip Line 25 Ω L = 13 mm
- L3 — Microstrip Line 25 Ω L = 10 mm
- L4 — Microstrip Line 50 Ω L = 5 mm
- L5 — Microstrip Line 50 Ω L = 7 mm
- P1 — Trimmer 5.0 kΩ
- R1 — Chip Resistor 2.2 Ω 1206 5%
- R2 — Chip Resistor 75 Ω 0805 5%
- R3 — Resistor 100 Ω 2.0 W
- R4 — Resistor 1.0 kΩ 5%
- T1 — Transistor BD135 or Similar

Board Material — 1/50", Teflon Glass, Cu Clad 2 Sides, 35 μm Thick

Figure 1. 960 MHz Test Circuit

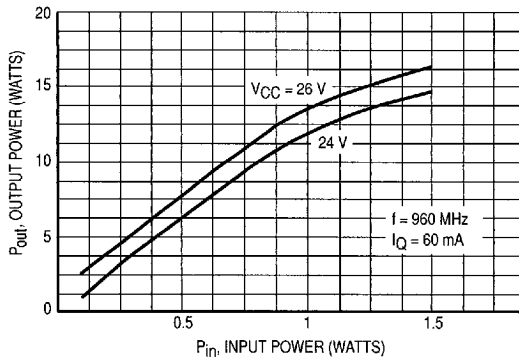
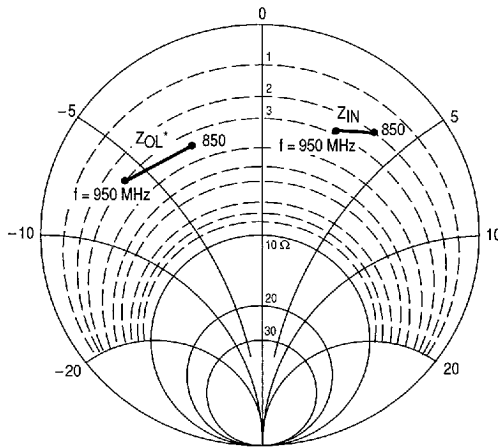


Figure 2. Output Power versus Input Power



$P_{out} = 10 \text{ W}$ $V_{CE} = 24 \text{ V}$

f MHz	Z_{IN} OHMS	Z_{OL}^* OHMS
850	$2.4 + j3.5$	$3.4 - j3.2$
900	$2.6 + j3.4$	$3.1 - j4.4$
950	$2.8 + j3.4$	$2.7 - j6.2$

Z_{OL}^* = Conjugate of the optimum load impedance. Into which the device operates at a given output power, voltage, and frequency.

Figure 3. Series Equivalent Input/Output Impedances

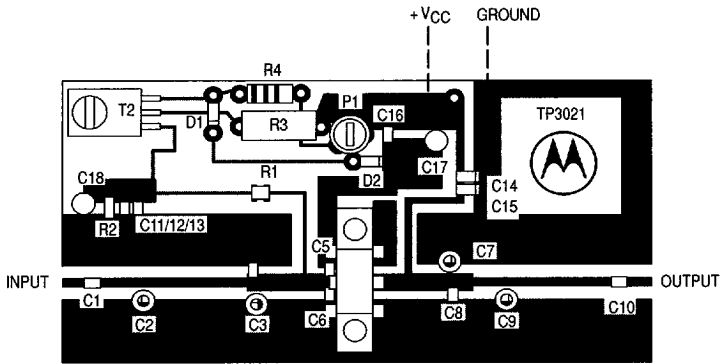


Figure 4. Test Circuit — Component Locations