

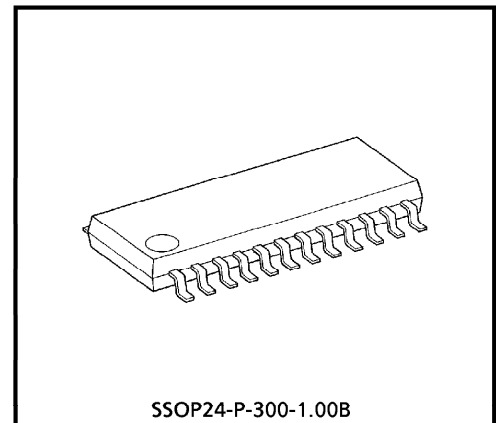
# TPD2007F

## LOW-SIDE POWER SWITCH ARRAY (8 CHANNELS) for MOTORS, SOLENOIDS, and LAMP DRIVES

The TPD2007F is an 8-channel low-side switch array for vertical power MOS FET output. A monolithic power IC, it can directly drive a power load from a CMOS or TTL logic circuit (such as an MPU). It offers overcurrent and overtemperature protection functions.

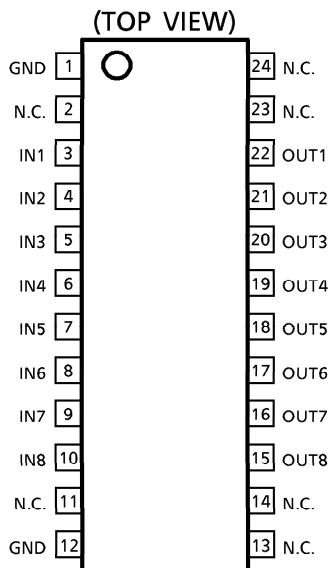
**FEATURES**

- A low-side switch array incorporating an N-channel power MOS FET. (1.4 Ω max.)
- Can directly drive a power load from a microprocessor.
- Built-in protection against overtemperature protection and overcurrent protection.
- 8-channel access enables space-saving design.
- High operating voltage : 40 V
- Low on-resistance : 1.4 Ω max. @V<sub>DD</sub> = 12 V, I<sub>O</sub> = 0.5 A (per channel)
- Supports parallel operation.
- Built-in an active clamp circuit
- Supplied in an SSOP-24 package (300 mil) in embossed taping.

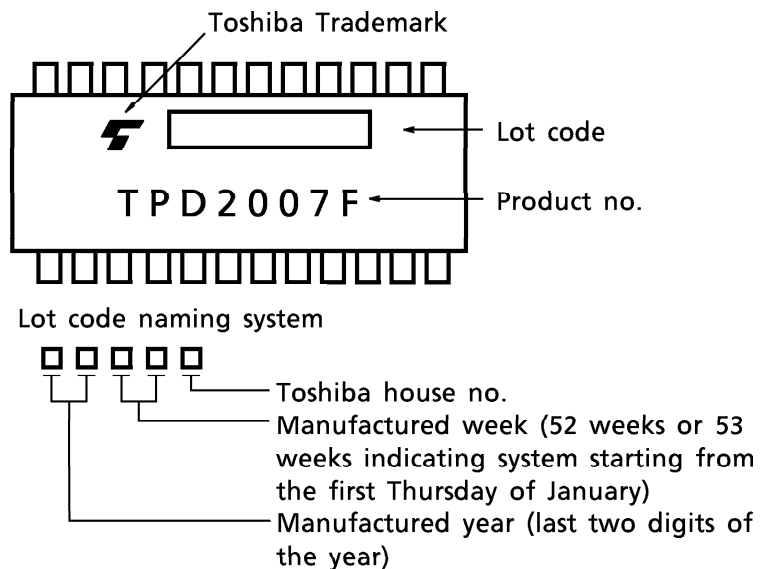


Weight : 0.29 g (typ.)

**PIN ASSIGNMENT**



**MARKING**

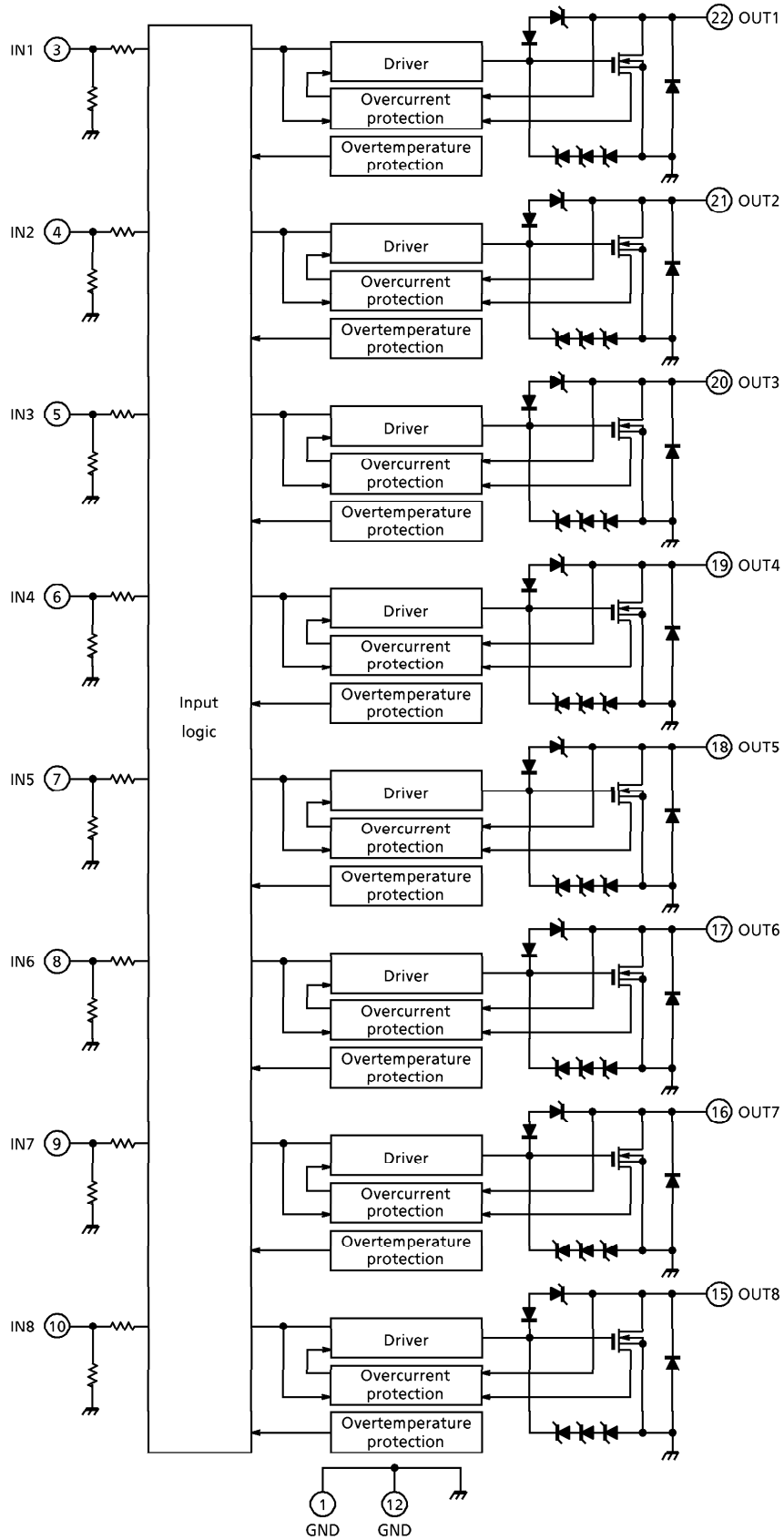


This device uses MOS structure, it is sensitive to electrostatics. Please take this into account.

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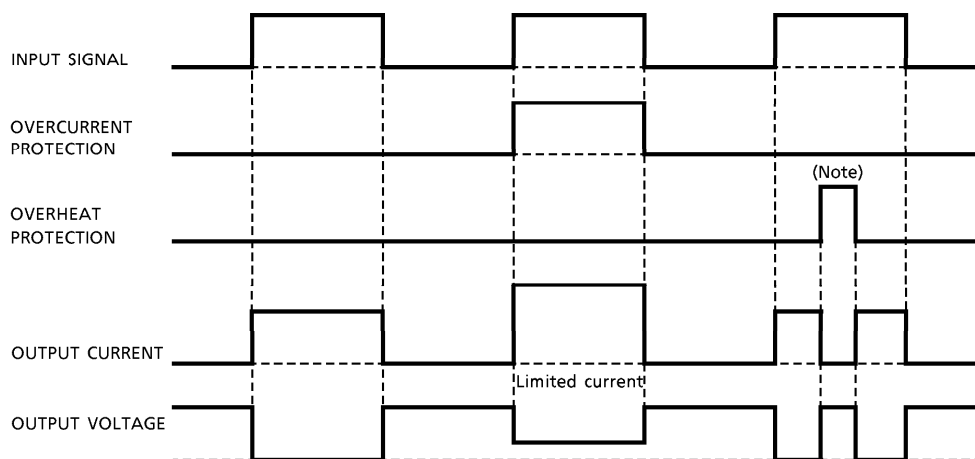
BLOCK DIAGRAM



**PIN DESCRIPTION**

PIN No.	SYMBOL	DESCRIPTION
1	GND	GND pin; in common with the pin no.12 internally.
2	N.C.	—
3	IN1	Control input pin for channel 1 and built-in pull-down resistor (300 kΩ typ.)
4	IN2	Control input pin for channel 2 and built-in pull-down resistor (300 kΩ typ.)
5	IN3	Control input pin for channel 3 and built-in pull-down resistor (300 kΩ typ.)
6	IN4	Control input pin for channel 4 and built-in pull-down resistor (300 kΩ typ.)
7	IN5	Control input pin for channel 5 and built-in pull-down resistor (300 kΩ typ.)
8	IN6	Control input pin for channel 6 and built-in pull-down resistor (300 kΩ typ.)
9	IN7	Control input pin for channel 7 and built-in pull-down resistor (300 kΩ typ.)
10	IN8	Control input pin for channel 8 and built-in pull-down resistor (300 kΩ typ.)
11	N.C.	—
12	GND	GND pin; in common with the pin no.1 internally.
13	N.C.	—
14	N.C.	—
15	OUT8	Output pin for channel 8
16	OUT7	Output pin for channel 7
17	OUT6	Output pin for channel 6
18	OUT5	Output pin for channel 5
19	OUT4	Output pin for channel 4
20	OUT3	Output pin for channel 3
21	OUT2	Output pin for channel 2
22	OUT1	Output pin for channel 1
23	N.C.	—
24	N.C.	—

**TIMING CHART**



(Note) : The overheating detector circuits feature hysteresis. After overheating is detected, normal operation is restored only when the junction temperature falls by the hysteresis amount (10°C typ.) in relation to the overheating detection temperature.

**TRUTH TABLE**

INPUT SIGNAL	OUTPUT SIGNAL	STATE
L	H	Normal
H	L	
L	H	Overcurrent protection
H	Internally limited	
L	H	Overtemperature protection
H	H	

**MAXIMUM RATINGS (Ta = 25°C)**

CHARACTERISTIC	SYMBOL	RATING	UNIT
Input Voltage	V <sub>IN</sub>	- 0.5~7	V
Drain-source Voltage	V <sub>DSS</sub>	40	V
Output Current	I <sub>D</sub>	Internally Limited	A
Power Dissipation (Operating All Channels, Ta = 25°C)	P <sub>T</sub>	0.8	W
		1.5 (Note)	
Single Pulse Avalanche Energy	E <sub>AS</sub>	10	mJ
Operating Temperature	T <sub>opr</sub>	- 40~85	°C
Junction Temperature	T <sub>j</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	- 55~150	°C

**THERMAL CHARACTERISTIC**

CHARACTERISTIC	SYMBOL	RATING	UNIT
Thermal Resistance Junction to Ambient (Operating All Channels, Ta = 25°C)	ΣR <sub>th(j-a)</sub>	156.3	°C / W
		83.4 (Note)	

(Note) : 60 mm × 60 mm × 1.6 t when a device is mounted on a glass epoxy PCB. (DC)

**ELECTRICAL CHARACTERISTICS** (Unless otherwise specified, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Drain-Source Clamp Voltage	$V_{(BR)DSS}$	—	$I_D = 10 \text{ mA}, V_{IN} = 0 \text{ V}$	40	—	—	
Input Voltage	$V_{th}$	—	$V_{DS} = 24 \text{ V}, I_{DS} = 1 \text{ mA}$	0.8	—	2.0	V
Input Current	$I_{IL}$	—	$V_{IN} = 0 \text{ V}$	-10	—	10	$\mu\text{A}$
	$I_{IH}$	—	$V_{IN} = 5 \text{ V}$	—	140	300	
On Resistance	$R_{DS(ON)}$	—	$V_{IN} = 5 \text{ V}, I_O = 0.5 \text{ A}$	—	1.0	1.4	$\Omega$
Off Current	$I_{DSS}$	—	$V_{DS} = 40 \text{ V}$	—	—	100	$\mu\text{A}$
Overcurrent Protection	$I_S(1)$	—	$V_{DS} = 12 \text{ V}, V_{IN} = 5 \text{ V}, R_L = 3 \Omega$	1	2	3	A
	$I_S(2)$	—	$V_{DS} = 30 \text{ V}, V_{IN} = 5 \text{ V}, R_L = 3 \Omega$	0.7	—	2	
Overtemperature Protection	Temperature	TSD	—	—	160	—	$^{\circ}\text{C}$
	Hysteresis	$\Delta\text{TSD}$	—	—	10	—	
Switching Time	$t_{ON}$	1	$V_{DD} = 12 \text{ V}, R_L = 24 \Omega, V_{IN} = 0 \text{ V} / 5 \text{ V}$	—	10	50	$\mu\text{s}$
	$t_{OFF}$	1		—	10	50	
Operating Input Voltage Protection Circuit	$V_{IN(P)}$	—	—	4.5	—	6.0	V
Drain-Source Diode Forward Voltage	$V_{DSF}$	—	$I_F = 1 \text{ A}, V_{IN} = 0 \text{ V}$	—	—	1.6	V

**DESCRIPTION OF PROTECTOR CIRCUIT**

(1) Overtemperature Protection

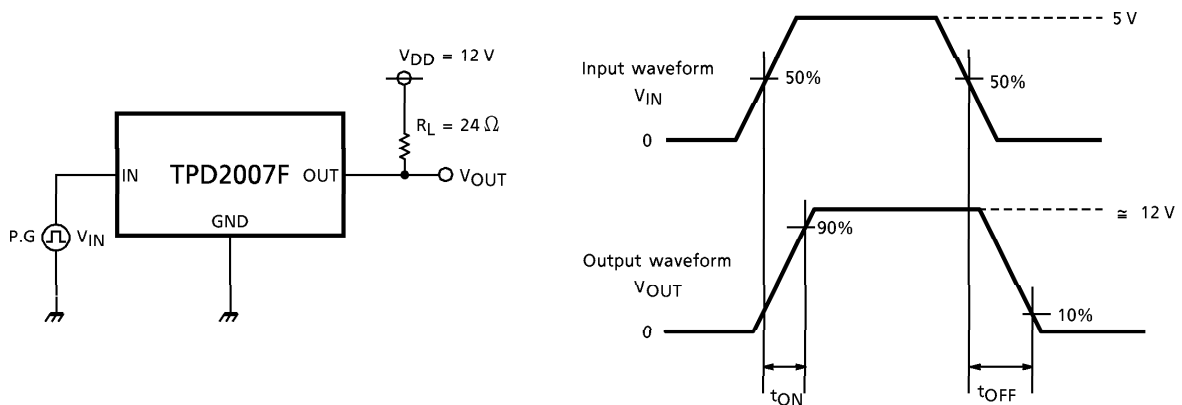
- The overheating detector circuits feature hysteresis. After overheating is detected, normal operation is restored only when the junction temperature falls by the hysteresis amount (10°C typ.) in relation to the overheating detection temperature.

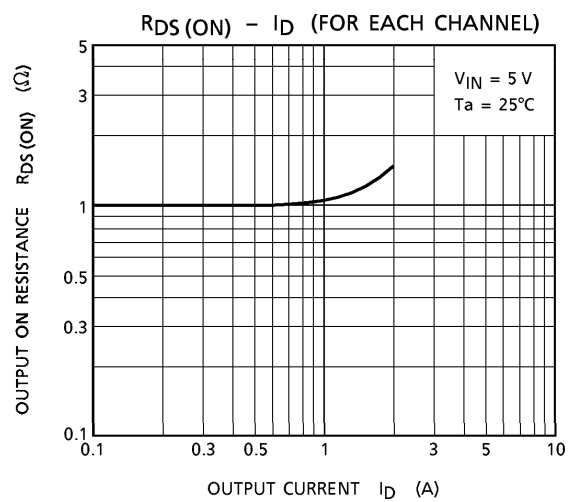
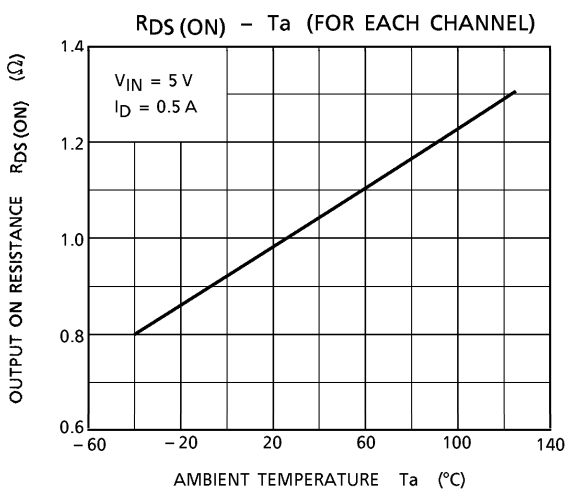
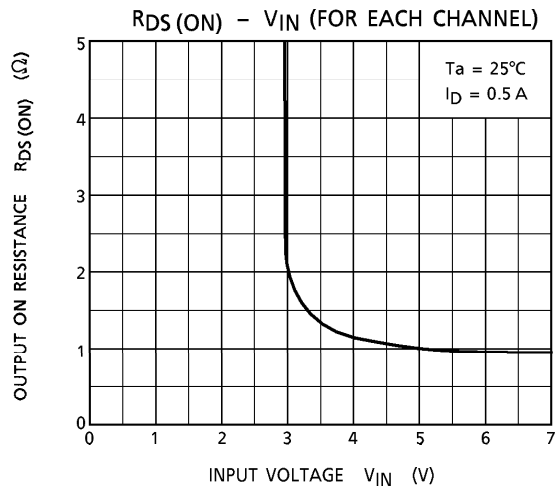
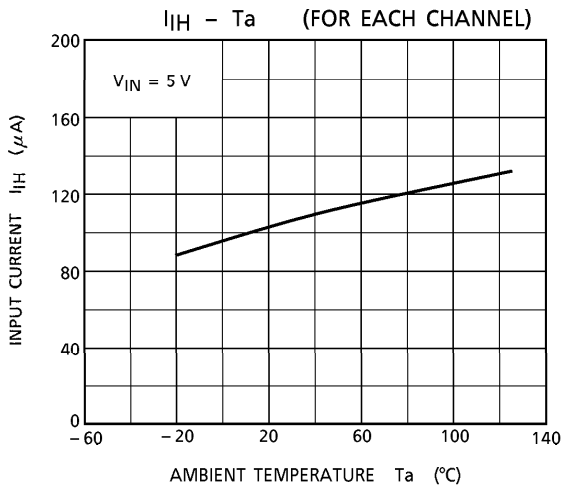
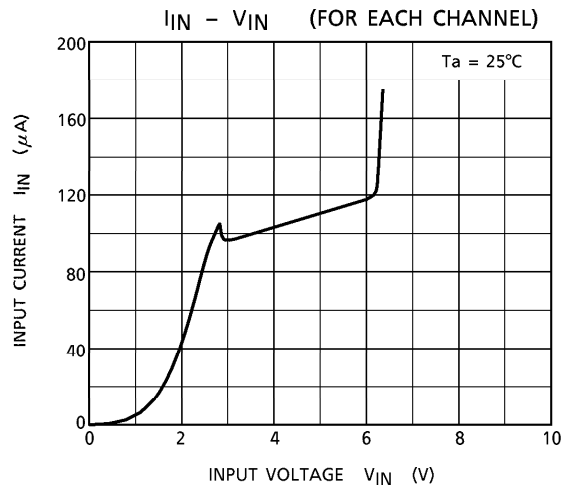
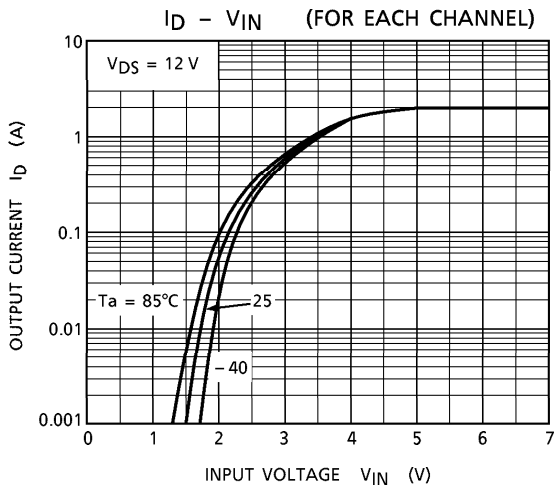
(2) Overcurrent Protection

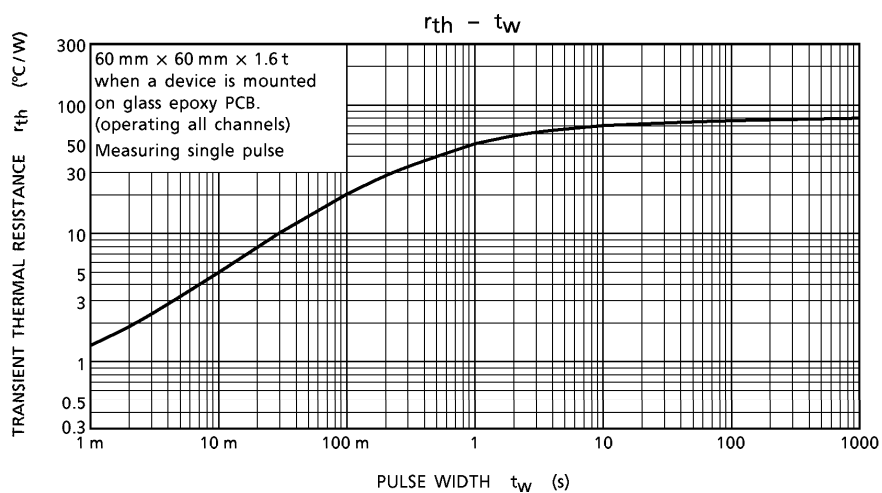
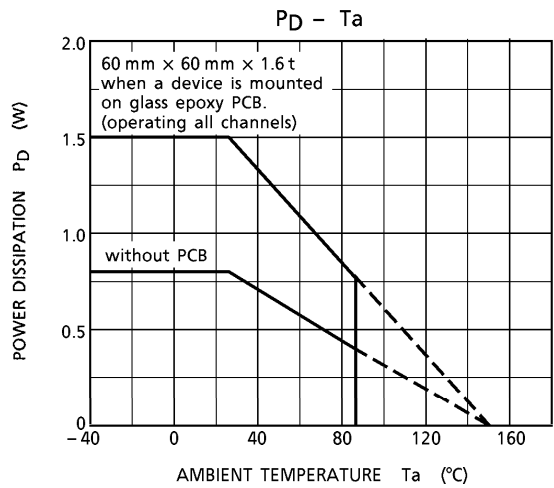
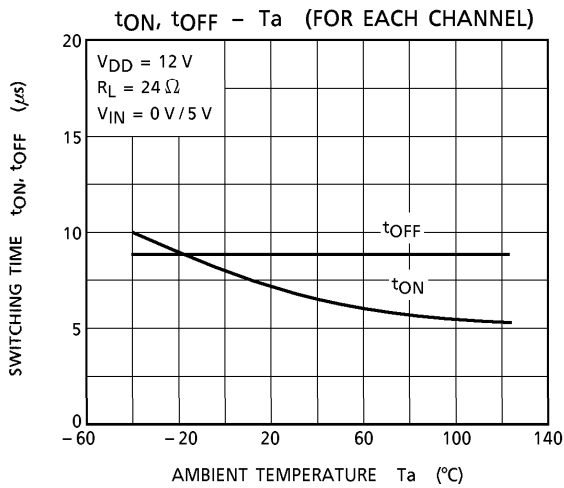
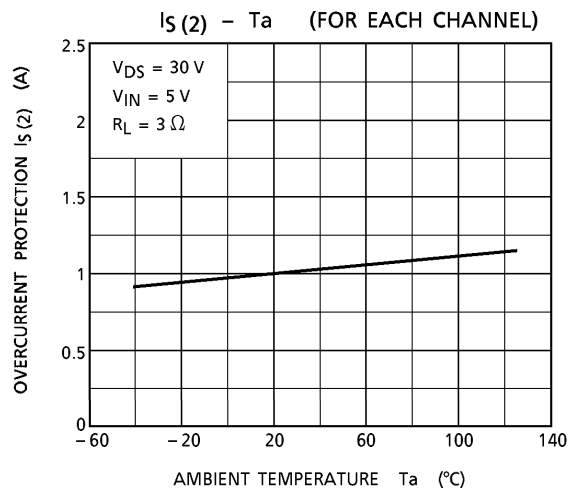
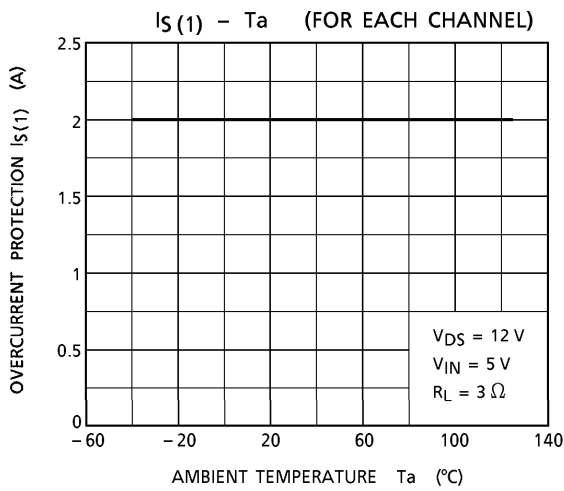
- When overcurrent is detected, the overcurrent limiter function limits the output current. Normal operation is restored when the load current drops below the overcurrent detection value.

**TEST CIRCUIT**

Switching Time







**MOISTURE-PROOF PACKING**

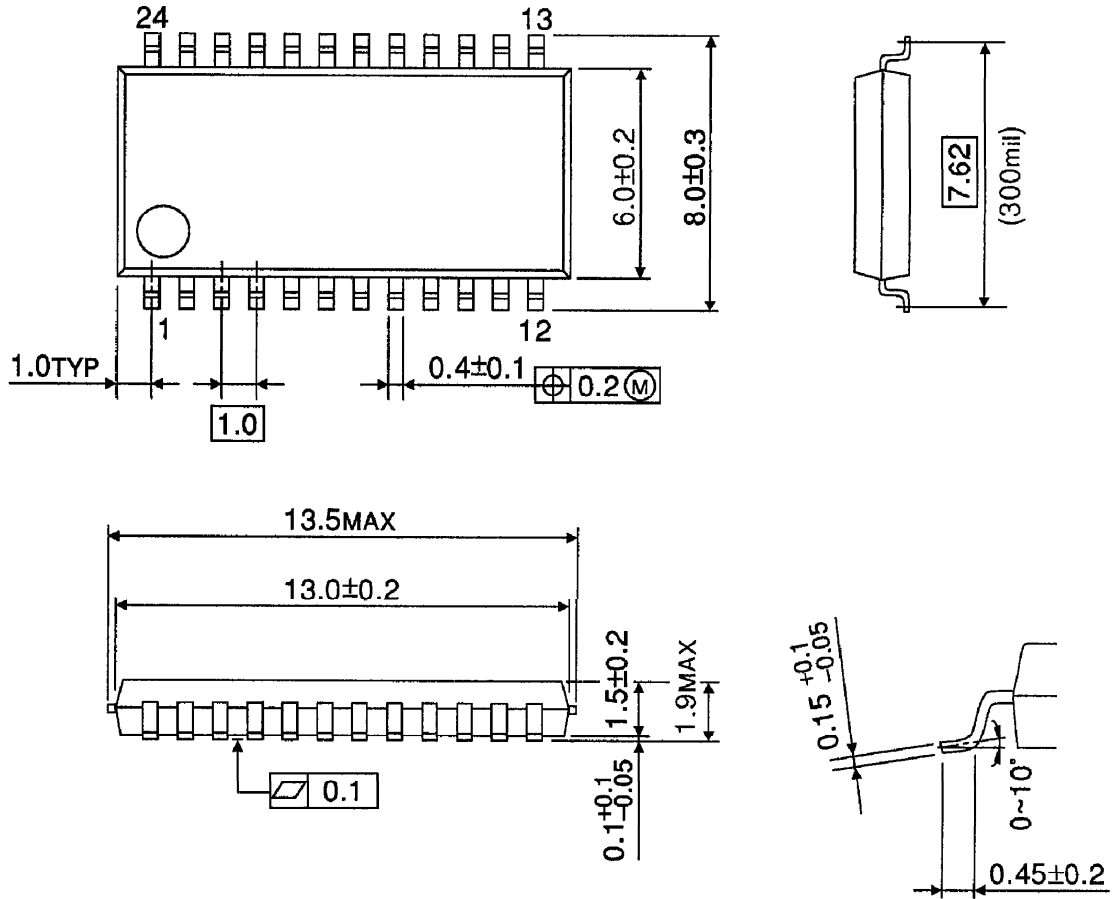
After the pack is opened, use the devices in a 30°C, 60% RH environment, and within the 48 hours. Embossed-tape packing cannot be baked. Devices so packed must be within their allowable time limits after unpacking, as specified on the packing.

Tape packing quantity: 500 devices/reel (EL) or 2000 devices/reel (EL1)



PACKAGE DIMENSIONS  
SSOP24-P-300-1.00B

Unit : mm



Weight : 0.29 g (typ.)