Synchronizing dual D-type flip-flop with metastable immune characteristics

74ABT5074

FEATURES

- Metastable immune characteristics
- Pin compatible with 74F74 and 74F5074
- Typical f_{MAX} = 200MHz
- Output skew guaranteed less than 2.0ns
- High source current (I_{OH} = 15mA) ideal for clock driver applications
- Output capability: +20mA/–15mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT5074 is a dual positive edge-triggered D-type flip-flop featuring individual data, clock, set and reset inputs; also true and complementary outputs.

Set ($\overline{S}$Dn) and reset ($\overline{R}$Dn) are asynchronous active low inputs and operate independently of the clock (CPn) input. Data must be stable just one setup time prior to the low-to-high transition of the clock for guaranteed propagation delays.

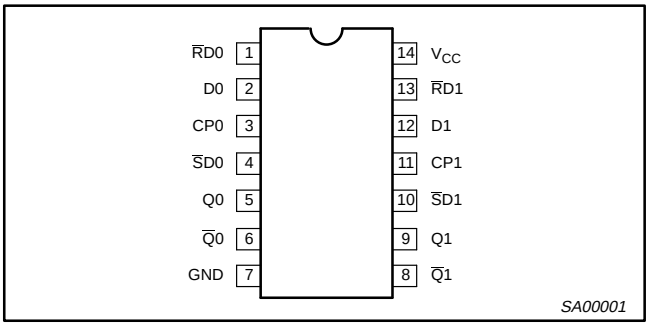
Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the Dn input may be changed without affecting the levels of the output.

The 74ABT5074 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup time and hold time are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74ABT5074 are:

$$\tau \cong 94\text{ps and } T_0 \cong 1.3 \times 10^7 \text{ sec}$$

where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 12	D0, D1	Data inputs
3, 11	CP0, CP1	Clock inputs (active rising edge)
4, 10	$\overline{S}$D0, $\overline{S}$D1	Set inputs (active-Low)
1, 13	$\overline{R}$D0, $\overline{R}$D1	Reset inputs (active-Low)
5, 9	Q0, Q1	Data outputs (active-Low), non-inverting
6, 8	$\overline{Q}$0, $\overline{Q}$1	Data outputs (active-Low), inverting
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	C_L = 50pF; V_{CC} = 5V	2.8 2.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
I_{CC}	Total supply current	Outputs disabled; V_{CC} =5.5V	2	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
14-pin plastic DIP	–40°C to +85°C	74ABT5074N	SOT27-1
14-pin plastic SOL	–40°C to +85°C	74ABT5074D	SOT108-1
14-pin plastic shrink small outline SSOP Type II	–40°C to +85°C	74ABT5074DB	SOT337-1
14-pin plastic thin shrink small outline (TSSOP) Type I	–40°C to +85°C	74ABT5074PW	SOT402-1

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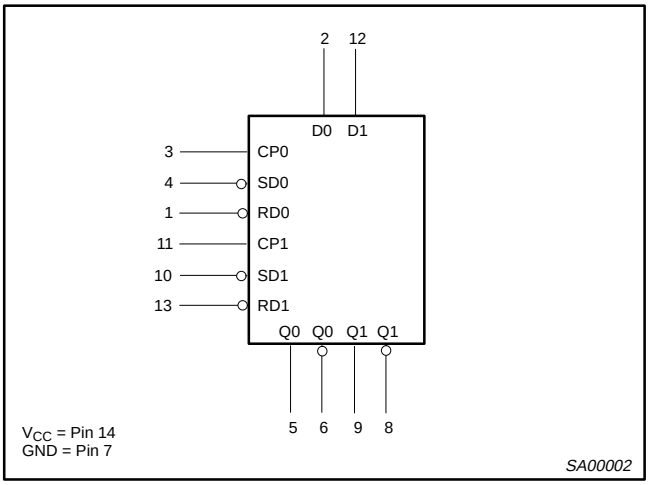
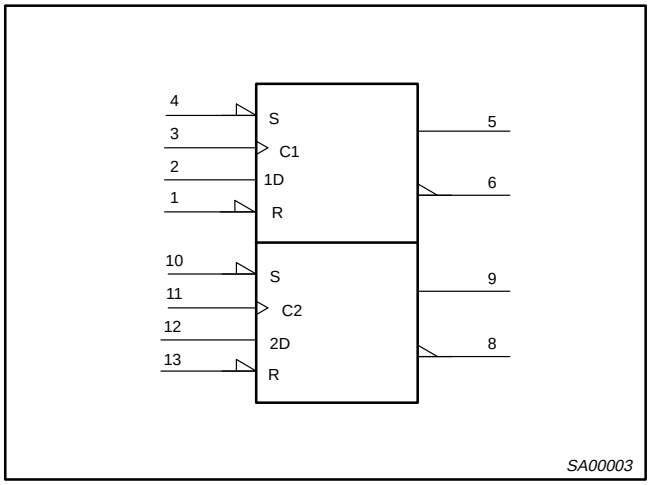
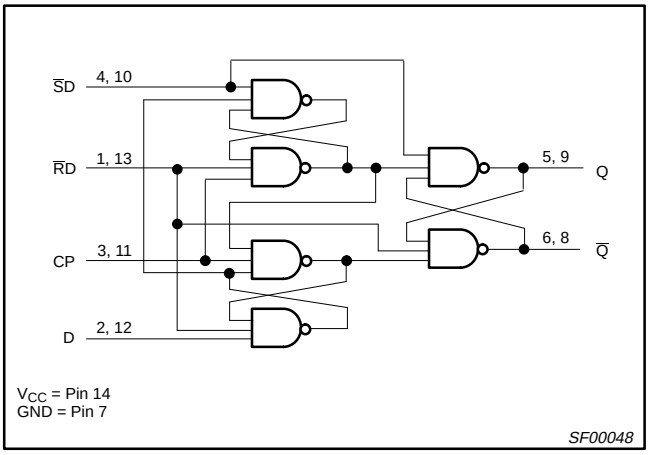
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous set
H	L	X	X	L	H	Asynchronous reset
L	L	X	X	L	H	Undetermined*
H	H	↑	h	H	L	Load ”1”
H	H	↑	l	L	H	Load ”0”
H	H	↥	X	NC	NC	Hold

NOTES:

H = High voltage level
h = High voltage level one setup time prior to low-to-high clock transition
L = Low voltage level
l = Low voltage level one setup time prior to low-to-high clock transition
NC = No change from the previous setup
X = Don’t care
↑ = Low-to-high clock transition
↥ = Not low-to-high clock transition
* = This setup is unstable and will change when either set or reset return to the high level

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METASTABLE IMMUNE CHARACTERISTICS

Philips Semiconductors uses the term 'metastable immune' to describe characteristics of some of the products in its family. By running two independent signal generators (see Figure 1) at nearly the same frequency (in this case 10MHz clock and 10.02MHz data) the device-under-test can often be driven into a metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform. An experiment was run by continuously operating the devices in the region where metastability will occur.

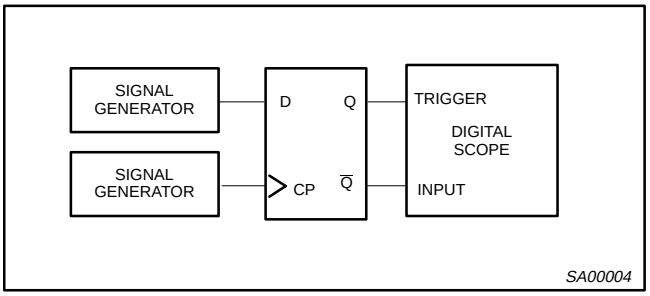


Figure 1. Test Setup

After determining the T_0 and τ of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the 74ABT5074 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz, and has decided that he would like to sample the output of the 74ABT5074 7 nanoseconds after the clock edge. He simply plugs his number into the following equation:

$$MTBF = e^{(t'/\tau)} / T_O * f_C * f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t' > h, h being the normal propagation delay). In this situation the f_I will be twice the data frequency of 20 MHz because input events consist of both of low and high transitions. Multiplying f_I by f_C gives an answer of 10^{15} Hz^2. From Figure 2 it is clear that the MTBF is greater than 10^{10} seconds. Using the above formula the actual MTBF is 1.69×10^{10} seconds or about 535 years.

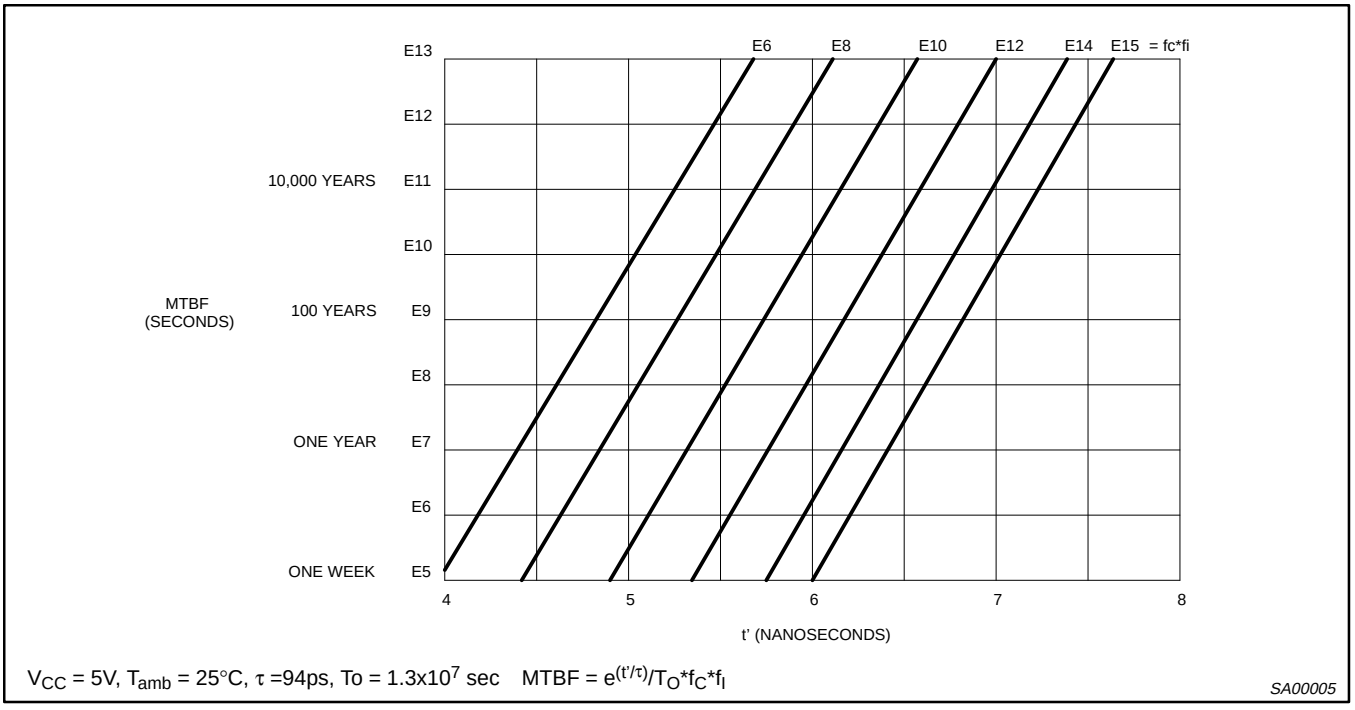


Figure 2. Mean Time Between Failures (MTBF) versus t'

TYPICAL VALUES FOR τ AND T_0 AT VARIOUS V_{CC}S AND TEMPERATURES

V_{CC}	T_{amb} = –40°C		T_{amb} = 25°C		T_{amb} = 85°C	
	τ	T_0	τ	T_0	τ	T_0
5.5V	84ps	1.0×10^6 sec	93ps	3.8×10^6 sec	89ps	1.5×10^9 sec
5.0V	84ps	2.7×10^8 sec	94ps	1.3×10^7 sec	106ps	2.2×10^6 sec
4.5V	89ps	1.0×10^9 sec	103ps	2.1×10^7 sec	115ps	4.4×10^6 sec

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	40	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–15	mA
I_{OL}	Low-level output current		20	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –15mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 20mA; V_I = V_{IL} or V_{IH}		0.35	0.5		0.5	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–75	–180	–50	–180	mA
I_{CC}	Quiescent supply current	V_{CC} = 5.5V; V_I = GND or V_{CC}		2	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.25	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40 to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	1	180	250		150		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	1	1.0 1.0	2.8 2.4	3.9 3.5	1.0 1.0	4.5 3.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn, $\overline{R}$Dn to Qn or $\overline{Q}$n	2	1.0 1.0	3.5 3.1	4.6 4.2	1.0 1.0	5.5 4.7	ns
$t_{sk(o)}$	Output skew[1, 2] CPn to Qn to $\overline{Q}$n	4			1.5		2.0	ns

NOTES:
1. | t_{PN} actual - t_{PM} actual | for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).

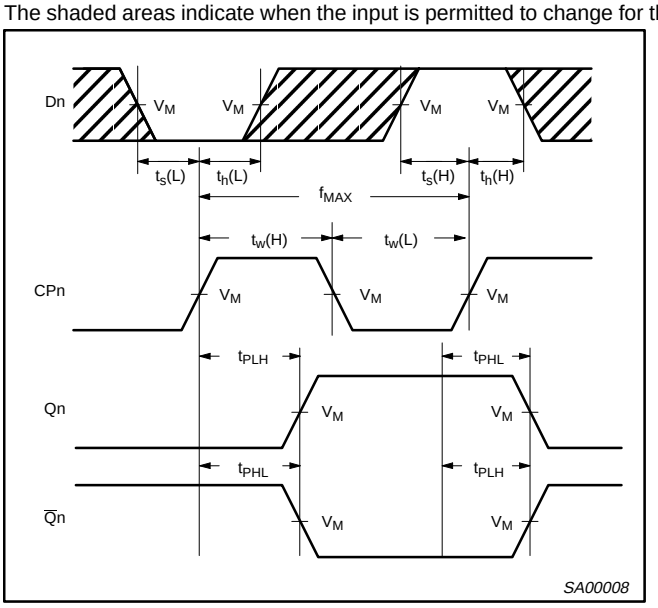
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

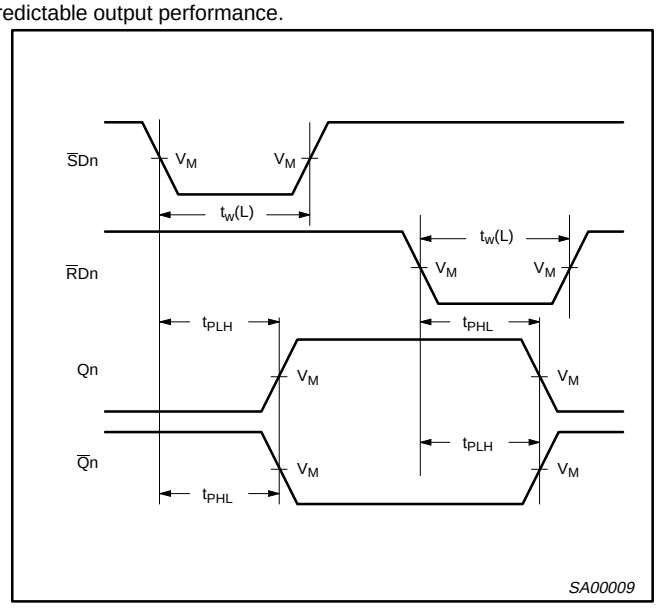
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C V_{CC} = +5.0V		T_{amb} = –40 to +85°C V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Setup time, High or Low Dn to CPn	1	2.5 2.5	1.5 1.5	2.5 2.5	ns
t_h(H) t_h(L)	Hold time, High or Low Dn to CPn	1	0 0	–1.4 –1.4	0 0	ns
t_w (H) t_w (L)	CPn pulse width, high or low	1	1.5 2.4	0.6 1.8	1.5 2.9	ns
t_w (L)	$\overline{S}$Dn or $\overline{R}$Dn pulse width, low	2	2.0	1.3	2.2	ns
t_{rec}	Recovery time $\overline{S}$Dn or $\overline{R}$Dn to CPn	3	2.4	1.3	2.8	ns

AC WAVEFORMS

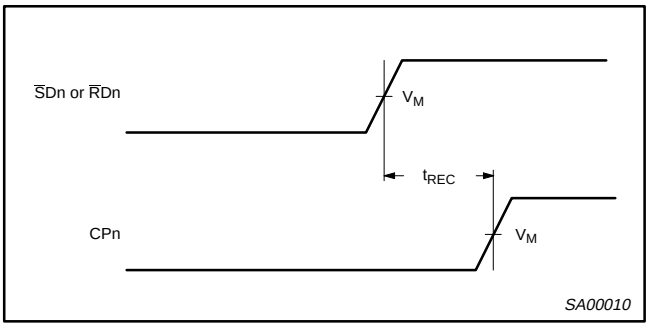
V_M = 1.5V, V_{IN} = GND to 3.0V
The shaded areas indicate when the input is permitted to change for the predictable output performance.



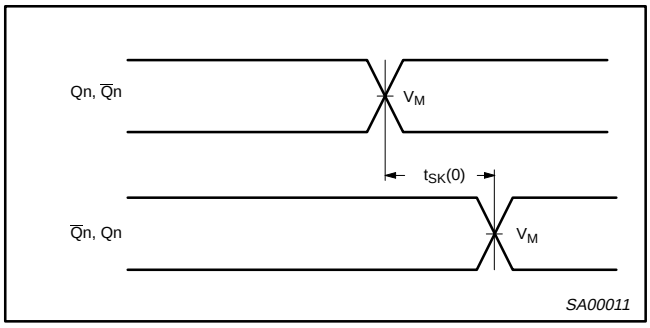
Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Time, and Clock Width



Waveform 2. Propagation Delay for Set and Reset to Output, Set and Reset Pulse Width

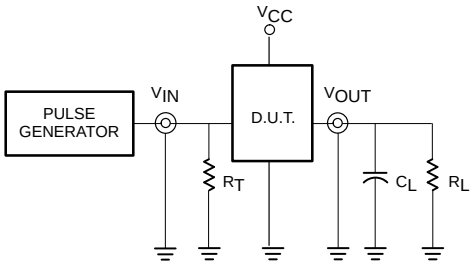


Waveform 3. Recovery Time for Set or Reset to Output

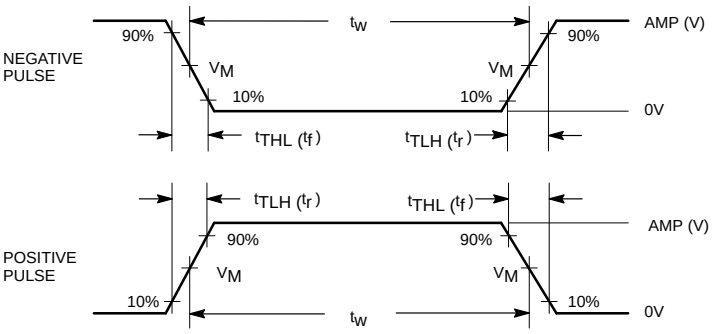


Waveform 4. Output Skew

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	amplitude	rep. rate	t_w	t_R	t_F
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00058