DATA SHEET

FTF3020-M

Full Frame CCD Image Sensor

Product specification
File under Image Sensors

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Philips
Semiconductors

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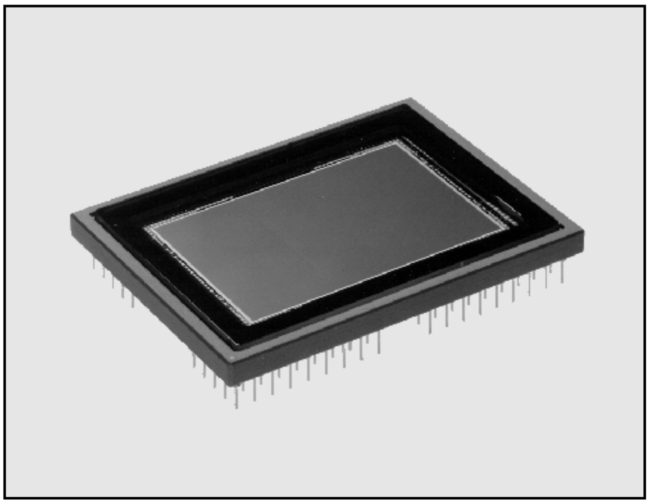
Full Frame CCD Image Sensor FTF3020-M

- **35mm film compatible image format (36 x 24 mm^2)**
- **6M active pixels (3072H x 2048V)**
- **Progressive scan**
- **Excellent anti-blooming**
- **Variable electronic shuttering**
- **Square pixel structure**
- **H and V binning**
- **100% optical fill factor**
- **High linear dynamic range (>72dB)**
- **High sensitivity**
- **Low dark current and fixed-pattern noise**
- **Low read-out noise**
- **Data rate up to 36 MHz**
- **Mirrored, split and four quadrant read-out**
- **Perfectly matched to visual spectrum**



Description

The FTF3020-M is a full frame CCD monochrome image sensor designed for professional digital photography applications, with very low dark current and a linear dynamic range of over 12 true bits at room temperature. The four low-noise output amplifiers, one at each corner of the chip, make the FTF3020-M suitable for a wide range of high-end visual light applications. With one output amplifier, a progressively scanned image can be read out at 5 frames per second. By using multiple outputs the frame rate increases accordingly. The device structure is shown in figure 1.

Device structure

Optical size:	36.864 mm (H) x 24.576 mm (V)	
Chip size:	39.148 mm (H) x 26.508 mm (V)	
Pixel size:	12 µm x 12 µm	
Active pixels:	3072 (H) x 2048 (V)	
Total no. of pixels:	3120 (H) x 2060 (V)	
Optical black pixels:	Left: 20 Right: 20	
Timing pixels:	Left: 4	Right: 4
Dummy register cells:	Left: 7	Right: 7
Optical black lines:	Bottom: 6	Top: 6

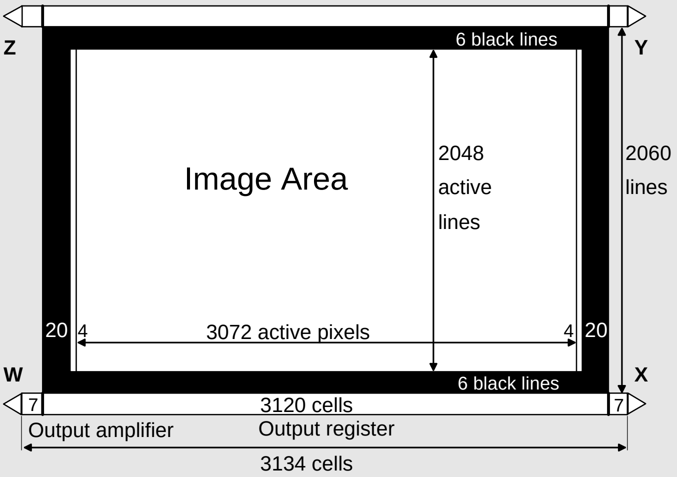


Figure 1 - Device structure

Architecture of the FTF3020-M

The optical centres of all pixels in the image section form a square grid. The charge is generated and integrated in this section. Output registers are located below and above the image section for read-out. After the integration time, the image charge is shifted one line at the time to either the upper or lower register or to both simultaneously, depending on the read-out mode. The left and the right half of each register can be controlled independently. This enables either single or multiple read-out. During vertical transport, the C3 gates separate the pixels in the register. The central C3 gates of the lower and upper registers are part of the left half of the sensor (W and Z quadrants respectively). Each register can be used for vertical binning. Each register contains a summing gate at both ends that can be used for horizontal binning (see figure 2).

IMAGE SECTION	
Image diagonal (active video only)	44.30 mm
Aspect ratio	3:2
Active image width x height	36.864 x 24.576 mm^2
Pixel width x height	12x12 μm^2
Geometric fill factor	100%
Image clock pins	16 pins (A1..A4)
Capacity of each clock phase	7.5nF per pin
Number of active lines	2048
Number of black reference lines	4 (=2x2)
Number of dummy black lines	8 (=2x4)
Total number of lines	2060
Number of active pixels per line	3072
Number of overscan (timing) pixels per line	8 (2x4)
Number of black reference pixels per line	40 (2x20)
Total number of pixels per line	3120

OUTPUT REGISTERS	
Output buffers on each corner	Three-stage source follower
Number of registers	2
Number of dummy cells per register	14 (2x7)
Number of register cells per register	3134 (3120+14)
Output register horizontal transport clock pins	6 pins per register (C1..C3)
Capacity of each C-clock phase	200 pF per pin
Overlap capacity between neighbouring C-clocks	40pF
Output register Summing Gates	4 pins (SG)
Capacity of each SG	15pF
Reset Gate clock phases	4 pins (RG)
Capacity of each RG	15pF

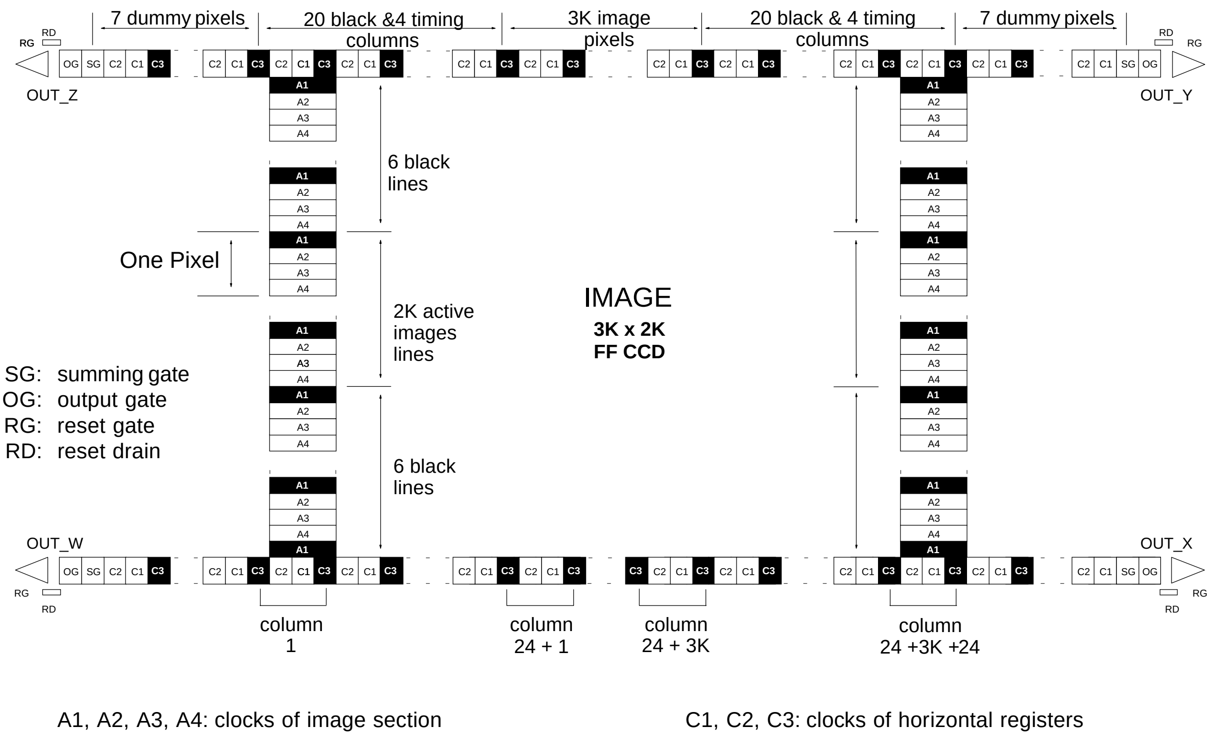


Figure 2 - Detailed internal structure

Specifications

ABSOLUTE MAXIMUM RATINGS[1]	MIN.	MAX.	UNIT
GENERAL:			
storage temperature	-55	+80	°C
ambient temperature during operation	-40	+60	°C
voltage between any two gates	-20	+20	V
DC current through any clock phase (absolute value)	-0.2	+2.0	µA
OUT current (no short circuit protection)	0	10	mA
VOLTAGES IN RELATION TO VPS:			
VNS, SFD, RD	-0.5	+30	V
VCS, SFS	-8	+5	V
all other pins	-5	+25	V
VOLTAGES IN RELATION TO VNS:			
SFD, RD	-15	+0.5	V
VCS, SFS, VPS	-30	+0.5	V
all other pins	-30	+0.5	V

DC CONDITIONS[2]		MIN. [V]	TYPICAL [V]	MAX. [V]	MAX. [mA]
VNS[3]	N substrate	18	24	28	15
VPS	P substrate	1	3	7	15
SFD	Source Follower Drain	16	20	24	4.5
SFS	Source Follower Source	0	0	0	1
VCS	Current Source	-5	0	3	-
OG	Output Gate	4	6.5	8	-
RD	Reset Drain	13	15.5	18	-

AC CLOCK LEVEL CONDITIONS[2]	MIN.	TYPICAL	MAX.	UNIT
IMAGE CLOCKS:				
A-clock amplitude during integration and hold	8	10		V
A-clock amplitude during vertical transport (duty cycle=5/8)[4]	10	14		V
A-clock low level		0		V
Charge Reset (CR) level on A-clock[5]	-5	-5		V
OUTPUT REGISTER CLOCKS:				
C-clock amplitude (duty cycle during hor. transport = 3/6)	4.75	5	5.25	V
C-clock low level	2	3.5		V
Summing Gate (SG) amplitude		10	10	V
Summing Gate (SG) low level		3.5		V
OTHER CLOCKS:				
Reset Gate (RG) amplitude	5	10	10	V
Reset Gate (RG) low level		3		V
Charge Reset (CR) pulse on Nsub[5]	0	10	10	V

[1] During Charge Reset it is allowed to exceed maximum rating levels (see note [5]).

[2] All voltages in relation to SFS.

[3] To set the VNS voltage for optimal Vertical Anti-Blooming (VAB), it should be adjustable between minimum and maximum values.

[4] Three-level clock is preferred for maximum charge; the swing during vertical transport should be 4V higher than the voltage during integration. A two level clock (typically 10V) can be used if a lower maximum charge handling capacity is allowed.

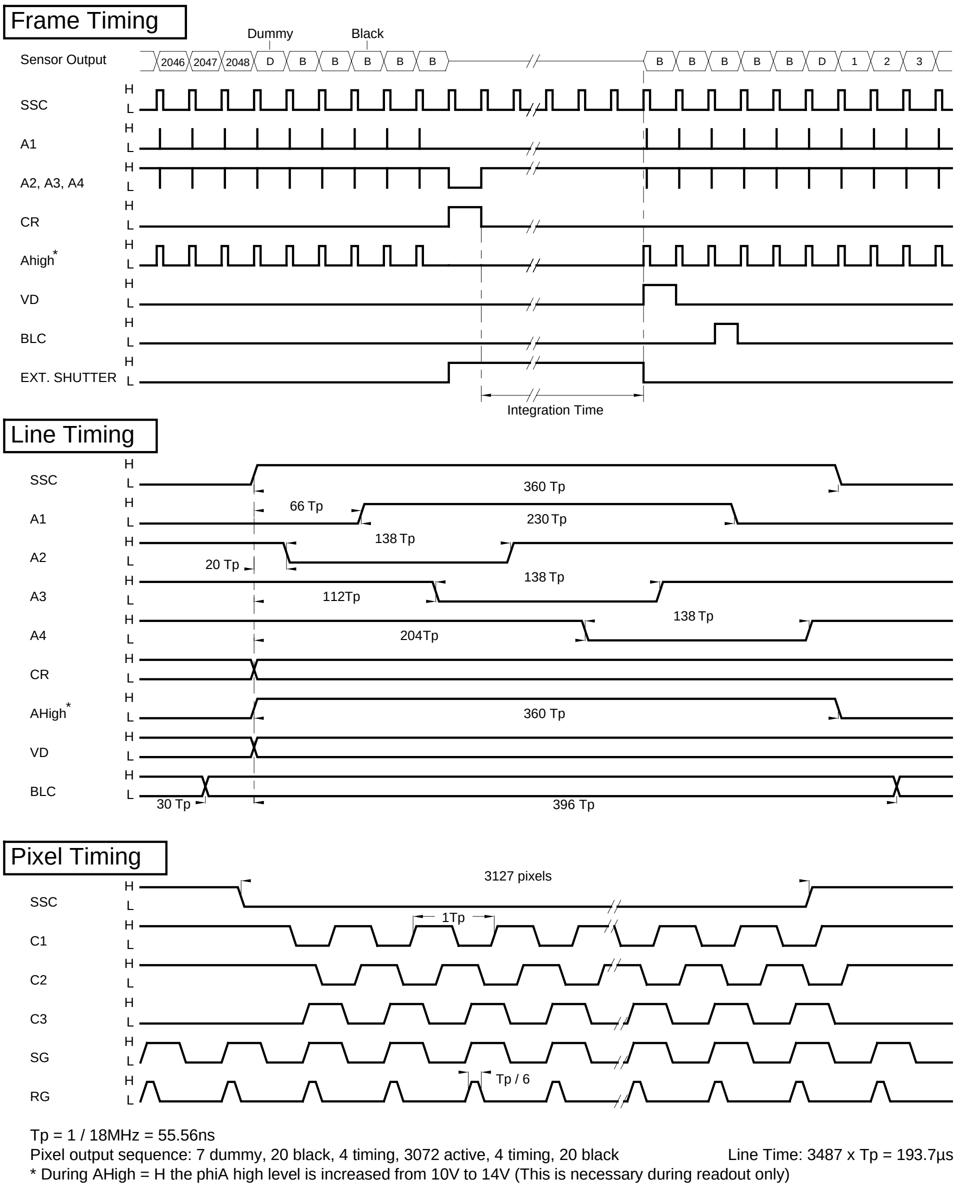
[5] Charge Reset can be achieved in two ways:
- The typical A-clock low level is applied to all image clocks; for proper CR, an additional Charge Reset pulse on VNS is required (preferred).
- The typical CR level is applied to all image clocks simultaneously.

Timing diagrams (for default operation)

AC CHARACTERISTICS		MIN.	TYPICAL	MAX.	UNIT
Horizontal frequency (1/Tp) [1]			18	36	MHz
Vertical frequency			50	100	kHz
Charge Reset (CR) time		10	193.7		µs
Rise and fall times:	image clocks (A)	10	20		ns
	register clocks (C) [2]	3	5	1/6 Tp	ns
	summing gate (SG)	3	5	1/6 Tp	ns
	reset gate (RG)	3	5	1/6 Tp	ns

[1] Tp = 1 clock period

[2] Duty cycle = 50% and phase shift of the C clocks is 120 degrees.



Tp = 1 / 18MHz = 55.56ns

Pixel output sequence: 7 dummy, 20 black, 4 timing, 3072 active, 4 timing, 20 black

Line Time: 3487 x Tp = 193.7µs

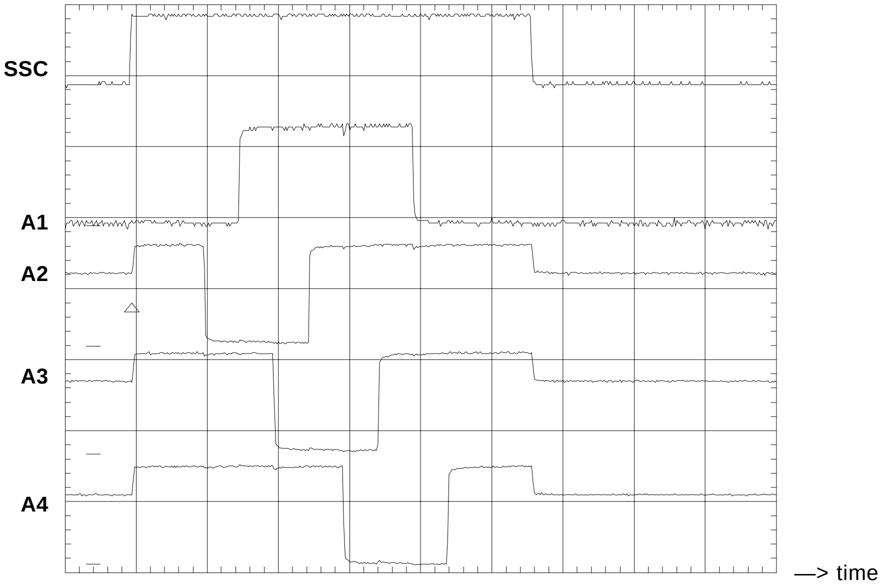
* During AHigh = H the phiA high level is increased from 10V to 14V (This is necessary during readout only)

VD: Frame pulse
CR: Charge Reset
BLC: Black Level Clamp
A1 to A4: Vertical image clocks

C1 to C3: Horizontal register clocks
SSC: Start-Stop C-clocks
SG: Summing gate
RG: Reset gate

Figure 3 - Timing diagrams

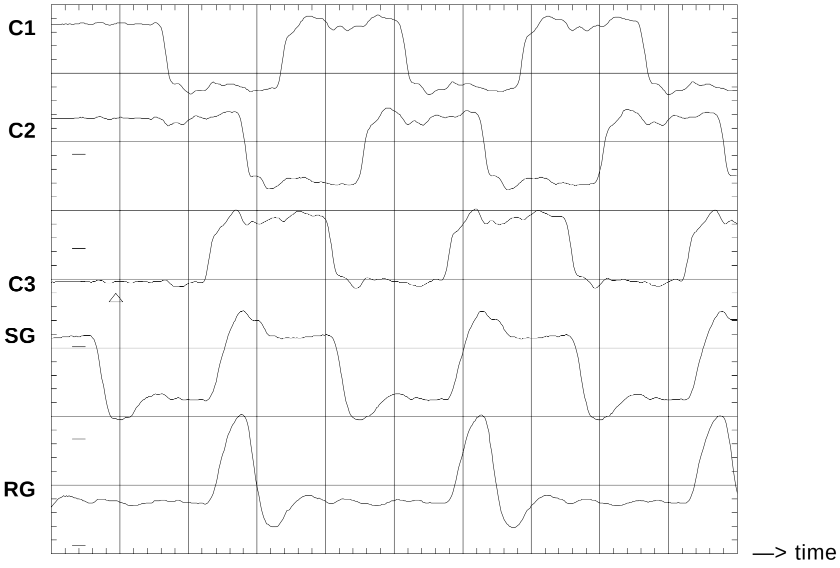
Line timing



Y / Div. : 10V (A1, A2, A3, A 4); 5V (SSC)

Figure 4 - Vertical readout

Pixel timing



Y / Div. : 5V (C1, C2, C3); 10V (SG, RG)

Figure 5 - Start horizontal readout

Performance

The test conditions for the performance characteristics are as follows:

- All values are measured using typical operating conditions.
- VNS is adjusted as low as possible while maintaining proper Vertical Anti-Blooming.
- Sensor temperature = 60°C (333K).
- Horizontal transport frequency = 18MHz.
- Vertical transport frequency = 50kHz (unless specified otherwise).
- Integration time = 10ms (unless specified otherwise).
- The light source is a lamp of 3200K in conjunction with neutral density filters and a 1.7mm thick BG40 infrared cut-off filter. For Linear Operation measurements, a temperature conversion filter (Melles Griot type no. 03FCG261, -120 mired, thickness: 2.5mm) is applied.

LINEAR OPERATION	MIN.	TYPICAL	MAX.	UNIT
Linear dynamic range [1]	4200:1(12bit)			
Charge Transfer Efficiency [2] vertical		0.999995		
Charge Transfer Efficiency [2] horizontal		0.999999		
Image lag			0	%
Resolution (MTF) @ 42 lp/mm	65			%
Responsivity	180	250		kel/lux·s
Quantum efficiency @ 530 nm	20	26		%
Low Pass Shading [3]		2.0	5	%
Random Non-Uniformity (RNU) [4]		0.3	5	%
VNS required for good Vertical Anti-Blooming (VAB)	18	24	28	V
Power dissipation at 2.5 frames/s		610		mW

[1] Linear dynamic range is defined as the ratio of Q_{lin} to read-out noise (the latter reduced by Correlated Double Sampling).

[2] Charge Transfer Efficiency values are tested by evaluation and expressed as the value per gate transfer.

[3] Low Pass Shading is defined as the ratio of the one-σ value of an 8x8 pixels blurred image (low-pass) to the mean signal value.

[4] RNU is defined as the ratio of the one-σ value of the highpass image to the mean signal value at nominal light.

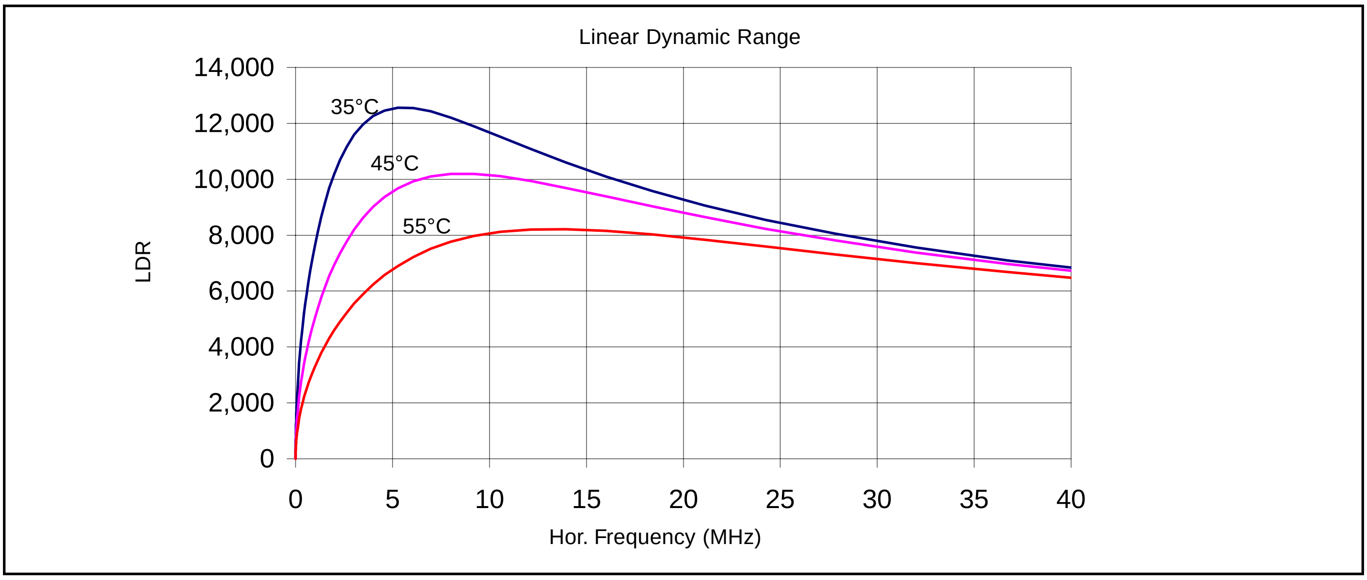


Figure 6 - Typical Linear dynamic range vs. horizontal read-out frequency and sensor temperature

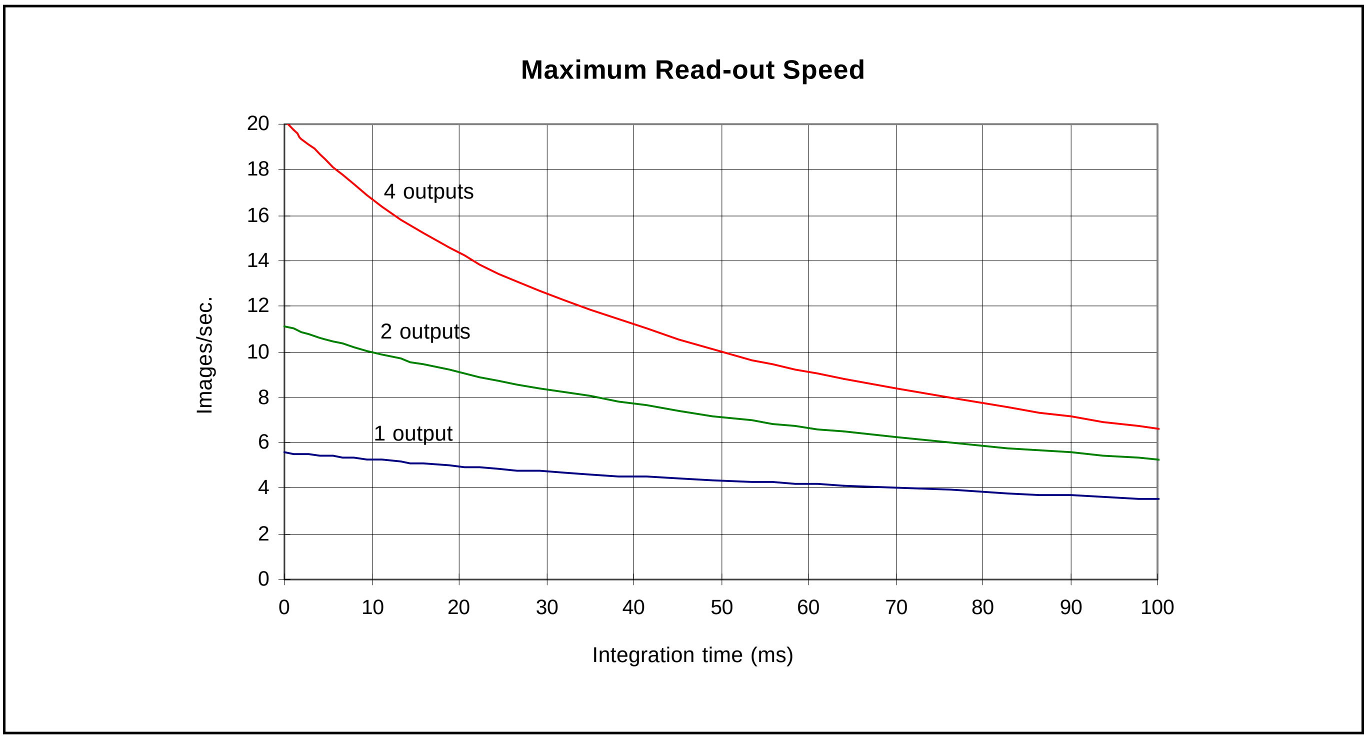


Figure 7 - Maximum number of images/second versus integration time

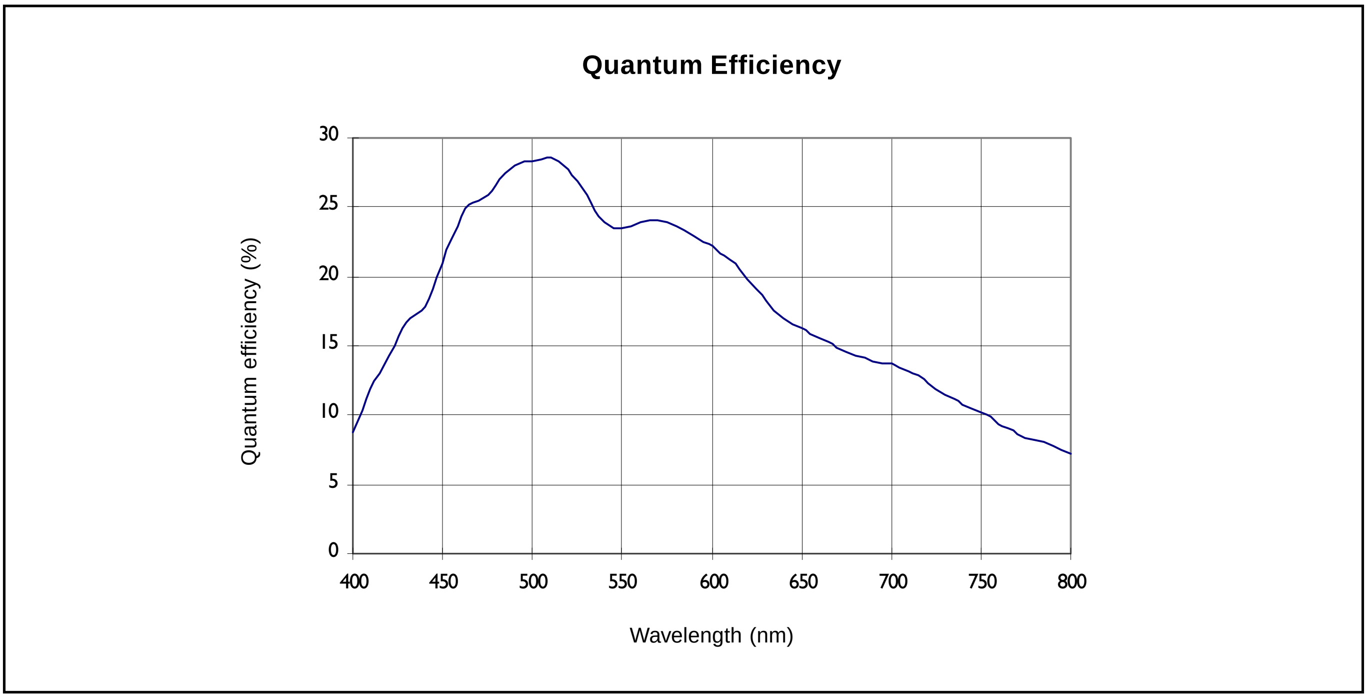


Figure 8 - Quantum efficiency versus wavelength

LINEAR/SATURATION	MIN.	TYPICAL	MAX.	UNIT
Full-well capacity saturation level (Qmax) [1]	240	500	600	kel.
Full-well capacity shading (Qmax, shading) [2]		10	50	%
Full-well capacity linear operation (Qlin) [3]	180	350		kel.
Charge handling capacity [4]		600		kel.
Overexposure [5] handling		200		x Qmax level

[1] Qmax is determined from the lowpass filtered image.

[2] Qmax, shading is the maximum difference of the full-well charges of all pixels, relative to Qmax.

[3] The linear full-well capacity Qlin is calculated from linearity test (see dynamic range). The evaluation test guarantees 97% linearity.

[4] Charge handling capacity is the largest charge packet that can be transported through the register and read-out through the output buffer.

[5] Overexposure over entire area while maintaining good Vertical Anti-Blooming (VAB). It is tested by measuring the dark line.

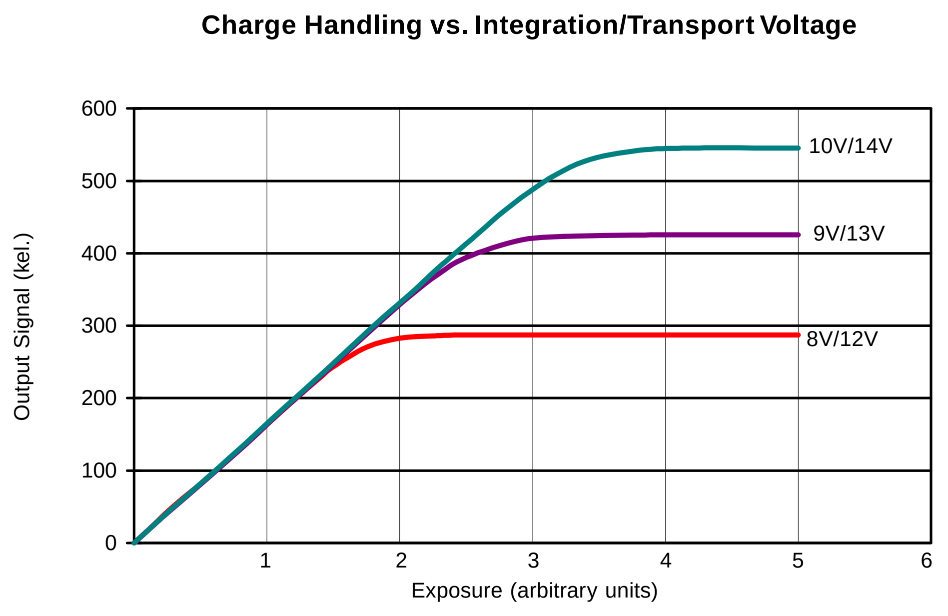


Figure 9 - Charge handling versus integration/transport voltage

OUTPUT BUFFERS	MIN.	TYPICAL	MAX.	UNIT
Conversion factor	5	7.5	10	µV/el.
Mutual conversion factor matching (ΔACF)[1]		0	2	µV/el.
Supply current		4.5		mA
Bandwidth		110		MHz
Output impedance buffer (R_{load} = 3.3kΩ, C_{load} = 2pF)		400		Ω

[1] Matching of the four outputs is specified as ΔACF with respect to reference measured at the operating point (Q_{lin}/2).

DARK CONDITION	MIN.	TYPICAL	MAX.	UNIT
Dark current level @ 30° C		20	30	pA/cm^2
Dark current level @ 60° C		0.3	0.6	nA/cm^2
Fixed Pattern Noise [1] (FPN) @ 60° C		15	25	el.
RMS readout noise @ 9MHz bandwidth after CDS		25	30	el.

[1] FPN is the one-σ value of the highpass image.

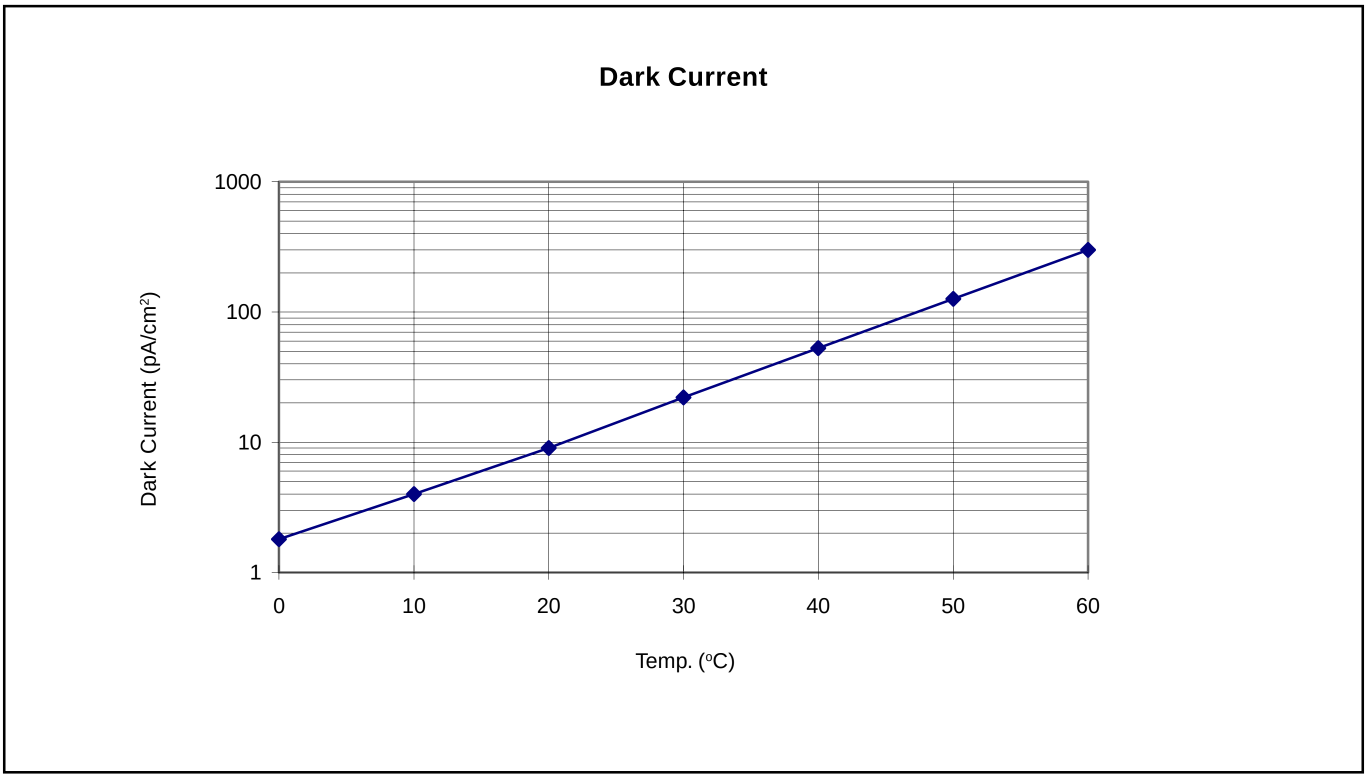


Figure 10 - Dark current versus temperature

Application information

Current handling

One of the purposes of VPS is to drain the holes that are generated during exposure of the sensor to light. Free electrons are either transported to the VRD connection and, if excessive (from over-exposure), free electrons are drained to VNS. No current should flow into any VPS connection of the sensor. During high overexposure a total current 10 to 15mA through all VPS connections together may be expected. The PNP emitter follower in the circuit diagram (figure 11) serves these current requirements.

VNS drains superfluous electrons as a result of overexposure. In other words, it only sinks current. During high overexposure a total current of 10 to 15mA through all VNS connections together may be expected. The NPN emitter follower in the circuit diagram meets these current requirements. The clamp circuit, consisting of the diode and electrolytic capacitor, enables the addition of a Charge Reset (CR) pulse on top of an otherwise stable VNS voltage. To protect the CCD, the current resulting from this pulse should be limited. This can be accomplished by designing a pulse generator with a rather high output impedance.

Decoupling of DC voltages

All DC voltages (not VNS, which has additional CR pulses as described above) should be decoupled with a 100nF decoupling capacitor. This capacitor must be mounted as close as possible to the sensor pin. Further noise reduction (by bandwidth limiting) is achieved by the resistors in the connections between the sensor and its voltage supplies. The electrons that build up the charge packets that will reach the floating diffusions only add up to a small current, which will flow through VRD. Therefore a large series resistor in the VRD connection may be used.

Outputs

To limit the on-chip power dissipation, the output buffers are designed with open source outputs. Outputs to be used should therefore be loaded with a current source or more simply with a resistance to GND. In order to prevent the output (which typically has an output impedance of about 400Ω) from bandwidth limitation as a result of capacitive loading, load the output with an emitter follower built from a high-frequency transistor. Mount the base of this transistor as close as possible to the sensor and keep the connection between the emitter and the next stage short. The CCD output buffer can easily be destroyed by ESD. By using this emitter follower, this danger is suppressed; do NOT reintroduce this danger by measuring directly on the output pin of the sensor with an oscilloscope probe. Instead, measure on the output of the emitter follower. Slew rate limitation is avoided by avoiding a too-small quiescent current in the emitter follower; about 10mA should do the job. The collector of the emitter follower should be decoupled properly to suppress the Miller effect from the base-collector capacitance.
A CCD output load resistor of 3.3kΩ typically results in a bandwidth of 110MHz. The bandwidth can be enlarged to about 130MHz by using a resistor of 2.2kΩ instead, which, however, also enlarges the on-chip power dissipation.

Device protection

The output buffers of the FTF3020-M are likely to be damaged if VPS rises above SFD or RD at any time. This danger is most realistic during power-on or power-off of the camera. The RD voltage should always be lower than the SFD voltage.

Never exceed the maximum output current. This may damage the device permanently. The maximum output current should be limited to 10mA.
Be especially aware that the output buffers of these image sensors are very sensitive to ESD damage.

Because of the fact that our CCDs are built on an n-type substrate, we are dealing with some parasitic npn transistors. To avoid activation of these transistors during switch-on and switch-off of the camera, we recommend the application diagram of figure 11.

Unused sections

To reduce power consumption the following steps can be taken. Connect unused output register pins (C1...C3, SG, OG) and unused SFS pins to zero Volts.

More information

Detailed application information is provided in the application note AN01 entitled ‘**Camera Electronics for the mK x nK CCD Image Sensor Family**’.

Device Handling

An image sensor is a MOS device which can be destroyed by electro-static discharge (ESD). Therefore, the device should be handled with care.

Always store the device with short-circuiting clamps or on conductive foam. Always switch off all electric signals when inserting or removing the sensor into or from a camera (the ESD protection in the CCD image sensor process is less effective than the ESD protection of standard CMOS circuits).

Being a high quality optical device, it is important that the cover glass remain undamaged. When handling the sensor, use fingercots.

When cleaning the glass we recommend using ethanol (or possibly water). Use of other liquids is strongly discouraged:

- if the cleaning liquid evaporates too quickly, rubbing is likely to cause ESD damage.
- the cover glass and its coating can be damaged by other liquids.

Rub the window carefully and slowly.

Dry rubbing of the window may cause electro-static charges or scratches which can destroy the device.

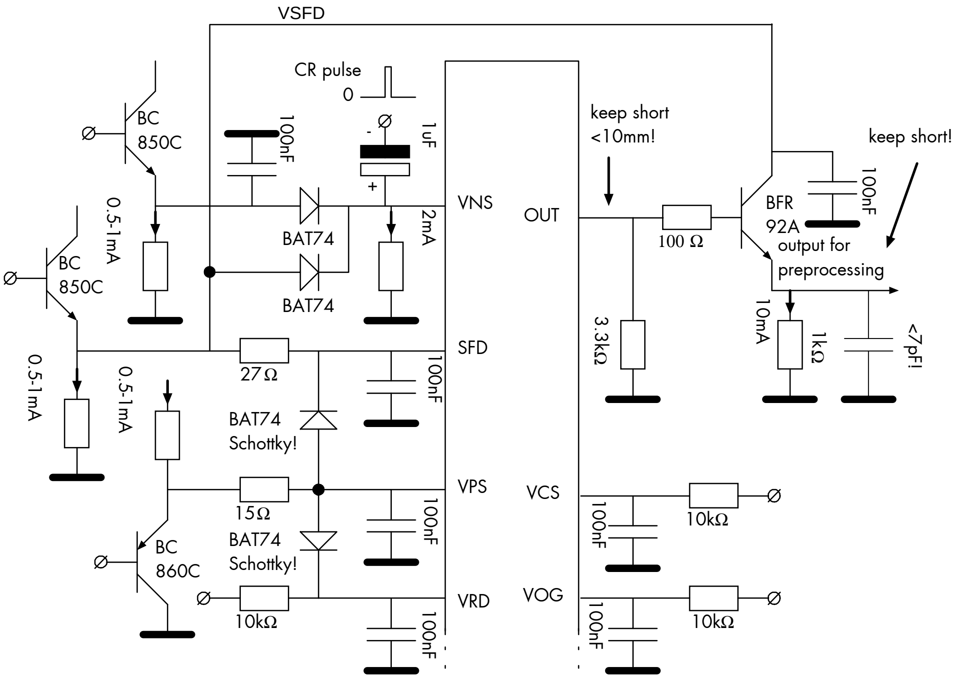


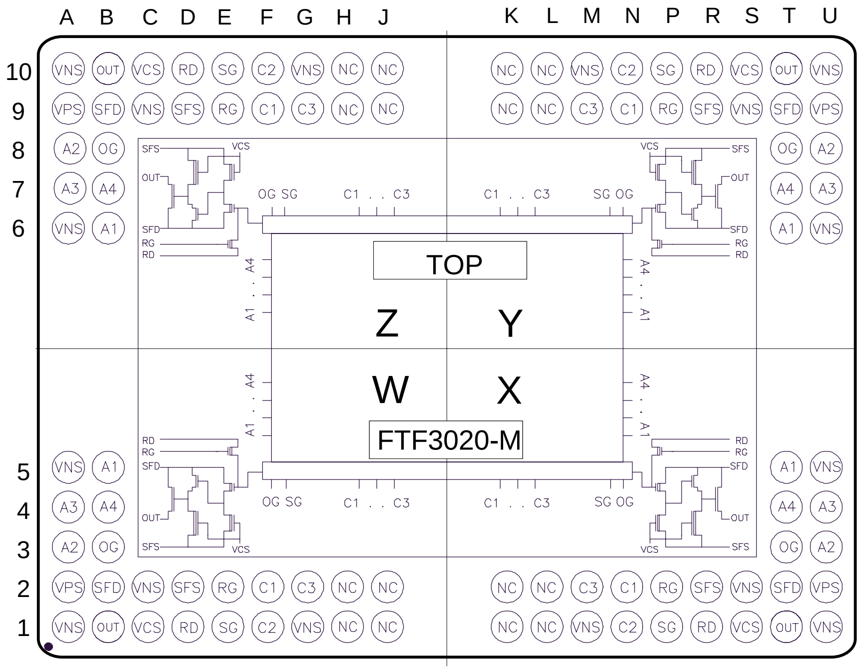
Figure 11 - Application diagram to protect the FTF3020-M

Pin configuration

The FTF3020-M is mounted in a Pin Grid Array (PGA) package with 96 pins in a 20x15 grid of 52.70 x 40.00 mm². The position of pin A1 (quadrant W) is marked with a gold dot on top of the package.

The image clock phases of quadrant W are internally connected to X, and Y is connected to Z.

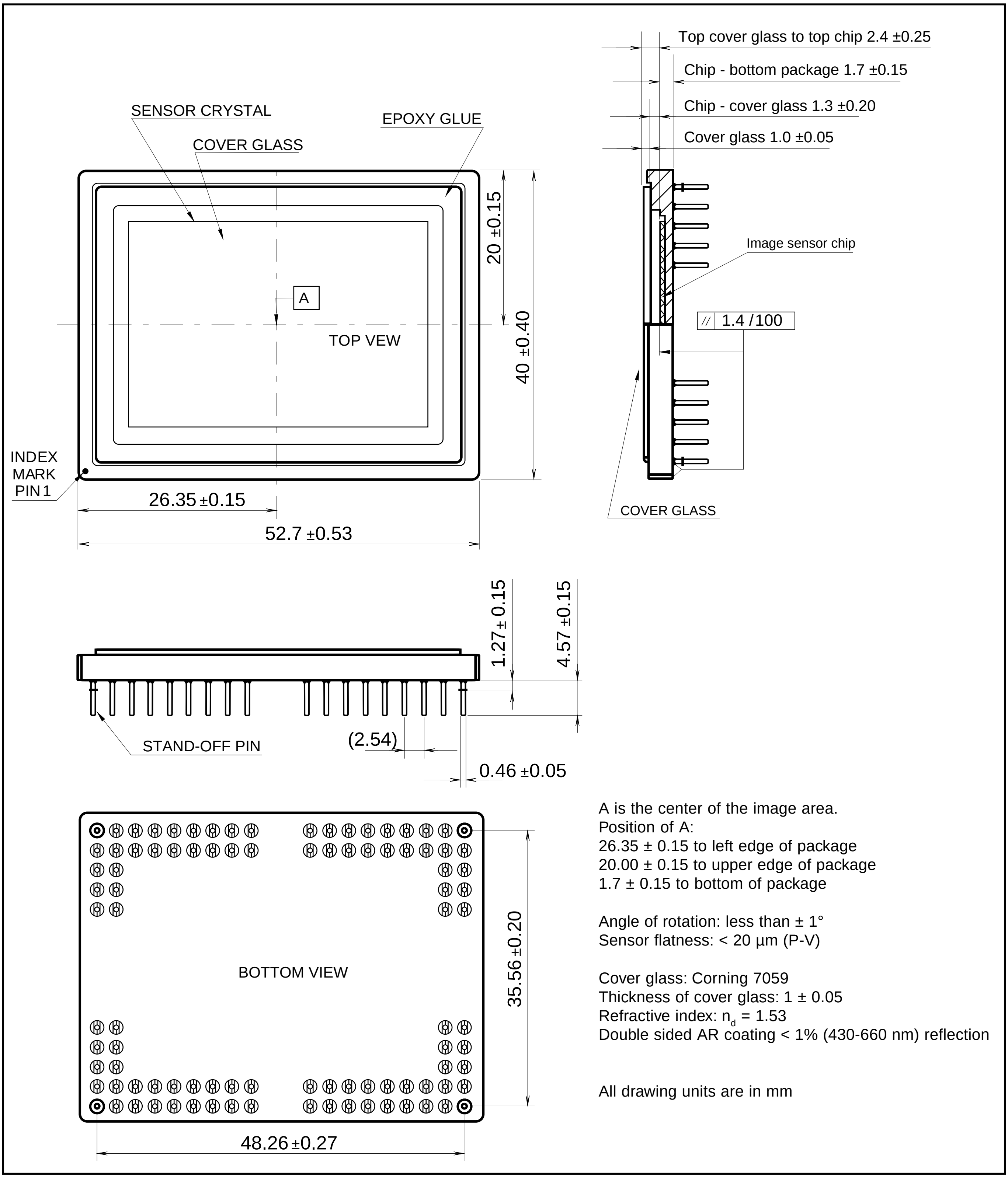
Symbol	Name	Pin # W	Pin # X	Pin # Y	Pin # Z
VNS	N substrate	A1	U1	U10	A10
VNS	N substrate	A5	U5	U6	A6
VNS	N substrate	C2	S2	S9	C9
VNS	N substrate	G1	M1	M10	G10
VPS	P substrate	A2	U2	U9	A9
SFD	Source Follower Drain	B2	T2	T9	B9
SFS	Source Follower Source	D2	R2	R9	D9
VCS	Current Source	C1	S1	S10	C10
OG	Output Gate	B3	T3	T8	B8
RD	Reset Drain	D1	R1	R10	D10
A1	Image Clock (Phase 1)	B5	T5	T6	B6
A2	Image Clock (Phase 2)	A3	U3	U8	A8
A3	Image Clock (Phase 3)	A4	U4	U7	A7
A4	Image Clock (Phase 4)	B4	T4	T7	B7
C1	Register Clock (Phase 1)	F2	N2	N9	F9
C2	Register Clock (Phase 2)	F1	N1	N10	F10
C3	Register Clock (Phase 3)	G2	M2	M9	G9
SG	Summing Gate	E1	P1	E10	P10
RG	Reset Gate	E2	P2	P9	E9
OUT	Output	B1	T1	T10	B10
NC	Not Connected	I1	K1	K10	I10
NC	Not Connected	I2	K2	K9	I9
NC	Not Connected	H1	L1	L10	H10
NC	Not Connected	H2	L2	L9	H9



DOT ON TOP OF CCD INDICATES LOCATION OF PIN 1

Figure 12 - FTF3020-M pin configuration (top view)

Package information



A is the center of the image area.
Position of A:
26.35 ± 0.15 to left edge of package
20.00 ± 0.15 to upper edge of package
1.7 ± 0.15 to bottom of package

Angle of rotation: less than ± 1°
Sensor flatness: < 20 µm (P-V)

Cover glass: Corning 7059
Thickness of cover glass: 1 ± 0.05
Refractive index: $n_d = 1.53$
Double sided AR coating < 1% (430-660 nm) reflection

All drawing units are in mm

Figure 13 - Mechanical drawing of the PGA package of the FTF3020-M

Order codes

The sensors can be ordered using the following codes:

FTF3020-M sensors		
Description	**Quality Grade**	**Order Code**
FTF3020-M/TG	Test grade	9922 157 31431
FTF3020-M/EG	Economy grade	9922 157 31451
FTF3020-M/IG	Industrial grade	9922 157 31421
FTF3020-M/HG	High grade	9922 157 31411

You can contact the Image Sensors division of Philips Semiconductors at the following address:

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