CLOCK GENERATOR FOR DESKTOP PC PLATFORMS

IDTCV104B
PRELIMINARY

FEATURES:

- **4 PLL architecture**
- **Linear frequency programming**
- **Independent frequency programming and SSC control**
- **Band-gap circuit for differential output**
- **High power-noise rejection ratio**
- **66MHz to 533MHz CPU frequency**
- **VCO frequency up to 1.1G**
- **Support index block read/write, single cycle index block read**
- **Programmable REF, 3V66, PCI, 48MHz I/O drive strength**
- **Programmable 3V66 and PCI Skew**
- **Available in SSOP package**

DESCRIPTION:

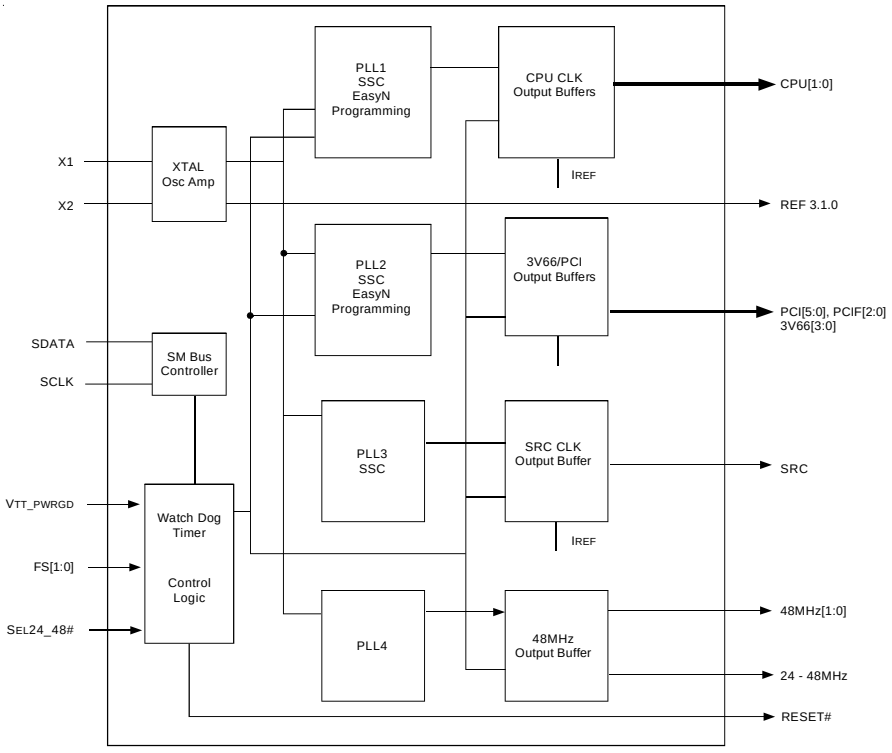
IDTCV104B is a 48 pin clock generation device for desktop PC platforms. This chip incorporates four PLLs to allow independent generation of CPU, AGP/PCI, SRC, and 48MHz clocks. The dedicated PLL for Serial ATA clock provides high accuracy frequency. This device also implements Band-gap referenced I_{REF} to reduce the impact of V_{DD} variation on differential outputs, which can provide more robust system performance.

Static PLL frequency divide error can be as low as 36 ppm, providing high accuracy output clock. Each CPU, AGP/PCI, SRC clock has its own Spread Spectrum selection.

KEY SPECIFICATION:

- **CPU/SRC CLK cycle to cycle jitter < 125ps**
- **SATA CLK cycle to cycle jitter < 125ps**
- **PCI CLK cycle to cycle jitter < 250ps**
- **Static PLL frequency divide error as low as 36ppm**

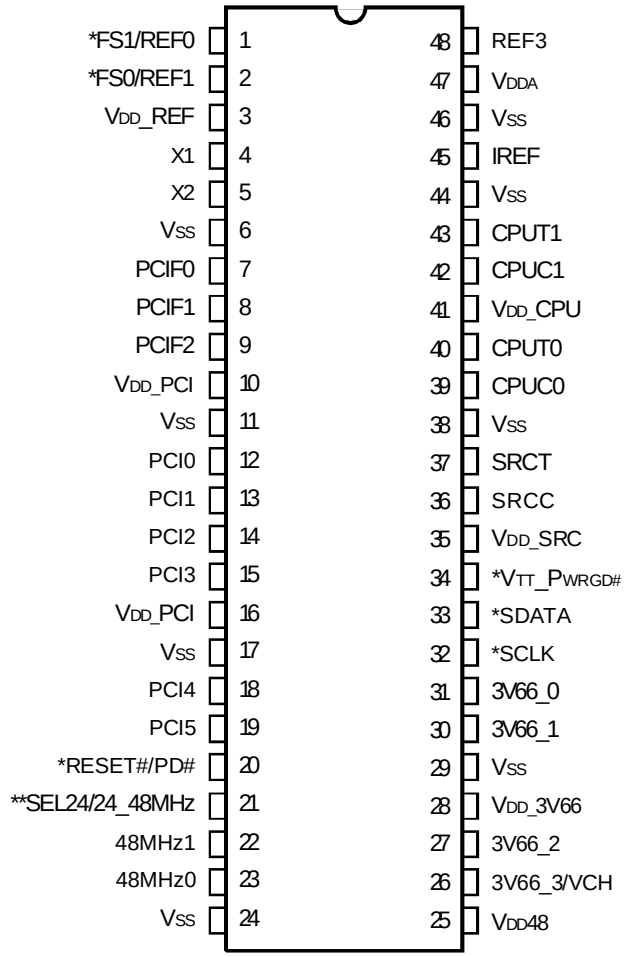
FUNCTIONAL BLOCK DIAGRAM



OUTPUT TABLE

CPU (Pair)	3V66	3V66/VCH	PCI	PCIF	REF	48MHz	24 - 48MHz	SRC (Pair)	Reset#
2	3	1	6	3	3	2	1	1	1

PIN CONFIGURATION



* = ~ 130KΩ internal pull-up.
** = ~ 130KΩ internal pull-down.

SSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Min	Max	Unit
VDDA	3.3V Core Supply Voltage		4.6	V
VDDIN	3.3V Logic Input Supply Voltage	GND - 0.5	4.6	V
TSTG	Storage Temperature	–65	+150	°C
TAMBIENT	Ambient Operating Temperature	0	+70	°C
TCASE	Case Temperature		+115	°C
ESD Prot	Input ESD Protection Human Body Model	2000		V

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

HW FREQUENCY SELECTION

FS1.0	CPU	AGP	PCI	N Resolution
00	100	66.66	33.3	0.223721591
01	200	66.66	33.3	0.447443181
10	133.33	66.66	33.3	0.298295454
11	166.67	66.66	33.3	0.397727272

SW FREQUENCY SELECTION

BS[2:0] and WBS[2:0] are band selects. Whenever there is a band switch, the user has to issue a WD soft alarm (see Byte 32 and Byte 33).
In CPU N/M programming, CPU frequency = N * resolution, N from 290 - 600.

CFS[3:0]	WDBS[2:0] or BS[2:0] = 000	WDBS[2:0] or BS[2:0] = 001	WDBS[2:0] or BS = 010	WDBS[2:0] or BS[2:0] = 011	WDBS[2:0] or BS[2:0] = 100	WDBS[2:0] or BS[2:0] = 101	WDBS[2:0] or BS[2:0] = 110	WDBS[2:0] or BS[2:0] = 111
000	100	200.01	133.34	166.65	200.01	400.01	266.66	333.3
001	100.9	201.8	135.13	167.84	66.67	401.8	267.57	334.89
010	102.91	204.93	138.11	169.83				
011	104.93	209.85	139.9	173.01				
100	110.07	215.22	141.99	175				
101	114.99	220.14	144.97	178.18				
110	119.91	225.06	147.95	180.17				
111	125.06	229.99	150.05	184.94				
N Resolution	0.223721591	0.447443181	0.298295454	0.397727272	0.447443181	0.894886363	0.894886363	0.795454544
Corresponding N	447	447	447	419	447	447	298	419

SPREAD SPECTRUM MAGNITUDE CONTROL (SMC)

SMC[2:0]	
000	Off
001	- 0.25
010	- 0.5
011	- 0.75
100	- 1
101	± 0.125
110	± 0.25
111	± 0.375

3V66-PCI/F SKEW

Skew[2:0]	
000	normal, 3V66 leads PCI 2.5ns
001	move forward 200ps
010	move forward 400ps
011	move forward 600ps
100	move backward 200ps
101	move backward 400ps
110	move backward 600ps
111	move backward 800ps

AGP/PCI FREQUENCY SELECTION

In AGP/PCI N/M programming, AGP frequency = N * 0.223721591, N from 290 - 600

AFS[2:0]	AGP	PCI	Corresponding N
000	66.67	33.33	298
001	68.68	34.34	307
010	70.7	35.35	316
011	72.71	36.35	325
100	74.5	37.25	333
101	76.51	38.26	342
110	78.53	39.26	351
111	80.54	40.27	360

AGP/PCI STRENGTH

Str[1:0]	
0, 0	1.2x
0, 1	0.7x
1, 0	0.8x
1, 1	1x

REF STRENGTH

REF Str[1:0]	
0, 0	1x
0, 1	0.8x
1, 0	1.2x
1, 1	0.7x

PIN DESCRIPTION

Pin Number	Name	Type	Description
1	FS1/REF0	I/O	Frequency select latch input 3.3V input HIGH/LOW voltage/ 14.318MHz reference clock output(1)
2	FS0/REF1	I/O	Frequency select latch input 2.5V input HIGH/LOW voltage/ 14.318MHz reference clock output(1)
3	VDD_REF	PWR	3.3V
4	X1	IN	Xtal input
5	X2	OUT	Xtal output
6	VSS	GND	GND
7	PCIF0	I/O	Frequency select latch input 3.3V input HIGH/LOW voltage/ PCI free running clock(2)
8	PCIF1	OUT	PCI free running clock
9	PCIF2	OUT	PCI free running clock
10	VDD_PCI	PWR	3.3V
11	VSS	GND	GND
12	PCI0	OUT	PCI clock
13	PCI1	OUT	PCI clock
14	PCI2	OUT	PCI clock
15	PCI3	OUT	PCI clock
16	VDD_PCI	PWR	3.3V
17	VSS	GND	GND
18	PCI4	OUT	PCI clock
19	PCI5	OUT	PCI clock
20	RESET#/PD#	OUT	Reset output signal from watchdog circuit, active LOW/ power down control input. Mode selectable through SM bus, Byte 34 bit 5, power on is RESET# mode.(1)
21	SEL24/24_48MHz	I/O	24MHz or 48MHz clock output. Frequency selected by SEL24 latch input. 1 = 24MHz, 0 = 48MHz, also can be programmed through SM bus Byte 34.(2)
22	48MHz1	OUT	48MHz clock output
23	48MHz0	OUT	48MHz clock output. Output drive strength can be doubled through SM programming. Power on is 2x.
24	VSS	GND	GND
25	VDD48	PWR	3.3V
26	3V66_3/VCH	OUT	66MHz or 48MHz clock output. Selectable by SM bus. Power on is 66MHz.
27	3V66_2	OUT	66MHz clock output
28	VDD_3V66	PWR	3.3V
29	VSS	GND	GND
30	3V66_1	OUT	66MHz clock output
31	3V66_0	OUT	66MHz clock output
32	SCLK	IN	SM bus clock(1)
33	SDATA	I/O	SM bus data(1)
34	VTT_PWRGD#	IN	Used for power on latch, active HIGH after power on becomes power down control, active LOW.(1)
35	VDD_SRC	PWR	3.3V
36	SRCC	OUT	SATA 0.7V current mode differential clock output
37	SRCT	OUT	SATA 0.7V current mode differential clock output
38	VSS	GND	GND
39	CPUC0	OUT	Hosts 0.7V current mode differential clock output
40	CPUT0	OUT	Hosts 0.7V current mode differential clock output

NOTES:
1. ~ 130KΩ internal pull-up.
2. ~ 130KΩ internal pull-down.

PIN DESCRIPTION (CONT.)

Pin Number	Name	Type	Description
41	V_{DD}_CPU	PWR	3.3V
42	CPUC1	OUT	Hosts 0.7V current mode differential clock output
43	CPUT1	OUT	Hosts 0.7V current mode differential clock output
44	V_{SS}	GND	GND
45	IREF	OUT	Reference current for differential clock output
46	V_{SS}	GND	GND
47	V_{DDA}	PWR	3.3V
48	REF3	OUT	14.318 MHz reference clock output

SM BUS PROTOCOL

INDEX BLOCK WRITE PROTOCOL

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Acknowledge
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Acknowledge
20-27	8	Master	Byte count N (0 is not a valid byte count)(1)
28	1	Slave	Acknowledge
29-36	8	Master	First data byte
37	1	Slave	Acknowledge
38-45	8	Master	Second data byte
46	1	Slave	Acknowledge
			:
			Nth data byte
			Stop

NOTE:
1. Bit [21:27] = byte count.
   Bit 20 = 1, bit [21:27] will be stored into I2C table, Byte 8. SM Bus Byte 8 is read byte count register, power on default is 0FH.
   Bit 20 = 0, normal SM bus operation.

INDEX BLOCK READ PROTOCOL

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Acknowledge
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Acknowledge
20	1	Master	Repeated start
21-28	8	Master	D3h
29	1	Slave	Acknowledge
30-37	8	Slave	Byte count, N, I2C table byte 8 value. Power on default is 0FH[15].
38	1	Master	Acknowledge
39-46	8	Slave	Offset data byte, specified by bit 11-18
47	1	Master	Acknowledge
48-55	8	Slave	Offset + 1 data byte
			:
		Slave	Offset + N-2
		Master	Acknowledge
		Slave	Offset + N-1
			Not acknowledge
			Stop

ONECYCLE™ INDEX BLOCK READ

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Acknowledge
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Acknowledge
20-27	8	Master	1xxxxxxx. Bit[20] = 1, followed with byte count, which will be stored into I2C table byte 8.
28	1	Slave	Acknowledge
29	1	Master	Repeated start
30-37	8	Master	D3h
38	1	Slave	Acknowledge
39-46	8	Slave	Byte count, N, I2C table byte 8 value. Power on default is 0FH[15].
47	1	Master	Acknowledge
48-55	8	Slave	Offset data byte, specified by bit[11:18]
56	1	Master	Acknowledge
57-64	8	Slave	Offset + 1 data byte
			:
		Slave	Offset + N-2
		Master	Acknowledge
		Slave	Offset + N-1
			Not acknowledge
			Stop

BYTE WRITE METHODS:

- **Setting bit[11:18] = starting address, bit [20:27] = 01H.**

BYTE READ METHODS (CHOSE ONE):

- **Use IDT OneCycle Index Block Read, bit[20:27] = 10000001. Notice that byte count register (byte 8) will be changed to 0IH.**
- **Use Index Block Write protocol to change byte count (byte 8) to 1. After that, use Index Block Read.**

TO CHANGE BYTE 8 VALUE:

- **Use IDT OneCycle Index Block Read, as above**
- **Use Index Block Write protocol to change byte 8 value.**

BYTE 0: DUMMY BYTE

BYTE 1

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	Reserve					0
6	Reserve					0
5	SS_EN	Spread spectrum enable	On	Off	RW	1
4	Reserve					0
3	SRCT, SRCC	Output enable	Tristate	Enable	RW	1
2	Reserve					1
1	CPUT1, CPUC1	Output enable	Tristate	Enable	RW	1
0	CPUT0, CPUC0	Output enable	Tristate	Enable	RW	1

BYTE 2

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	SRCT	SRCT Powerdown drive mode	Driven in power down	Tristate in power down	RW	0
6	Reserve					0
5	CPUT1, 0	CPUT Powerdown drive mode	Driven in power down	Tristate in power down	RW	0
4	Reserve					0
3	3V66_2	Output enable	Tristate	Enable	RW	1
2	Reserve					1
1	Reserve					1
0	Reserve					1

BYTE 3

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	Reserve					0
6	Reserve				RW	1
5	PCI5	Output enable	Tristate	Enable	RW	1
4	PCI4	Output enable	Tristate	Enable	RW	1
3	PCI3	Output enable	Tristate	Enable	RW	1
2	PCI2	Output enable	Tristate	Enable	RW	1
1	PCI1	Output enable	Tristate	Enable	RW	0
0	PCI0	Output enable	Tristate	Enable	RW	1

BYTE 4

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	48MHz0	Drive strength	2 * DRIVE	Normal	RW	0
6	SRCFS0	SRC frequency select	100MHz	200MHz	RW	0
5	Reserve				RW	1
4	3V66_1	Output enable	Tristate	Enable	RW	1
3	3V66_0	Output enable	Tristate	Enable	RW	1
2	PCIF2	Output enable	Tristate	Enable	RW	1
1	PCIF1	Output enable	Tristate	Enable	RW	1
0	PCIF0	Output enable	Tristate	Enable	RW	1

BYTE 5

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	3V66_3/VCH	3V66_3/VCH mode select	3V66 mode, 66MHz	VCH mode, 48MHz	RW	0
6	Reserve					0
5	Reserve					0
4	3V66_3/VCH	Output enable	Tristate	Enable	RW	1
3	Reserve					0
2	Reserve					0
1	Reserve					0
0	Reserve					0

BYTE 6: DUMMY BYTE

BYTE 7

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	RID3					x
6	RID2					x
5	RID1					x
4	RID0					x
3	VID3					0
2	VID2					1
1	VID1					0
0	VID0					1

BYTE 8 (READ BYTE COUNT REGISTER)

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	Reserve					0
6	BC6	See note 1				0
5	BC5					0
4	BC4					0
3	BC3					1
2	BC2					0
1	BC1					0
0	BC0					1

NOTE:
1. Can be written by index block write or OneCycle block read. See SM BUS PROTOCOL tables.

BYTES 9-20: DUMMY BYTES

BYTE 21

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	PCIFStr1	AGP/PCI STRENGTH table				1
6	PCIFStr0	AGP/PCI STRENGTH table				1
5	Reserve					1
4	Reserve					1
3	Reserve					1
2	Reserve					1
1	3V66Str1	AGP/PCI STRENGTH table				1
0	3V66Str0	AGP/PCI STRENGTH table				1

BYTE 22

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	REFStr1	REF STRENGTH table				1
6	REFStr0	REF STRENGTH table				0
5	PCIStrC1	PCI[7:5] strength control, AGP/PCI STRENGTH table				1
4	PCIStrC0	PCI[7:5] strength control, AGP/PCI STRENGTH table				1
3	PCIStrB1	PCI[4:2] strength control, AGP/PCI STRENGTH table				1
2	PCIStrB0	PCI[4:2] strength control, AGP/PCI STRENGTH table				1
1	PCIStrA1	PCI[1:0] strength control, AGP/PCI STRENGTH table				1
0	PCIStrA0	PCI[1:0] strength control, AGP/PCI STRENGTH table				1

BYTE 23

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	48MHz0	Output enable	Tristate	Enable	RW	1
6	24_48MHz	Output enable	Tristate	Enable	RW	1
5	REF1	Output enable	Tristate	Enable	RW	1
4	REF0	Output enable	Tristate	Enable	RW	1
3	Reserve					1
2	48MHz1	Output enable	Tristate	Enable	RW	1
1	REF3	Output enable	Tristate	Enable	RW	1
0	Reserve					0

BYTE 24

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	WDHRB	WD hard alarm status read back			R	
6	WDSRB	WD soft alarm status read back			R	
5						
4						
3						
2						0
1	FSR1	HW FS1 read back			R	HW FS1
0	FSR0	HW FS0 read back			R	HW FS0

BYTE 25: CPU PLL CONTROL

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	CPU frequency band source select	0 = selected by HW latched FS[1:0], CFS[2:0] 1 = selected by BS[2:0], CFS[2:0]	HW	SW	RW	0
6	BS2, Band select 2	BS[2:0] CFS[2:0] select CPU frequency(1)			RW	0
5	BS1, Band select 1	BS[2:0] CFS[2:0] select CPU frequency(1)			RW	0
4	BS0, Band select 0	BS[2:0] CFS[2:0] select CPU frequency(1)			RW	0
3	CFS2	BS[2:0] CFS[2:0] select CPU frequency(1)			RW	0
2	CFS1	BS[2:0] CFS[2:0] select CPU frequency(1)			RW	0
1	CFS0	BS[2:0] CFS[2:0] select CPU frequency(1)			RW	0
0	CPU N Programming Enable	CPU N Programming Enable	Disable	Enable	RW	0

NOTES:
1. See SW FREQUENCY SELECTION table.

BYTE 26: CPU PLL CONTROL

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	WDBS2	At the event of WD hard alarm time out, If Byte 32 bit 7 = 1, CPU frequency is selected by WDBS[2:0] WDCFS[2:0](1)			RW	1
6	WDBS1				RW	0
5	WDBS0				RW	0
4	CSMC2	CPU SMC2, SMC table			RW	0
3	CSMC1	CPU SMC1, SMC table			RW	1
2	CSMC0	CPU SMC0, SMC table			RW	0
1	CPN9	CPU PLL N9			RW	
0	CPN8	CPU PLL N8			RW	

NOTE:
1. See SW FREQUENCY SELECTION table.

BYTE 27: CPU PLL N PROGRAMMING

In CPU N programming mode, CPU frequency = CPN[9:0] * band resolution. CPN[9:0] range is 290 - 600. CPN0 has to be written for the CPN[9:0] to be loaded into PLL N driver. See SW FREQUENCY SELECTION table.

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	CPN7	CPU PLL N7			RW	
6	CPN6	CPU PLL N6			RW	
5	CPN5	CPU PLL N5			RW	
4	CPN4	CPU PLL N4			RW	
3	CPN3	CPU PLL N3			RW	
2	CPN2	CPU PLL N2			RW	
1	CPN1	CPU PLL N1			RW	
0	CPN0	CPU PLL N0			RW	

BYTE 28: AGP/PCI PLL CONTROL

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	AFS2	See AGP/PCI FREQUENCY SELECTION table			RW	0
6	AFS1	See AGP/PCI FREQUENCY SELECTION table			RW	0
5	AFS0	See AGP/PCI FREQUENCY SELECTION table			RW	0
4	WDAFS2	AGP/PCI WD hard alarm time out frequency selection			RW	0
3	WDAFS1	AGP/PCI WD hard alarm time out frequency selection			RW	0
2	WDAFSO	AGP/PCI WD hard alarm time out frequency selection			RW	0
1	APN9	AGP/PCI PLL N9			RW	
0	APN8	AGP/PCI PLL N8			RW	

BYTE 29: AGP/PCI N PROGRAMMING

In AGP/PCI N programming mode, AGP/PCI frequency = APN[9:0] * 0.223721591. APN[9:0] range is 290 - 600. APN0 has to be written for the APN[9:0] to be loaded into PLL N divider.

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	APN7	AGP/PCI PLL N7			RW	
6	APN6	AGP/PCI PLL N6			RW	
5	APN5	AGP/PCI PLL N5			RW	
4	APN4	AGP/PCI PLL N4			RW	
3	APN3	AGP/PCI PLL N3			RW	
2	APN2	AGP/PCI PLL N2			RW	
1	APN1	AGP/PCI PLL N1			RW	
0	APN0	AGP/PCI PLL N0			RW	

BYTE 30: AGP/PCI SRC CONTROL

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	AGP/PCI N Programming Mode Enable	AGP/PCI N Programming Enable	Disable	Enable	RW	0
6	AGP/PCI Frequency Source Select	0 = fixed 66/33MHz 1 = selected by AFS[2:0](1)	66/33MHz		RW	0
5	AGP SMC 2	AGP/PCI SSC magnitude control(2)			RW	0
4	AGP SMC 1	AGP/PCI SSC magnitude control(2)			RW	1
3	AGP SMC 0	AGP/PCI SSC magnitude control(2)			RW	0
2	3V66-PCI/F skew 2	Adjust 3V66 and PCI/F skew(3)			RW	0
1	3V66-PCI/F skew 1	Adjust 3V66 and PCI/F skew(3)			RW	0
0	3V66-PCI/F skew 0	Adjust 3V66 and PCI/F skew(3)			RW	0

NOTES:
1. See AGP/PCI FREQUENCY SELECTION table.
2. See SMC table.
3. See 3V66 AND PCI/F SKEW table.

BYTE 31: WATCHDOG TIMER

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	WD Hard Alarm timer 7	Specify WD Hard Alarm time out waiting time.			RW	0
6	WD Hard Alarm timer 6	Time Out time = WD Hard Alarm timer[7:0] * 290ms			RW	0
5	WD Hard Alarm timer 5	Default is 11*290 = 3.2s			RW	0
4	WD Hard Alarm timer 4				RW	0
3	WD Hard Alarm timer 3				RW	1
2	WD Hard Alarm timer 2				RW	0
1	WD Hard Alarm timer 1				RW	1
0	WD Hard Alarm timer 0				RW	1

BYTE 32: WD SOFT RESET TIMER

WD Soft Alarm timer has to be shorter than WD Hard Alarm timer. WDE and WD Soft Alarm bits, Byte 33 bit 7 and bit 5, have to be enabled for this Soft Alarm function.

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	CPU WD Hard Alarm safe frequency mode select	0 = frequency select controlled by Byte 25 bit 7 1 = CPU frequency specified by WDBS[2:0] WDCFS[2:0]	HW/I2C	WDBS WDCFS	RW	0
6	WDCFS2	CPU WD time out safe frequency select(1)			RW	0
5	WDCFS1				RW	0
4	WDCFS0				RW	0
3	WD soft alarm timer 3	Specify WD Soft Alarm Time Out time Time Out time = WD Soft Alarm Timer[3:0]*290ms			RW	0
2	WD soft alarm timer 2				RW	0
1	WD soft alarm timer 1				RW	1
0	WD soft alarm timer 0				RW	0

NOTE:
1. See SW FREQUENCY SELECTION table.

BYTE 33: WD CONTROL

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	WDE	Watchdog enable	Disable	Enable	RW	0
6	WD FS relatch	Relatch HW FS2, 1, 0 in event of WD Hard Alarm time out	Disable	Enable	RW	0
5	WD Soft Alarm enable	WD Soft Alarm enable	Disable	Enable	RW	0
4	AGP/PCI WD Hard Alarm time out safe frequency mode select	In event of WD Hard Alarm time out 0 = AGP/PCI frequency controlled by Byte 30 bit 6 1 = AGP/PCI frequency specified by WDAFS[2:0]	HW/I2C	WDAFS	RW	0
3	SRC SMC 2	SRC SSC magnitude control(1)				1
2	SRC SMC 1	SRC SSC magnitude control(1)				0
1	SRC SMC 0	SRC SSC magnitude control(1)				1
0	Reserve					0

NOTE:
1. See SMC table.

BYTE 34

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	SW 24_48MHz control override	0 = controlled by hardware, 1 = controlled by bit 6	HW control	controlled by bit 6	RW	0
6	24_48MHz select		48MHz	24MHz	RW	0
5	Reset#/PD#	Reset#/PD# mode select	Reset#	PD#	RW	0
4						0
3						0
2						
1						
0						

CPU AND AGP CLOCK FREQUENCY SELECTION

Band switch will take effect only when WD Soft Alarm time out is issued, which means there is a RESET issued. Even if the user changed BS[2:0], if there is no WD Soft Alarm, CPU PLL still uses the old band.

CPN[9:0] and APN[9:0] will be loaded into PLL only when CPN0 and APN0 are written respectively.

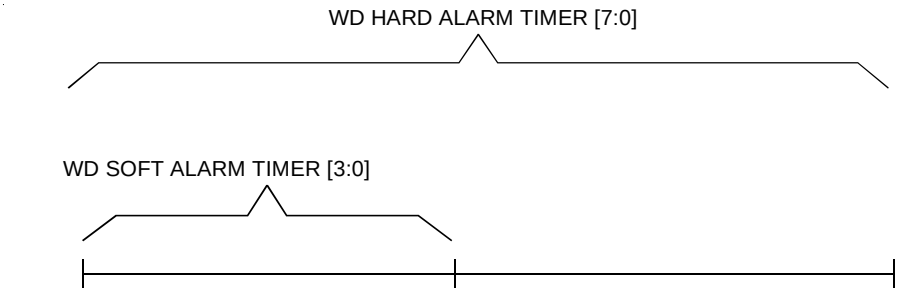
CPU FREQUENCY

Byte 25 bit 0, bit 7	CPU Frequency Selected by:
00	HW FS[1:0]
01	BS[2:0], CFS[2:0], Byte 25
10	CPN[9:0] * Band Resolution
11	CPN[9:0] * Band Resolution

AGP/PCI FREQUENCY

Byte 30 bit 7, bit 6	AGP/PCI Frequency Selected by:
00	66/33
01	AFS[2:0], Byte 28
10	APN[9:0] * 0.223721591
11	APN[9:0] * 0.223721591

WD SOFT AND HARD ALARM/TIME OUT OPERATION



WDE
- Trigger Watch Dog Circuit

WD SOFT ALARM TIME OUT
If WD Soft Alarm Enabled:
- Set WDSRB
- Issue RESET#
- Switch CPU PLL band

WD HARD ALARM TIME OUT
- Set WDHRB
- Issue RESET#
- Change CPU Frequency (see Byte 32, bit 7)
- Change AGP/PCI Frequency (see Byte 33, bit 4)
- If WD FS Relatch enabled, relatch HW FS2, FS1, FS0
- Reset Byte 30 bit 7, and Byte 25 bit 0, to 0

User only uses WD Soft Alarm when there is a band switch. It can be from HW to SW select, or in the SW select with band change. Soft Alarm Timer has to be shorter than Hard Alarm Timer.

At the event of WD Hard Alarm time out, CPU Safe return frequency is decided by two bits: Byte 32 bit 7 and Byte 25 bit 7. AGP/PCI Safe Return Frequency is decided by Byte 33 bit 4 and Byte 30 bit 6. Byte 30 bit 7, and Byte 25 bit 0, will be reset to 0.

Byte 32 bit 7, Byte 25 bit 7	CPU WD Hard Alarm Time Out Frequency Select:
00	Latched HW FS[1:0]
01	BS[2:0], CFS[2:0], Byte 25
10	WDBS[2:0], WDCFS[2:0], Byte 26 and Byte 32
11	WDBS[2:0], WDCFS[2:0], Byte 26 and Byte 32

Byte 33 bit 4, Byte 30 bit 6	AGP/PCI Hard Alarm Time Out Frequency Select:
00	66/33MHz
01	AFS[2:0], Byte 28
10	WDAFS, Byte 28
11	WDAFS, Byte 28

ELECTRICAL CHARACTERISTICS - INPUT / SUPPLY / COMMON OUTPUT PARAMETERS

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	3.3V Input HIGH Voltage	3.3V ± 5%	2	—	V_{DD} + 0.3	V
V_{IL}	3.3V Input LOW Voltage	3.3V ± 5%	V_{SS} - 0.3	—	0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	–5	—	5	µA
I_{IL1}	Input LOW Current	V_{IN} = 0V, inputs with no pull-up resistors	–5	—	—	µA
I_{IL2}	Input LOW Current	V_{IN} = 0V, inputs with pull-up resistors	–200	—	—	µA
$I_{DD3.3OP}$	Operating Supply Current	Full active, C_L = full load	—	—	400	mA
$I_{DD3.3PD}$	Powerdown Current	All differential pairs driven	—	—	70	mA
		All differential pairs tri-stated	—	—	12	
F_I	Input Frequency(2)	V_{DD} = 3.3V	—	14.31818	—	MHz
L_{PIN}	Pin Inductance(3)		—	—	7	nH
C_{IN}	Input Capacitance(3)	Logic inputs	—	—	5	pF
C_{OUT}		Output pin capacitance	—	—	6	
C_{INX}		X1 and X2 pins	—	—	5	
T_{STAB}	Clock Stabilization(3,4)	From V_{DD} power-up or de-assertion of PD# to first clock	—	—	1.8	ms
	Modulation Frequency(3)	Triangular modulation	30	—	33	KHz
	T_{DRIVE}_SRC(3)	SRC output enable after PCI_Stop# de-assertion	—	—	15	ns
	T_{DRIVE}_PD#(3)	CPU output enable after PD# de-assertion	—	—	300	us
	T_{FALL}_PD#(3)	Fall time of PD#	—	—	5	ns
	T_{RISE}_PD#(4)	Rise time of PD#	—	—	5	ns
	T_{DRIVE}_CPU_Stop#(3)	CPU output enable after CPU_Stop# de-assertion	—	—	10	us
	T_{FALL}_CPU_Stop#(3)	Fall time of PD#	—	—	5	ns
	T_{RISE}_CPU_Stop#(4)	Rise time of PD#	—	—	5	ns

NOTES:
1. Available to CV104A, CV105A, CV107A, and CV109A.
2. Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.
3. This parameter is guaranteed by design, but not 100% production tested.
4. See TIMING DIAGRAMS for timing requirements.

ELECTRICAL CHARACTERISTICS - CPU AND SRC 0.7 CURRENT MODE DIFFERENTIAL PAIR(1)

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Z_O	Current Source Output Impedance(2)	$V_O = V_X$	3000	—	—	Ω
V_{OVS}	Maximum Voltage (Overshoot)		—	—	V_H + 0.3	V
V_{UDS}	Minimum Voltage (Undershoot)		-0.3	—	—	V
V_{HIGH}	Voltage HIGH(2)	Statistical measurement on single-ended signal using	660	—	850	mV
V_{LOW}	Voltage LOW(2)	oscilloscope math function	–150	—	150	
V_{OVS}	Max Voltage(2)	Measurement on single-ended signal using absolute value	—	—	1150	mV
V_{UDS}	Min Voltage(2)		–300	—	—	
$V_{CROSS(ABS)}$	Crossing Voltage (abs)(2)		250	—	550	mV
d - V_{CROSS}	Crossing Voltage (var)(2)	Variation of crossing over all edges	—	—	140	mV
ppm	Long Accuracy(2,3)	See T_{PERIOD} Min. - Max. values	–300	—	300	ppm
T_{PERIOD}	Average Period(3)	400MHz nominal, no Intel spec	2.4993	—	2.5008	ns
		333.33MHz nominal, no Intel spec	2.9991	—	3.0009	
		266.66MHz nominal, no Intel spec	3.7489	—	3.7511	
		200MHz nominal	4.9985	—	5.0015	
		166.66MHz nominal	5.9982	—	6.0018	
		133.33MHz nominal	7.4978	—	7.5023	
		100MHz nominal	9.997	—	10.003	
T_{PERIOD}	Average Period(3)	400MHz spread, no Intel spec	2.4993	—	2.5008	ns
		333.33MHz spread, no Intel spec	2.9991	—	3.0009	
		266.66MHz spread, no Intel spec	3.7489	—	3.7511	
		200MHz spread	4.9985	—	5.0266	
		166.66MHz spread	5.9982	—	6.032	
		133.33MHz spread	7.4978	—	7.54	
		100MHz spread	9.997	—	10.0533	
t_R	Rise Time(2)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
t_F	Fall Time(2)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
d-t_R	Rise Time Variation(2)		—	—	125	ps
d-t_F	Fall Time Variation(2)		—	—	125	ps
d_{T3}	Duty Cycle(2)	Measurement from differential waveform	45	—	55	%
t_{SK3}	Skew(2)	V_T = 50%	—	—	100	ps
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(2)	Measurement from differential waveform	—	—	85	ps

NOTES:
1. SRC clock outputs run only at 100MHz or 200MHz. Specs for 133.33 and 166.66 do not apply to SRC clock pair.
2. This parameter is guaranteed by design, but not 100% production tested.
3. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - 3V66

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 30pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1,2)	See Tperiod Min. - Max. values	-300	—	300	ppm
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
T_{PERIOD}	Clock Period(2)	66MHz output nominal	14.9955	—	15.0045	ns
		66MHz output spread	14.9955	—	15.0799	
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising/Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.4V, V_{OH} = 2.4V	0.5	—	2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.4V, V_{OH} = 2.4V	0.5	—	2	ns
t_{SK1}	Skew(1)	V_T = 1.5V	—	—	250	ps
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter(1)	V_T = 1.5V, 3V66	—	—	250	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - PCICLK / PCICLK_F

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 30pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1,2)	See Tperiod Min. - Max. values	—	—	300	ppm
T_{PERIOD}	Clock Period(2)	33.33MHz output nominal	29.991	—	30.009	ns
		33.33MHz output spread	29.991	—	30.1598	
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising edge rate	1	—	4	V/ns
	Edge Rate(1)	Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.4V, V_{OH} = 2.4V	0.5	—	2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.4V, V_{OH} = 2.4V	0.5	—	2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
t_{SK1}	Skew(1)	V_T = 1.5V	—	—	500	ps
$t_{JCYC-CYC}$	Jitter(1)	V_T = 1.5V	—	—	250	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS, 48MHZ, USB AND VCH

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1,2)	See Tperiod Min. - Max. values	—	—	300	ppm
TPERIOD	Clock Period(2)	48MHz output nominal	20.8271	—	20.8396	ns
VOH	Output HIGH Voltage	IOH = -1mA	2.4	—	—	V
VOL	Output LOW Voltage	IOL = 1mA	—	—	0.55	V
IOH	Output HIGH Current	VOH at Min. = 1V	-33	—	—	mA
		VOH at Max. = 3.135V	—	—	-33	
IOL	Output LOW Current	VOL at Min. = 1.95V	30	—	—	mA
		VOL at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising edge rate	1	—	2	V/ns
	Edge Rate(1)	Falling edge rate	1	—	2	V/ns
tR1	Rise Time(1)	VOL = 0.4V, VOH = 2.4V	1	—	2	ns
tF1	Fall Time(1)	VOL = 0.4V, VOH = 2.4V	1	—	2	ns
dT1	Duty Cycle(1)	VT = 1.5V	45	—	55	%
tJCYC-CYC	Jitter(1)		—	—	350	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS, DOT 48MHZ

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1,2)	See Tperiod Min. - Max. values	—	—	300	ppm
TPERIOD	Clock Period(2)	48MHz output nominal	20.8271	—	20.8396	ns
VOH	Output HIGH Voltage	IOH = -1mA	2.4	—	—	V
VOL	Output LOW Voltage	IOL = 1mA	—	—	0.55	V
IOH	Output HIGH Current	VOH at Min. = 1V	-33	—	—	mA
		VOH at Max. = 3.135V	—	—	-33	
IOL	Output LOW Current	VOL at Min. = 1.95V	30	—	—	mA
		VOL at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising edge rate	2	—	4	V/ns
	Edge Rate(1)	Falling edge rate	2	—	4	V/ns
tR1	Rise Time(1)	VOL = 0.4V, VOH = 2.4V	0.5	—	1	ns
tF1	Fall Time(1)	VOL = 0.4V, VOH = 2.4V	0.5	—	1	ns
dT1	Duty Cycle(1)	VT = 1.5V	45	—	55	%
tJCYC-CYC	Jitter(1)		—	—	350	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

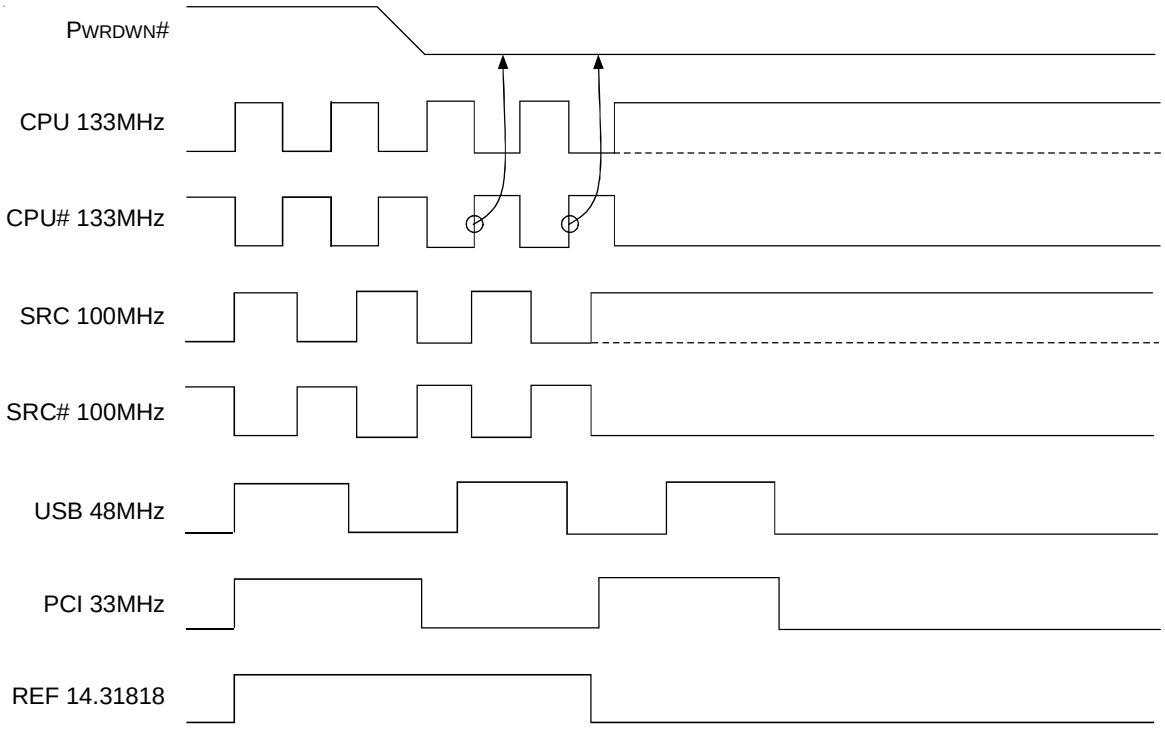
PD#, POWER DOWN

PD# is an asynchronous active low input used to shut off all clocks cleanly prior to clock power. When PD# is asserted low all clocks will be driven low before turning off the VCO. In PD# de-assertion all clocks will start without glitches.

PWRDWN#	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	3V66	REF
1	Normal	Normal	Normal	Normal	33MHz	48MHz	66MHz	14.318MHz
0	IREF * 2 or float	Float	IREF * 2 or float	Float	Low	Low	Low	Low

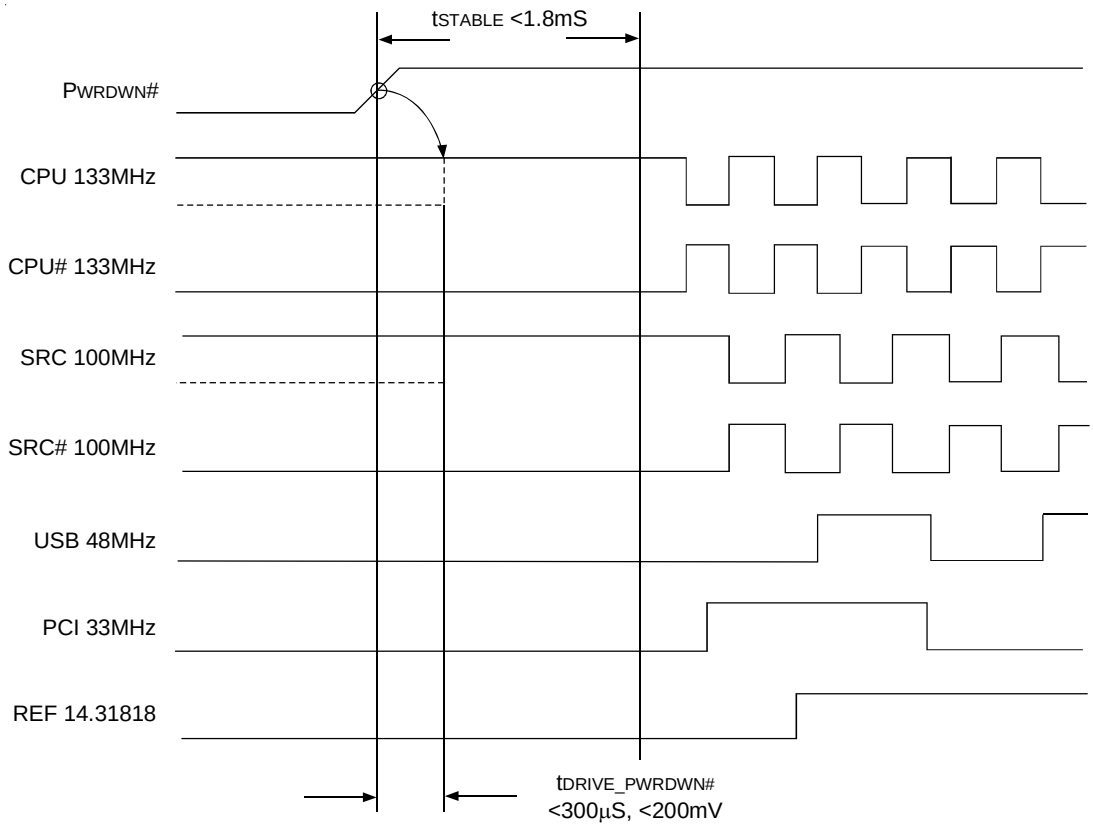
PD# ASSERTION

PD# should be sampled low by two consecutive CPU# rising edges before stopping clocks. All single-ended clocks will be held low on their next high to low transition. All differential clocks will be held high on the next high to low transition of the complimentary clock. If the control register determining to drive mode is set to 'tri-state', the differential pair will be stopped in tri-state mode, undriven. When the drive mode but corresponding to the CPU or SRC clock of interest is set to '0' the true clock will be driven high at 2 x IREF and the complementary clock will be tristated. If the control register is programmed to '1' both clocks will be tristated.

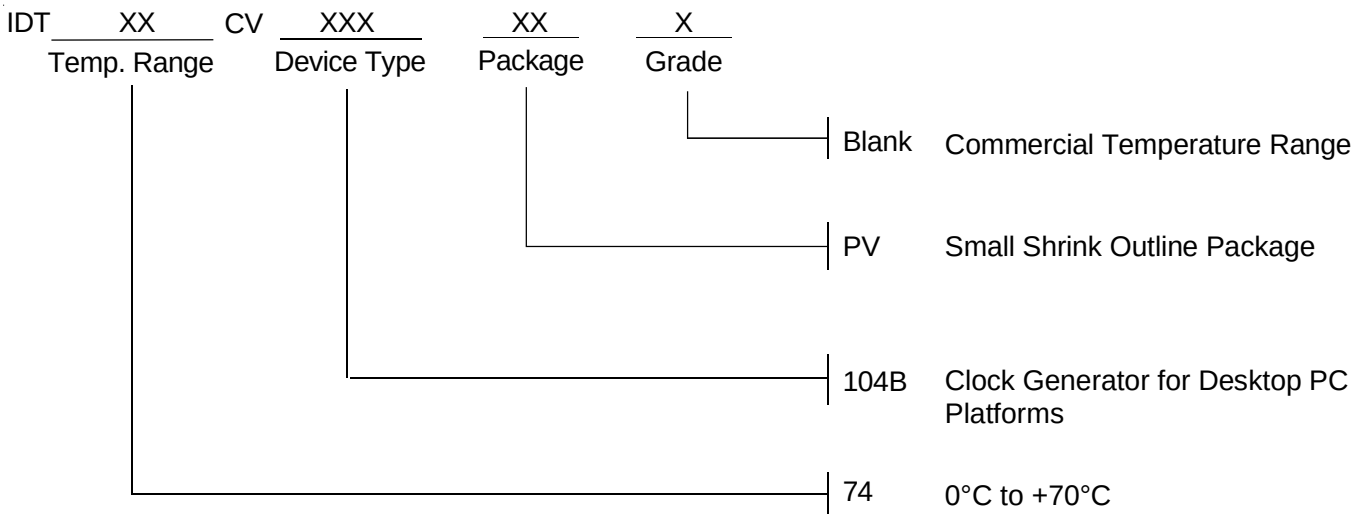


PD# DE-ASSERTION

The time from the de-assertion of PD# or until power supply ramps to get stable clocks will be less than 1.8ms. If the drive mode control bit for PD# tristate is programmed to '1' the stopped differential pair must first be driven high to a minimum of 200mV in less than 300µs of PD# deassertion.



ORDERING INFORMATION



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