Dot Matrix LED Unit for Indoor Use LT1461ED(Chip On Board Type)

■ Features

- No. of dots : 16×16dots
- Outline dimensions : 64×64mm
- Dot size : ø2.8mm
- Dot pitch : 4.0mm
- Radiation color : Yellow-green+Red(dichromatic type)
- Driving method : 1/16 duty dynamic drive

LT1461ED

■ Absolute Maximum Ratings (Ta=25˚C)

Parameter	Symbol	Rating	Unit
Supply voltage for IC	V_{CC}	6.0	V
Supply voltage for LED	V_{LED}	6.0	V
Input voltage	V_I	-0.3 to +5.5	V
Turn-on time	t_{ON}	1	ms
Operating temperature	T_{opr}	-10 to +45	˚C
Storage temperature	T_{stg}	-20 to +70	˚C
Power dissipation	P	13	W

■ Electrical Characteristics (V_{CC}=5V,V_{LED}=5V,Ta=25˚C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage for IC	V_{CC}	4.75	5.0	5.25	V
Supply voltage for LED	V_{LED}	—	5.0	5.25	V
IC current dissipation*1	I_{CC}	—	50	—	mA
LED current dissipation*1	I_{LED}	—	1.8	—	A
Input voltage	V_{IH}	3.5	—	—	V
	V_{IL}	—	—	1.5	V
Input current	I_{IH}	—	—	0.1	µA
	I_{IL}	—	—	0.12	mA
Clock frequency	f_{CLK}	—	—	4	MHz
Frame frequency	f_{FR}	80	—	625	Hz

*1 Under the condition that dichromatic all dots are lit.

■ Optical Characteristics (V_{CC}=5V,V_{LED}=5V,Ta=25˚C)

Parameter		Symbol	TYP	Unit
Luminance	Red	L_V	90	cd/m²
	Yellow-green		90	
Viewing angle		$2\theta 1/2$	80	°
Peak emission wavelength	Red	λp	635	nm
	Yellow-green		565	

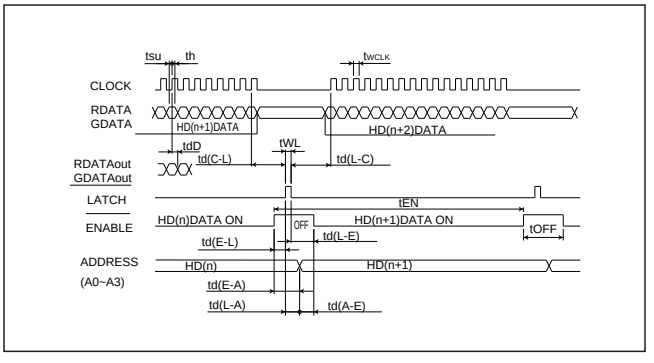
■ Terminal Functions

Connector	Symbol	Function
Power supply (CN1)	V_{LED}	Supply voltage for LED (+5V)
	V_{CC}	Supply voltage for IC (+5V)
	GND1	Ground for IC
	GND2	Ground for LED
Input signal (CN2)	A0 to A3	Address specification signal for row driver
	RDATA	Serial data input for red (H=ON, L=OFF)
	GDATA	Serial data input for yellow-green (H=ON, L=OFF)
	$\overline{LATCH}$	Latch signal of display data. L: Contents are latched.
	$\overline{ENABLE}$	Controls ON/OFF of LED (H: LED OFF)
	CLOCK	Clock signal for data transmission in the shift-register. (L→H: serial data is shifted.)
	GND1	Ground for signal. (Connected to ground for IC)
Output signal (CN3)	A0 to A3	Buffered input signal
	RDATA	Input signal generated through 16-bit shift register or buffer
	GDATA	Input signal generated through 16-bit shift register or buffer
	$\overline{LATCH}$	Buffered input signal
	$\overline{ENABLE}$	Buffered input signal
	CLOCK	Buffered input signal
	GND1	Ground for signal. (Connected to ground for IC)

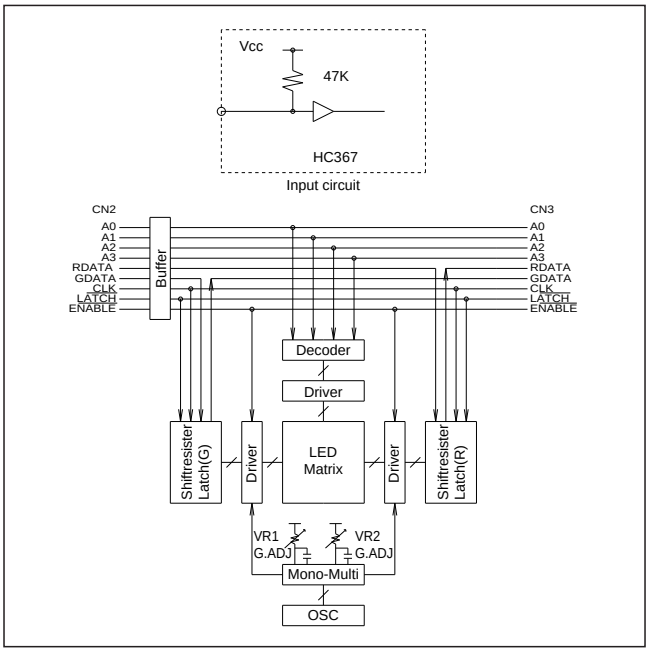
Each signal is used as input signal for next unit.

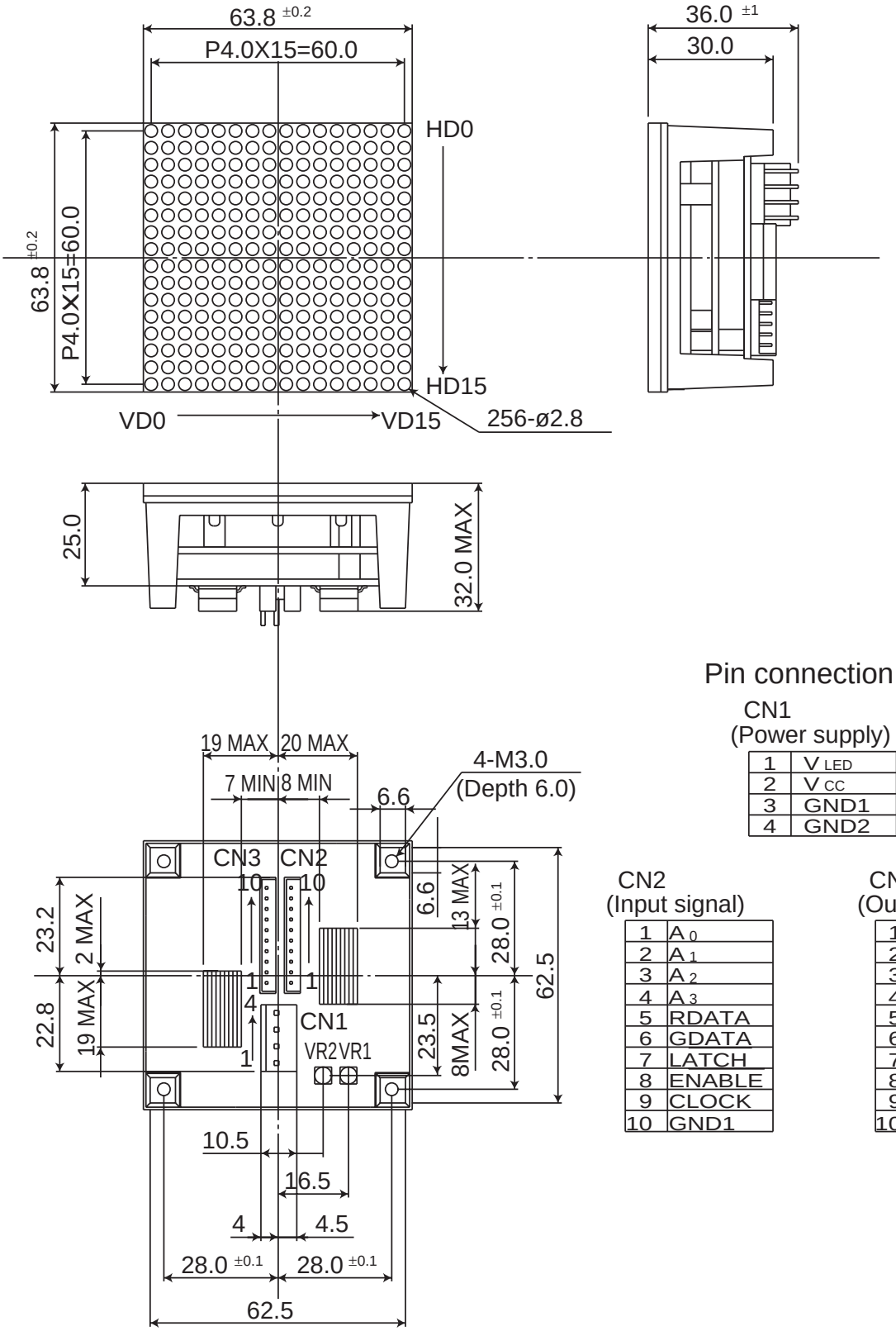
* As for the terminal number, refer to the outline dimensions.

■ Timing Chart



■ Block Diagram





Pin connection

CN1
(Power supply)

1	V_{LED}
2	V_{CC}
3	GND1
4	GND2

CN2
(Input signal)

1	A_0
2	A_1
3	A_2
4	A_3
5	RDATA
6	GDATA
7	LATCH
8	ENABLE
9	CLOCK
10	GND1

CN3
(Output signal)

1	A_0
2	A_1
3	A_2
4	A_3
5	RDATA
6	GDATA
7	LATCH
8	ENABLE
9	CLOCK
10	GND1