

# 4.5ns Single/Dual Supply 3V/5V Comparator with Rail-to-Rail Output

## FEATURES

- **UltraFast: 4.5ns at 20mV Overdrive**  
**7ns at 5mV Overdrive**
- **Low Power: 4.2mA at 3V**
- Separate Input and Output Power Supplies
- Output Optimized for 3V and 5V Supplies
- Input Voltage Range Extends 100mV Below Negative Rail
- TTL/CMOS Compatible Rail-to-Rail Output
- Low Power Shutdown Mode: 0.1 $\mu$ A

## APPLICATIONS

- High Speed Differential Line Receiver
- Crystal Oscillator Circuits
- Level Translators
- Threshold Detectors/Discriminators
- Zero-Crossing Detectors
- High Speed Sampling Circuits
- Delay Lines

## DESCRIPTION

The LT<sup>®</sup>1719 is an UltraFast<sup>™</sup> comparator optimized for low voltage operation. Separate supplies allow flexible operation to accommodate separate analog input ranges and output logic levels. The input voltage range extends from 100mV below  $V_{EE}$  to 1.2V below  $V_{CC}$ . Internal hysteresis makes the LT1719 easy to use even with slow moving input signals. The rail-to-rail outputs directly interface to TTL and CMOS. Alternatively the symmetric output drive can be harnessed for analog applications or for easy translation to other single supply logic levels.

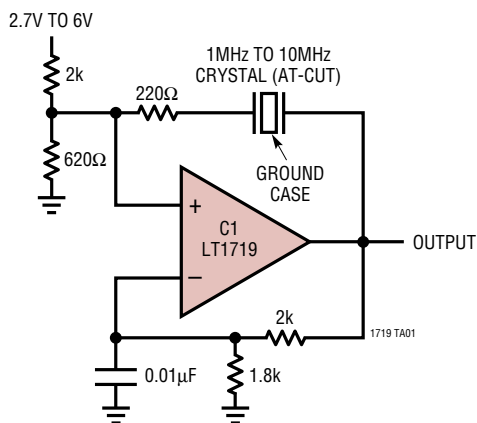
The LT1719 is available in the 8-pin SO package; a shutdown control allows for reduced power consumption and extended battery life in portable applications.

For a dual/quad comparator with similar performance, see the LT1720/LT1721.

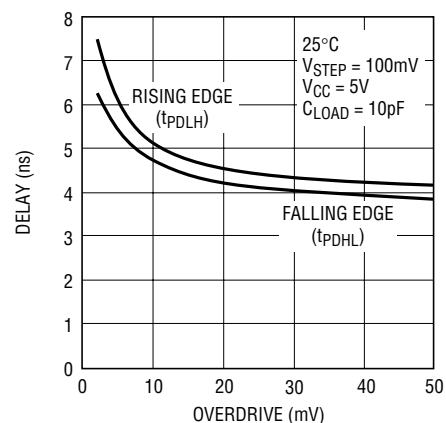
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## TYPICAL APPLICATION

2.7V to 6V Crystal Oscillator with TTL/CMOS Output



Propagation Delay vs Overdrive



1719 TA02

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage	
+V <sub>S</sub> to GND	7V
V <sub>CC</sub> to V <sub>EE</sub>	12V
+V <sub>S</sub> to V <sub>EE</sub>	12V
V <sub>EE</sub> to GND	-12V to 0.3V
Input Current (+IN, -IN or SHDN)	±10mA
Output Current (Continuous)	±20mA
Operating Temperature Range	
C Grade	0°C to 70°C
I Grade	-40°C to 85°C
Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

## PACKAGE/ORDER INFORMATION

<p>S8 PACKAGE 8-LEAD PLASTIC SO T<sub>JMAX</sub> = 150°C, θ<sub>JA</sub> = 200°C/W</p>	ORDER PART NUMBER
	LT1719CS8 LT1719IS8
	S8 PART MARKING
	1719 1719I

Consult factory for Military grade parts.

## ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T<sub>A</sub> = 25°C. V<sub>CC</sub> = 5V, V<sub>EE</sub> = -5V, +V<sub>S</sub> = 5V, V<sub>CM</sub> = 1V, C<sub>OUT</sub> = 10pF, V<sub>SHDN</sub> = 0.5V, V<sub>OVERDRIVE</sub> = 20mV, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V <sub>CC</sub> - V <sub>EE</sub>	Input Supply Voltage		● 2.7		10.5	V
+V <sub>S</sub>	Output Supply Voltage		● 2.7		6	V
V <sub>CMR</sub>	Input Voltage Range	(Note 2)	● V <sub>EE</sub> - 0.1		V <sub>CC</sub> - 1.2	V
V <sub>TRIP+</sub>	Input Trip Points	(Note 3)	● -1.5		5.5	mV
V <sub>TRIP-</sub>			● -5.5		1.5	mV
V <sub>OS</sub>	Input Offset Voltage	(Note 3)		● 0.4	2.5	mV
					3.5	mV
V <sub>HYST</sub>	Input Hysteresis Voltage	(Note 3)	● 2.0	3.5	7	mV
ΔV <sub>OS</sub> /ΔT	Input Offset Voltage Drift		●	10		μV/°C
I <sub>B</sub>	Input Bias Current		● -6	-2.5	0	μA
I <sub>OS</sub>	Input Offset Current		●	0.2	0.6	μA
CMRR	Common Mode Rejection Ratio	(Note 4)	● 55	70		dB
PSRR	Power Supply Rejection Ratio	(Note 5)	● 65	80		dB
A <sub>V</sub>	Voltage Gain	(Note 6)		∞		
V <sub>OH</sub>	Output High Voltage	I <sub>SOURCE</sub> = 4mA, V <sub>IN</sub> = V <sub>TRIP+</sub> + 10mV	● +V <sub>S</sub> - 0.4			V
V <sub>OL</sub>	Output Low Voltage	I <sub>SINK</sub> = 10mA, V <sub>IN</sub> = V <sub>TRIP-</sub> - 10mV	●		0.4	V
t <sub>PD20</sub>	Propagation Delay	V <sub>OVERDRIVE</sub> = 20mV (Note 7), V <sub>EE</sub> = 0V	●	4.5	6.5	ns
		V <sub>OVERDRIVE</sub> = 20mV, V <sub>EE</sub> = -5V			8.0	ns
				4.2		ns
t <sub>PD5</sub>	Propagation Delay	V <sub>OVERDRIVE</sub> = 5mV (Notes 7, 8), V <sub>EE</sub> = 0V	●	7	10	ns
					13	ns
t <sub>SKEW</sub>	Propagation Delay Skew	(Note 9) Between t <sub>PD+</sub> /t <sub>PD-</sub>		0.5	1.5	ns
t <sub>r</sub>	Output Rise Time	10% to 90%		2.5		ns
t <sub>f</sub>	Output Fall Time	90% to 10%		2.2		ns

**ELECTRICAL CHARACTERISTICS** The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 5\text{V}$ ,  $V_{EE} = -5\text{V}$ ,  $+V_S = 5\text{V}$ ,  $V_{CM} = 1\text{V}$ ,  $C_{OUT} = 10\text{pF}$ ,  $V_{SHDN} = 0.5\text{V}$ ,  $V_{OVERDRIVE} = 20\text{mV}$ , unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{JITTER}$	Output Timing Jitter	$V_{IN} = 1.2V_{P-P}$ (6dBm), $Z_{IN} = 50\Omega$ $f = 20\text{MHz}$		15 11		$\text{pSRMS}$ $\text{pSRMS}$
$f_{MAX}$	Maximum Toggle Frequency	$V_{OVERDRIVE} = 50\text{mV}$ , $+V_S = 3\text{V}$ $V_{OVERDRIVE} = 50\text{mV}$ , $+V_S = 5\text{V}$		70 62.5		MHz MHz
$t_{OFF}$	Turn-Off Delay	Time to $Z_{OUT} \geq 10k\Omega$		75		ns
$t_{ON}$	Wake-Up Delay	Time to $V_{OH}$ or $V_{OL}$ , $I_{LOAD} = 1\text{mA}$		350		ns
$I_{CC}$	Positive Input Stage Supply Current	$+V_S = V_{CC} = 5\text{V}$ , $V_{EE} = -5\text{V}$	●	1.0	2.2	mA
		$+V_S = V_{CC} = 3\text{V}$ , $V_{EE} = 0\text{V}$	●	0.9	1.8	mA
$I_{EE}$	Negative Input Stage Supply Current	$+V_S = V_{CC} = 5\text{V}$ , $V_{EE} = -5\text{V}$	●	-4.8	-2.6	mA
		$+V_S = V_{CC} = 3\text{V}$ , $V_{EE} = 0\text{V}$	●	-3.8	-2.2	mA
$I_S$	Positive Output Stage Supply Current	$+V_S = V_{CC} = 5\text{V}$ , $V_{EE} = -5\text{V}$	●	4.2	8	mA
		$V_S = V_{CC} = 3\text{V}$ , $V_{EE} = 0\text{V}$	●	3.3	6	mA
$I_{CCS}$	Disabled Supply Currents	$+V_S = 6\text{V}$ , $V_{CC} = 5\text{V}$ , $V_{EE} = -5\text{V}$	●	0.2	30	$\mu\text{A}$
$I_{SS}$		$V_{SHDN} = 5.5\text{V}$	●	7	50	$\mu\text{A}$
$I_{EES}$			●	-30	-0.2	$\mu\text{A}$
$I_{CCSO}$		$+V_S = 6\text{V}$ , $V_{CC} = 5\text{V}$ , $V_{EE} = -5\text{V}$	●	0.1	20	$\mu\text{A}$
$I_{SSO}$	Shutdown Pin Open		●	0.1	20	$\mu\text{A}$
$I_{EEO}$			●	-20	0.1	$\mu\text{A}$

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** If one input is within these common mode limits, the other input can go outside the common mode limits and the output will be valid.

**Note 3:** The LT1719 comparator includes internal hysteresis. The trip points are the input voltage needed to change the output state in each direction. The offset voltage is defined as the average of  $V_{TRIP+}$  and  $V_{TRIP-}$ , while the hysteresis voltage is the difference of these two.

**Note 4:** The common mode rejection ratio is measured with  $V_{CC} = 5\text{V}$ ,  $V_{EE} = -5\text{V}$  and is defined as the change in offset voltage measured from  $V_{CM} = -5.1\text{V}$  to  $V_{CM} = 3.8\text{V}$ , divided by 8.9V.

**Note 5:** The power supply rejection ratio is measured with  $V_{CM} = 1\text{V}$  and is defined as the worst of: the change in offset voltage from  $V_{EE} = -5\text{V}$  to  $V_{EE} = 0\text{V}$  divided by 5V, or the change in offset voltage

from  $V_{CC} = +V_S = 2.7\text{V}$  to  $V_{CC} = +V_S = 6\text{V}$  (with  $V_{EE} = 0\text{V}$ ) divided by 3.3V.

**Note 6:** Because of internal hysteresis, there is no small-signal region in which to measure gain. Proper operation of internal circuitry is ensured by measuring  $V_{OH}$  and  $V_{OL}$  with only 10mV of overdrive.

**Note 7:** Propagation delay measurements made with 100mV steps. Overdrive is measured relative to  $V_{TRIP\pm}$ .

**Note 8:**  $t_{PD}$  cannot be measured in automatic handling equipment with low values of overdrive. The LT1719 is 100% tested with a 100mV step and 20mV overdrive. Correlation tests have shown that  $t_{PD}$  limits can be guaranteed with this test, if additional DC tests are performed to guarantee that all internal bias conditions are correct.

**Note 9:** Propagation Delay Skew is defined as:

$$t_{SKEW} = |t_{PDLH} - t_{PDHL}|$$

## PIN FUNCTIONS

**$V_{CC}$  (Pin 1):** Positive Supply Voltage for Input Stage.

**+IN (Pin 2):** Noninverting Input of Comparator.

**-IN (Pin 3):** Inverting Input of Comparator.

**$V_{EE}$  (Pin 4):** Negative Supply Voltage for Input Stage and Chip Substrate.

**GND (Pin 5):** Ground.

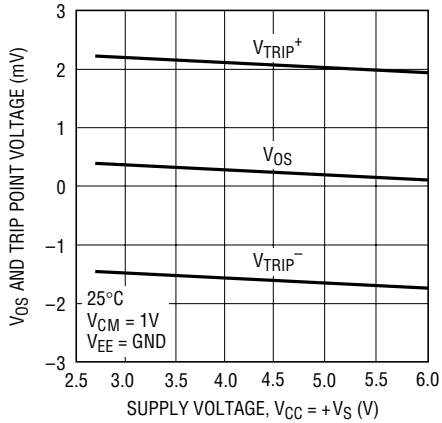
**SHDN (Pin 6):** Shutdown. Pull to ground to enable comparator.

**OUT (Pin 7):** Output of Comparator.

**$+V_S$  (Pin 8):** Positive Supply Voltage for Output Stage.

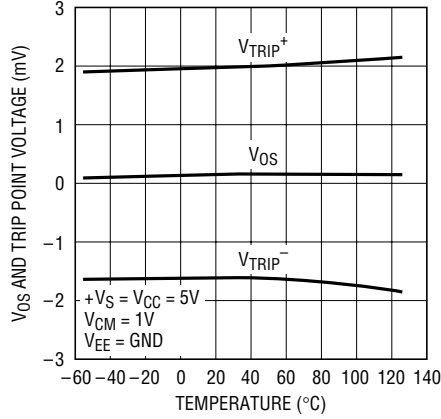
# TYPICAL PERFORMANCE CHARACTERISTICS

**Input Offset and Trip Voltages vs Supply Voltage**



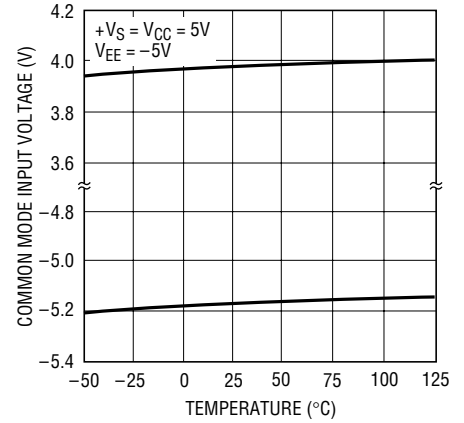
1719 G01

**Input Offset and Trip Voltages vs Temperature**



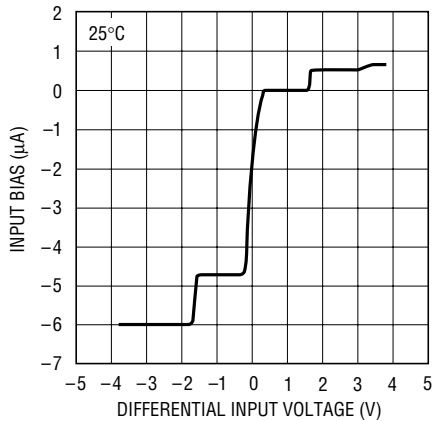
1719 G02

**Input Common Mode Limits vs Temperature**



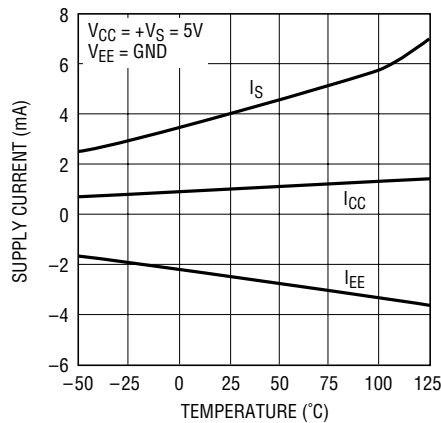
1719 G03

**Input Current vs Differential Input Voltage**



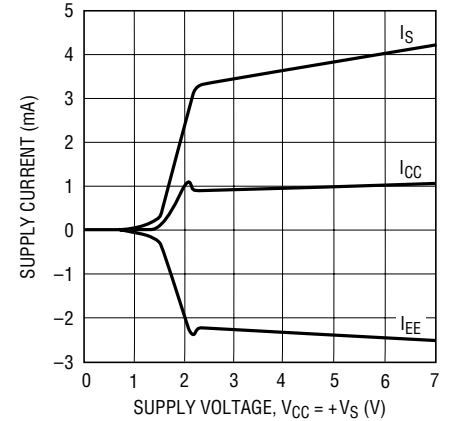
1719 G04

**Quiescent Supply Current vs Temperature**



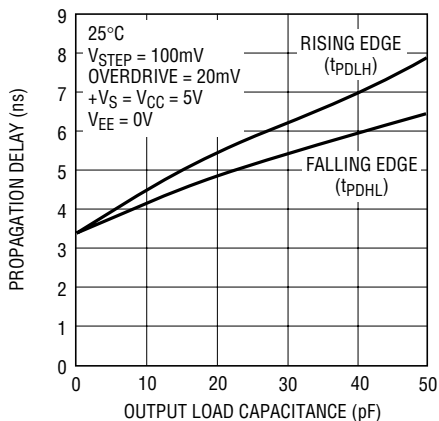
1719 G05

**Quiescent Supply Current vs Supply Voltage**



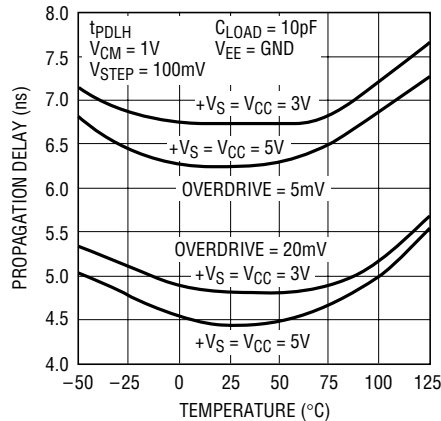
1719 G06

**Propagation Delay vs Load Capacitance**



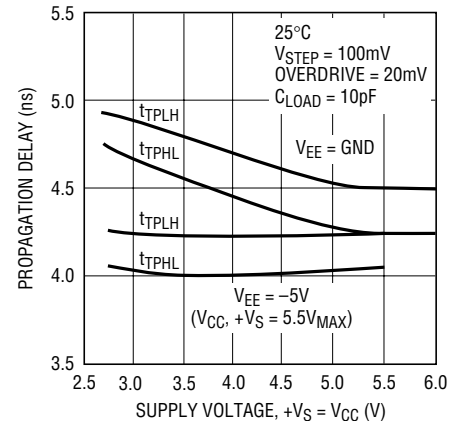
1719 G07

**Propagation Delay vs Temperature**



1719 G08

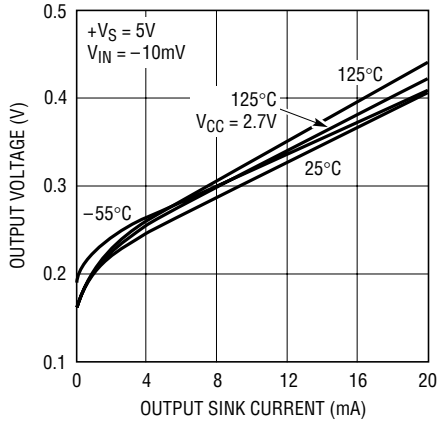
**Propagation Delay vs Supply Voltage**



1719 G09

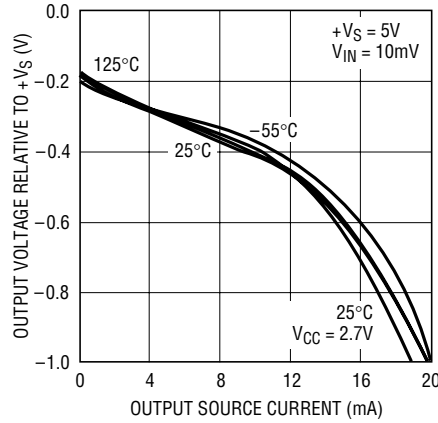
# TYPICAL PERFORMANCE CHARACTERISTICS

**Output Low Voltage vs Load Current**



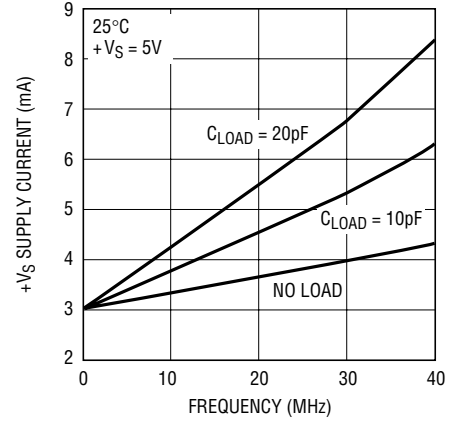
1719 G10

**Output High Voltage vs Load Current**



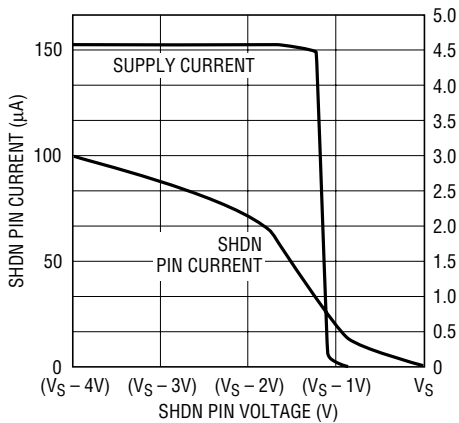
1719 G11

**Supply Current vs Frequency**



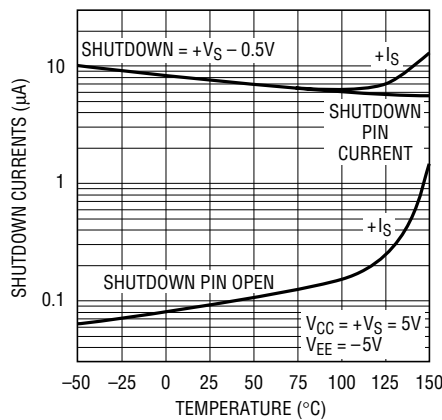
1719 G12

**Shutdown Currents vs Shutdown Voltage**



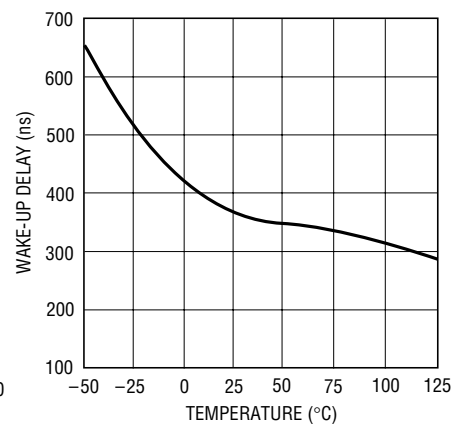
1719 G13

**Shutdown Currents vs Temperature**



1719 G14

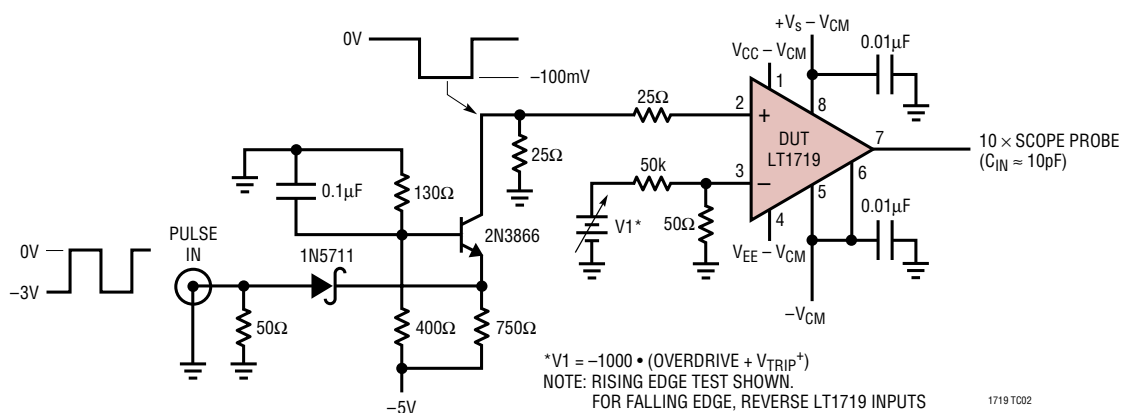
**Wake-Up Delay vs Temperature**



1719 G15

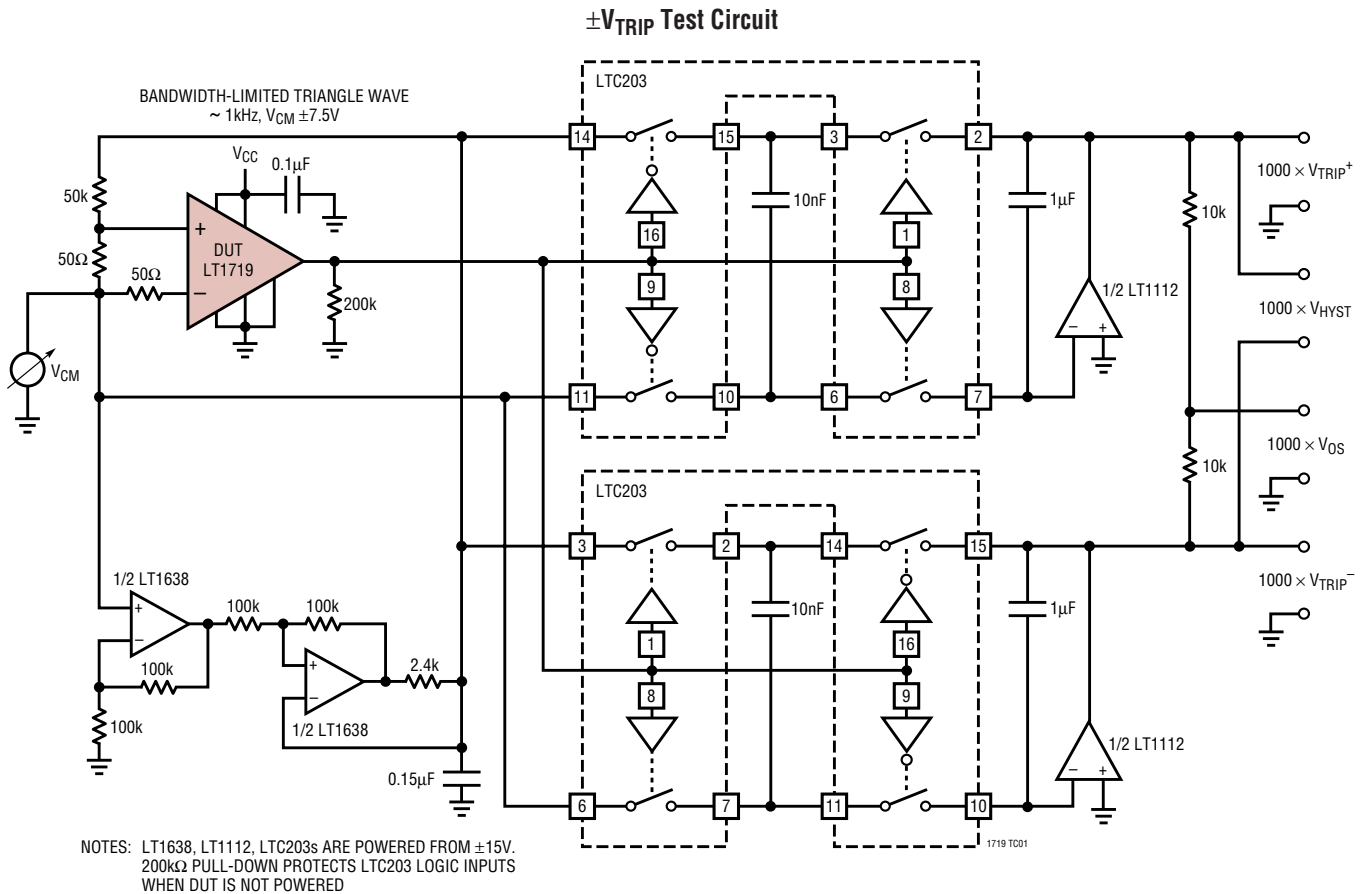
# TEST CIRCUITS

**Response Time Test Circuit**



1719 T002

TEST CIRCUITS



APPLICATIONS INFORMATION

Power Supply Configurations

The LT1719 has separate supply pins for the input and output stages that allow flexible operation, accommodating separate voltage ranges for the analog input and the output logic. Of course, a single 3V/5V supply may be used by tying +V<sub>S</sub> and V<sub>CC</sub> together as well as GND and V<sub>EE</sub>.

The minimum voltage requirement can be simply stated as both the output and the input stages need at least 2.7V and the V<sub>EE</sub> pin must be equal to or less than ground.

The following rules must be adhered to in any configuration:

- $2.7V \leq (V_{CC} - V_{EE}) \leq 10.5V$
- $2.7V \leq (+V_S - GND) \leq 6V$
- $(+V_S - V_{EE}) \leq 10.5V$
- $V_{EE} \leq \text{Ground}$

Although the ground pin need not be tied to system ground, most applications will use it that way. Figure 1 shows three common configurations. The final one is uncommon, but it will work and may be useful as a level translator; the input stage is run from -5.2V and ground while the output stage is run from 3V and ground. In this case the common mode input voltage range does not include ground, so it may be helpful to tie V<sub>CC</sub> to 3V anyway. Conversely, V<sub>CC</sub> may also be tied below ground, as long as the above rules are not violated.

Input Voltage Considerations

The LT1719 is specified for a common mode range of -100mV to 3.8V when used with a single 5V supply. A more general consideration is that the common mode range is 100mV below V<sub>EE</sub> to 1.2V below V<sub>CC</sub>. The criterion for this common mode limit is that the output still

## APPLICATIONS INFORMATION

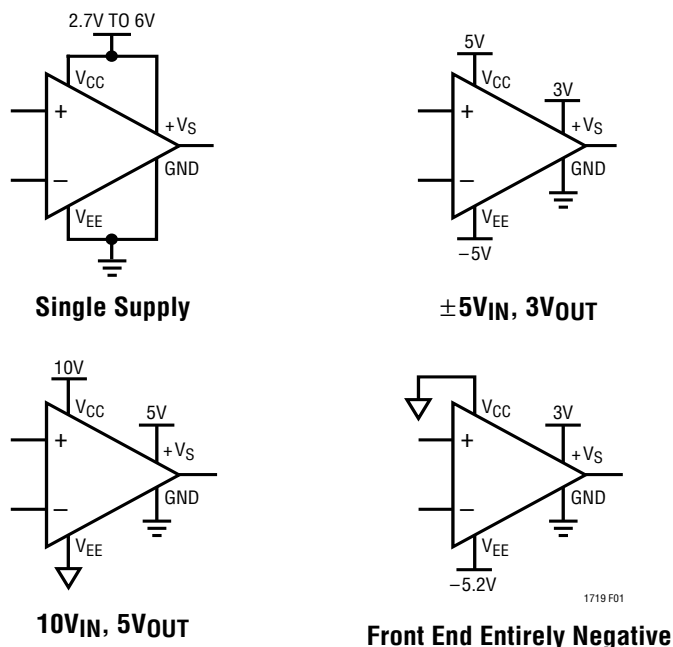


Figure 1. Variety of Power Supply Configurations

responds correctly to a small differential input signal. If one input is within the common mode limit, the other input signal can go outside the common mode limits, up to the absolute maximum limits, and the output will retain the correct polarity.

When either input signal falls below the negative common mode limit, the internal PN diode formed with the substrate can turn on, resulting in significant current flow through the die. An external Schottky clamp diode between the input and the negative rail can speed up recovery from negative overdrive by preventing the substrate diode from turning on.

When both input signals are below the negative common mode limit, phase reversal protection circuitry prevents false output inversion to at least  $-400\text{mV}$  common mode. However, the offset and hysteresis in this mode will increase dramatically, to as much as  $15\text{mV}$  each. The input bias currents will also increase.

When both input signals are above the positive common mode limit, the input stage will get debiased and the output polarity will be random. However, the internal hysteresis will hold the output to a valid logic level. When at least one of the inputs returns to within the common mode limits, recovery from this state will take as long as  $1\mu\text{s}$ .

The input stage is protected against damage from large differential signals, up to and beyond a differential voltage equal to the supply voltage, limited only by the absolute maximum currents noted. External input protection circuitry is only needed if currents would otherwise exceed these absolute maximums. The internal catch diodes can conduct current up to these rated maximums without latchup, even when the supply voltage is at the absolute maximum rating.

The propagation delay does not increase significantly when driven with large differential voltages, but with low levels of overdrive, an apparent increase may be seen with large source resistances due to an RC delay caused by the  $2\text{pF}$  typical input capacitance.

### Input Bias Current

Input bias current is measured with both inputs held at  $1\text{V}$ . As with any PNP differential input stage, the LT1719 bias current flows out of the device. It will go to zero on the higher of the two inputs and double on the lower of the two inputs. With more than two diode drops of differential input voltage, the LT1719's input protection circuitry activates, and current out of the lower input will increase an additional 30% and there will be a small bias current into the higher of the two input pins, of  $4\mu\text{A}$  or less. See the Typical Performance curve "Input Current vs Differential Input Voltage."

### High Speed Design Considerations

Application of high speed comparators is often plagued by oscillations. The LT1719 has  $4\text{mV}$  of internal hysteresis, which will prevent oscillations as long as parasitic output to input feedback is kept below  $4\text{mV}$ . However, with the  $2\text{V/ns}$  slew rate of the LT1719 outputs, a  $4\text{mV}$  step can be created at a  $100\Omega$  input source with only  $0.02\text{pF}$  of output to input coupling. The LT1719's pinout has been arranged to minimize problems by placing the sensitive inputs away from the outputs, shielded by the power rails. The input and output traces of the circuit board should also be separated, and the requisite level of isolation is readily achieved if a topside ground plane runs between the output and the inputs. For multilayer boards where the ground plane is internal, a topside ground or supply trace should be run between the inputs and the output.

## APPLICATIONS INFORMATION

Figure 2 shows a typical topside layout of the LT1719 on such a multilayer board. Shown is the topside metal etch including traces, pin escape vias, and the land pads for an SO-8 LT1719 and its adjacent X7R 10nF bypass capacitors in the 1206 case.

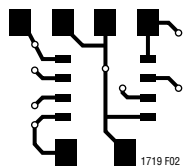


Figure 2. Typical Topside Metal for Multilayer PCB Layouts

The ground trace from Pin 5 runs under the device up to the bypass capacitor, shielding the inputs from the outputs. Note the use of a common via for the LT1719 and the bypass capacitors, which minimizes interference from high frequency energy running around the ground plane or power distribution traces.

The supply bypass should include an adjacent 10nF ceramic capacitor and a 2.2 $\mu$ F tantalum capacitor no farther than 5cm away; use more capacitance on  $+V_S$  if driving more than 4mA loads. To prevent oscillations, it is helpful to balance the impedance at the inverting and noninverting inputs; source impedances should be kept low, preferably 1k $\Omega$  or less.

The outputs of the LT1719 are capable of very high slew rates. To prevent overshoot, ringing and other problems with transmission line effects, keep the output traces shorter than 10cm, or be sure to terminate the lines to maintain signal integrity. The LT1719 can drive DC terminations of 200 $\Omega$  or more, but lower characteristic impedance traces can be used with series termination or AC termination topologies.

### Shutdown Control

The LT1719 features a shutdown control pin for reduced quiescent current when the comparator is not needed. During shutdown, the inputs and the outputs become high impedances. The LT1719 is enabled when the shutdown input is pulled low. A logic high disables the comparator. The logic interface is based on the output power rails,  $+V_S$  and GND, with a threshold roughly two diode drops less

than  $+V_S$ . Therefore, if driven by a standard TTL gate, a pull-up resistor should be used. Because shutdown is active high, this resistor adds little power drain during shutdown.

For applications that do not use the shutdown feature, it may be helpful to tie the shutdown control to ground through a 100 $\Omega$  resistor rather than directly. This allows the SHDN pin to be pulled high during debug or in-circuit test (bed of nails) so that the output node can be wiggled without damaging the low impedance output driver of the LT1719.

The shutdown state is not guaranteed to be useful as a multiplexer. Digital signals can have extremely fast edge rates that may be enough to momentarily activate the LT1719 output stage via internal capacitive coupling. No damage to the LT1719 will result, but this could prove deleterious to the intended recipient of the signal.

The LT1719 includes a FET pull-up on the shutdown control pin (see Simplified Schematic) as well as other internal structures to make the shutdown state current drain  $\ll 1\mu$ A. Shutdown is guaranteed with an open circuit on the shutdown control pin. When the shutdown control pin is driven to  $+V_S - 0.5V$ , the 70k $\Omega$  linear region impedance of the pull-up FET will cause a current flow of 7 $\mu$ A (typ) into the  $+V_S$  pin and out the shutdown pin. Currents in all other power supply terminals will be  $< 1\mu$ A.

### Power Supply Sequencing

The LT1719 is designed to tolerate any power supply sequencing at system turn-on and power down. In any of the previously shown power supply configurations, the various supplies can activate in any order without excessive current drain by the LT1719.

As always, the Absolute Maximum Ratings must not be exceeded, either on the power supply terminals or the input terminals. Power supply sequencing problems can occur when input signals are powered from supplies that are independent of the LT1719's supplies. For the comparator inputs, the signals should be powered from the same  $V_{CC}$  and  $V_{EE}$  supplies as the LT1719. For the shutdown input, the signal should be powered from the same  $+V_S$  as the LT1719.



## APPLICATIONS INFORMATION

### Hysteresis

The LT1719 includes internal hysteresis, which makes it easier to use than many other similar speed comparators.

The input-output transfer characteristic is illustrated in Figure 3 showing the definitions of  $V_{OS}$  and  $V_{HYST}$  based upon the two measurable trip points. The hysteresis band makes the LT1719 well behaved, even with slowly moving inputs.

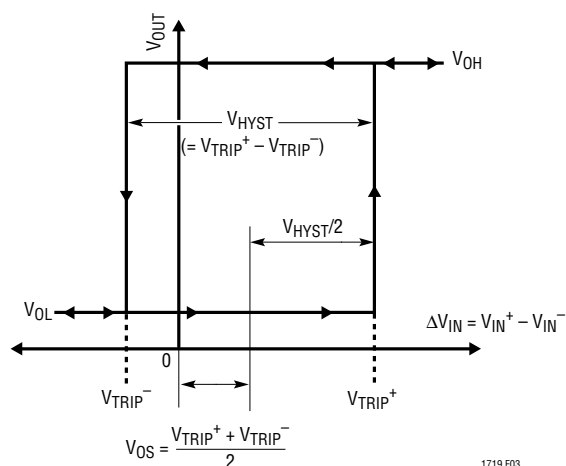


Figure 3. Hysteresis I/O Characteristics

The exact amount of hysteresis will vary from part to part as indicated in the specifications table. The hysteresis level will also vary slightly with changes in supply voltage and common mode voltage. A key advantage of the LT1719 is the significant reduction in these effects, which is important whenever an LT1719 is used to detect a threshold crossing in one direction only. In such a case, the relevant trip point will be all that matters, and a stable offset voltage with an unpredictable level of hysteresis, as seen in competing comparators, is useless. The LT1719 is many times better than prior comparators in these regards. In fact, the CMRR and PSRR tests are performed by checking for changes in either trip point to the limits indicated in the specifications table. Because the offset voltage is the average of the trip points, the CMRR and PSRR of the offset voltage is therefore guaranteed to be at least as good as those limits. This more stringent test also puts a limit on the common mode and power supply dependence of the hysteresis voltage.

Additional hysteresis may be added externally. The rail-to-rail outputs of the LT1719 make this more predictable than with TTL output comparators due to the LT1719's small variability of  $V_{OH}$  (output high voltage).

To add additional hysteresis, set up positive feedback by adding additional external resistor R3 as shown in Figure 4. Resistor R3 adds a portion of the output to the threshold set by the resistor string. The LT1719 pulls the outputs to  $+V_S$  and ground to within 200mV of the rails with light loads, and to within 400mV with heavy loads. For the load of most circuits, a good model for the voltage on the right side of R3 is 300mV or  $+V_S - 300\text{mV}$ , for a total voltage swing of  $(+V_S - 300\text{mV}) - (300\text{mV}) = +V_S - 600\text{mV}$ .

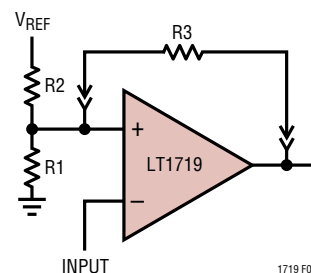


Figure 4. Additional External Hysteresis

With this in mind, calculation of the resistor values needed is a two-step process. First, calculate the value of R3 based on the additional hysteresis desired, the output voltage swing and the impedance of the primary bias string:

$$R3 = (R1 || R2)(+V_S - 0.6V)/(\text{additional hysteresis})$$

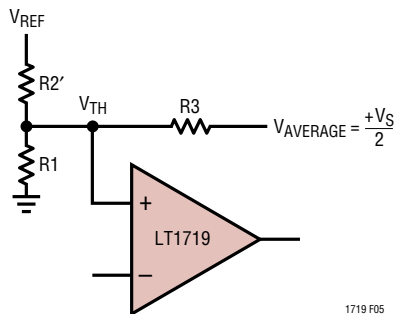
Additional hysteresis is the desired overall hysteresis less the internal 4mV hysteresis.

The second step is to recalculate R2 to set the same average threshold as before. The average threshold before was set at  $V_{TH} = (V_{REF})(R1)/(R1 + R2)$ . The new R2 is calculated based on the average output voltage ( $+V_S/2$ ) and the simplified circuit model in Figure 5. To assure that the comparator's noninverting input is, on average, the same  $V_{TH}$  as before:

$$R2' = (V_{REF} - V_{TH})/(V_{TH}/R1 + (V_{TH} - V_S/2)/R3)$$

For additional hysteresis of 10mV or less, it is not uncommon for R2' to be the same as R2 within 1% resistor tolerances.

## APPLICATIONS INFORMATION



**Figure 5. Model for Additional Hysteresis Calculations**

This method will work for additional hysteresis of up to a few hundred millivolts. Beyond that, the impedance of R3 is low enough to effect the bias string, and adjustment of R1 may also be required. Note that the currents through the R1/R2 bias string should be many times the input currents of the LT1719. For 5% accuracy, the current must be at least 20 times the input current, more for higher accuracy.

### Interfacing the LT1719 to ECL

The LT1719 comparators can be used in high speed applications where Emitter-Coupled Logic (ECL) is deployed. To interface the output of the LT1719 to ECL logic inputs, standard TTL/CMOS to ECL level translators such as the 10H124, 10H424 and 100124 can be used. These components come at a cost of a few nanoseconds additional delay as well as supply currents of 50mA or more, and are only available in quads. A faster, simpler and lower power translator can be constructed with resistors as shown in Figure 6.

Figure 6a shows the standard TTL to Positive ECL (PECL) resistive level translator. This translator cannot be used for the LT1719, or with CMOS logic, because it depends on the 820Ω resistor to limit the output swing ( $V_{OH}$ ) of the all-NPN TTL gate with its so-called totem-pole output. The LT1719 is fabricated in a complementary bipolar process and the output stage has a PNP driver that pulls the output nearly all the way to the supply rail, even when sourcing 10mA.

Figure 6b shows a three resistor level translator for interfacing the LT1719 to ECL running off the same supply rail. No pull-down on the output of the LT1719 is needed, but pull-down R3 limits the  $V_{IH}$  seen by the PECL gate. This is needed because ECL inputs have both a minimum and maximum  $V_{IH}$  specification for proper operation. Resistor

values are given for both ECL interface types; in both cases it is assumed that the LT1719 operates from the same supply rail.

Figure 6c shows the case of translating to PECL from an LT1719 powered by a 3V supply rail. Again, resistor values are given for both ECL interface types. This time four resistors are needed, although with 10KH/E, R3 is not needed. In that case, the circuit resembles the standard TTL translator of Figure 6a, but the function of the new resistor, R4, is much different. R4 loads the LT1719 output when high so that the current flowing through R1 doesn't forward bias the LT1719's internal ESD clamp diode. Although this diode can handle 20mA without damage, normal operation and performance of the output stage can be impaired above 100μA of forward current. R4 prevents this with the minimum additional power dissipation.

Finally, Figure 6d shows the case of driving standard, negative-rail, ECL with the LT1719. Resistor values are given for both ECL interface types and for both a 5V and 3V LT1719 supply rail. Again, a fourth resistor, R4 is needed to prevent the low state current from flowing out of the LT1719, turning on the internal ESD/substrate diodes. Resistor R4 again prevents this with the minimum additional power dissipation.

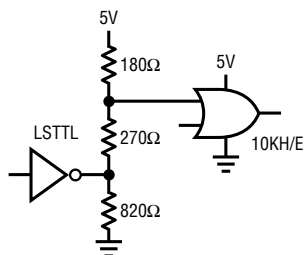
Of course, if the  $V_{EE}$  of the LT1719 is the same as the ECL negative supply, the GND pin can be tied to it as well and  $+V_S$  grounded. Then the output stage has the same power rails as the ECL and the circuits of Figure 6b can be used.

For all the dividers shown, the output impedance is about 110Ω. This makes these fast, less than a nanosecond, with most layouts. Avoid the temptation to use speedup capacitors. Not only can they foul up the operation of the ECL gate because of overshoots, they can damage the ECL inputs, particularly during power-up of separate supply configurations.

The level translator designs assume one gate load. Multiple gates can have significant  $I_{IH}$  loading, and the transmission line routing and termination issues also make this case difficult.

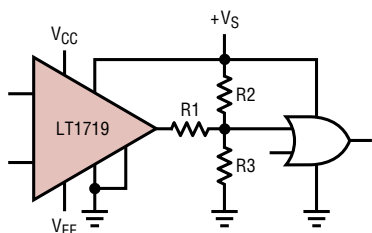
ECL, and particularly PECL, is valuable technology for high speed system design, but it must be used with care. With less than a volt of swing, the noise margins need to be

# APPLICATIONS INFORMATION



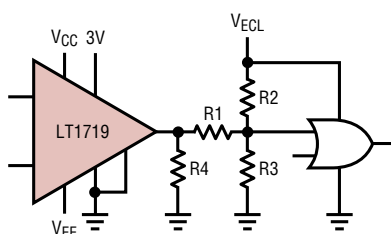
DO NOT USE FOR LT1719  
LEVEL TRANSLATION. SEE TEXT

(a) STANDARD TTL TO PECL TRANSLATOR



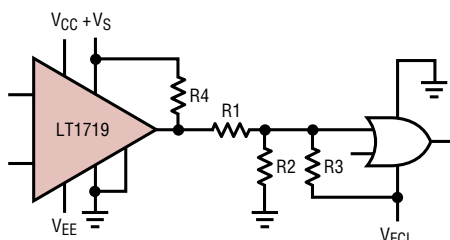
	+Vs	R1	R2	R3
10KH/E	5V OR 5.2V	510Ω	180Ω	750Ω
100K/E	4.5V	620Ω	180Ω	510Ω

(b) LT1719 OUTPUT TO PECL TRANSLATOR



	VECL	R1	R2	R3	R4
10KH/E	5V OR 5.2V	300Ω	180Ω	OMIT	560Ω
100K/E	4.5V	330Ω	180Ω	1500Ω	1000Ω

(c) 3V LT1719 OUTPUT TO PECL TRANSLATOR



ECL FAMILY	VECL	+Vs	R1	R2	R3	R4
10KH/E	-5.2V	5V	560Ω	270Ω	330Ω	1200Ω
		3V	270Ω	510Ω	300Ω	330Ω
100K/E	-4.5V	5V	680Ω	270Ω	300Ω	1500Ω
		3V	330Ω	390Ω	270Ω	430Ω

1719 F06

(d) LT1719 OUTPUT TO STANDARD ECL TRANSLATOR

Figure 6

evaluated carefully. Note that there is some degradation of noise margin due to the  $\pm 5\%$  resistor selections shown. With 10KH/E, there is no temperature compensation of the logic levels, whereas the LT1719 and the circuits shown give levels that are stable with temperature. This will lower the noise margin over temperature. In some configurations it is possible to add compensation with diode or transistor junctions in series with the resistors of these networks.

For more information on ECL design, refer to the ECLiPS data book (DL140), the 10KH system design handbook (HB205) and PECL design (AN1406), all from Motorola.

## Circuit Description

The block diagram of the LT1719 is shown in Figure 7. The circuit topology consists of a differential input stage, a gain stage with hysteresis and a complementary common-emitter output stage. All of the internal signal paths utilize low voltage swings for high speed at low power.

The input stage topology maximizes the input dynamic range available without requiring the power, complexity and die area of two complete input stages such as are found in rail-to-rail input comparators. With a single 2.7V supply, the LT1719 still has a respectable 1.6V of input

## APPLICATIONS INFORMATION

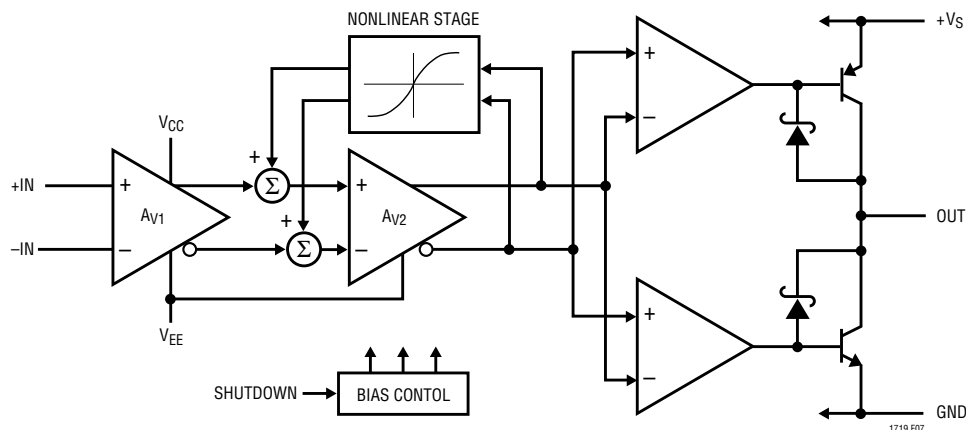


Figure 7. LT1719 Block Diagram

common mode range. The differential input voltage range is rail-to-rail, without the large input currents found in competing devices. The input stage also features phase reversal protection to prevent false outputs when the inputs are driven below the  $-100\text{mV}$  common mode voltage limit.

The internal hysteresis is implemented by positive, nonlinear feedback around a second gain stage. Until this point, the signal path has been entirely differential. The signal path is then split into two drive signals for the upper and lower output transistors. The output transistors are connected common emitter for rail-to-rail output operation. The Schottky clamps limit the output voltages at about  $300\text{mV}$  from the rail, not quite the  $50\text{mV}$  or  $15\text{mV}$  of Linear Technology's rail-to-rail amplifiers and other products. But the output of a comparator is digital, and this output stage can drive TTL or CMOS directly. It can also drive ECL, as described earlier, or analog loads as demonstrated in the applications to follow.

The bias conditions and signal swings in the output stage are designed to turn their respective output transistors off faster than on. This helps minimize the surge of current from  $+V_S$  to ground that occurs at transitions, to minimize the frequency-dependent increase in power consumption. The frequency dependence of the supply current is shown in the Typical Performance Characteristics.

### Speed Limits

The LT1719 comparator is intended for high speed applications, where it is important to understand a few limitations. These limitations can roughly be divided into three categories: input speed limits, output speed limits, and internal speed limits.

There are no significant input speed limits except the shunt capacitance of the input nodes. If the  $2\text{pF}$  typical input nodes are driven, the LT1719 will respond.

The output speed is constrained by two mechanisms, the first of which is the slew currents available from the output transistors. To maintain low power quiescent operation, the LT1719 output transistors are sized to deliver  $35\text{mA}$  to  $60\text{mA}$  typical slew currents. This is sufficient to drive small capacitive loads and logic gate inputs at extremely high speeds. But the slew rate will slow dramatically with heavy capacitive loads. Because the propagation delay ( $t_{PD}$ ) definition ends at the time the output voltage is halfway between the supplies, the fixed slew current makes the LT1719 faster at  $3\text{V}$  than  $5\text{V}$  with large capacitive loads and sufficient input overdrive.

Another manifestation of this output speed limit is skew, the difference between  $t_{PD}^+$  and  $t_{PD}^-$ . The slew currents of the LT1719 vary with the process variations of the PNP and NPN transistors, for rising edges and falling edges respectively. The typical  $0.5\text{ns}$  skew can have either polarity, rising edge or falling edge faster. Again, the skew will increase dramatically with heavy capacitive loads.

## APPLICATIONS INFORMATION

A separate output speed limit is the clamp turnaround. The LT1719 output is optimized for fast initial response, with some loss of turnaround speed, limiting the toggle frequency. The output transistors are idled in a low power state once  $V_{OH}$  or  $V_{OL}$  is reached, by detecting the Schottky clamp action. It is only when the output has slewed from the old voltage to the new voltage, and the clamp circuitry has settled, that the idle state is reached and the LT1719 is fully ready to toggle again. This is typically 8ns for each direction, resulting in a maximum toggle frequency of 62.5MHz. With higher frequencies, dropout and runt pulses can result. Increases in capacitive load will increase the time needed for slewing due to the limited slew currents and the maximum toggle frequency will decrease further. For high toggle frequency applications, consider the LT1394, whose linear output stage can toggle at 100MHz typical.

The internal speed limits manifest themselves as dispersion. All comparators have some degree of dispersion, defined as a change in propagation delay versus input overdrive. The propagation delay of the LT1719 will vary with overdrive, from a typical of 4.5ns at 20mV overdrive to 7ns at 5mV overdrive (typical). The LT1719's primary source of dispersion is the hysteresis stage. As a change of polarity arrives at the gain stage, the positive feedback of the hysteresis stage subtracts from the overdrive available. Only when enough time has elapsed for a signal to propagate forward through the gain stage, backwards through the hysteresis path and forward through the gain stage again, will the output stage receive the same level of overdrive that it would have received in the absence of hysteresis.

The LT1719 is several hundred picoseconds faster when  $V_{EE} = -5V$ , relative to single supply operation. This is due to the internal speed limit; the gain stage operates between  $V_{EE}$  and  $+V_S$ , and it is faster with higher reverse voltage bias due to reduced silicon junction capacitances.

In many applications, as shown in the following examples, there is plenty of input overdrive. Even in applications providing low levels of overdrive, the LT1719 is fast enough that the absolute dispersion of 2.5ns ( $= 7 - 4.5$ ) is often small enough to ignore.

The gain and hysteresis stage of the LT1719 is simple, short and high speed to help prevent parasitic oscillations while adding minimum dispersion. This internal "self-latch" can be usefully exploited in many applications because it occurs early in the signal chain, in a low power, fully differential stage. It is therefore highly immune to disturbances from other parts of the circuit, such as the output, or on the supply lines. Once a high speed signal trips the hysteresis, the output will respond, after a fixed propagation delay, without regard to these external influences that can cause trouble in nonhysteretic comparators.

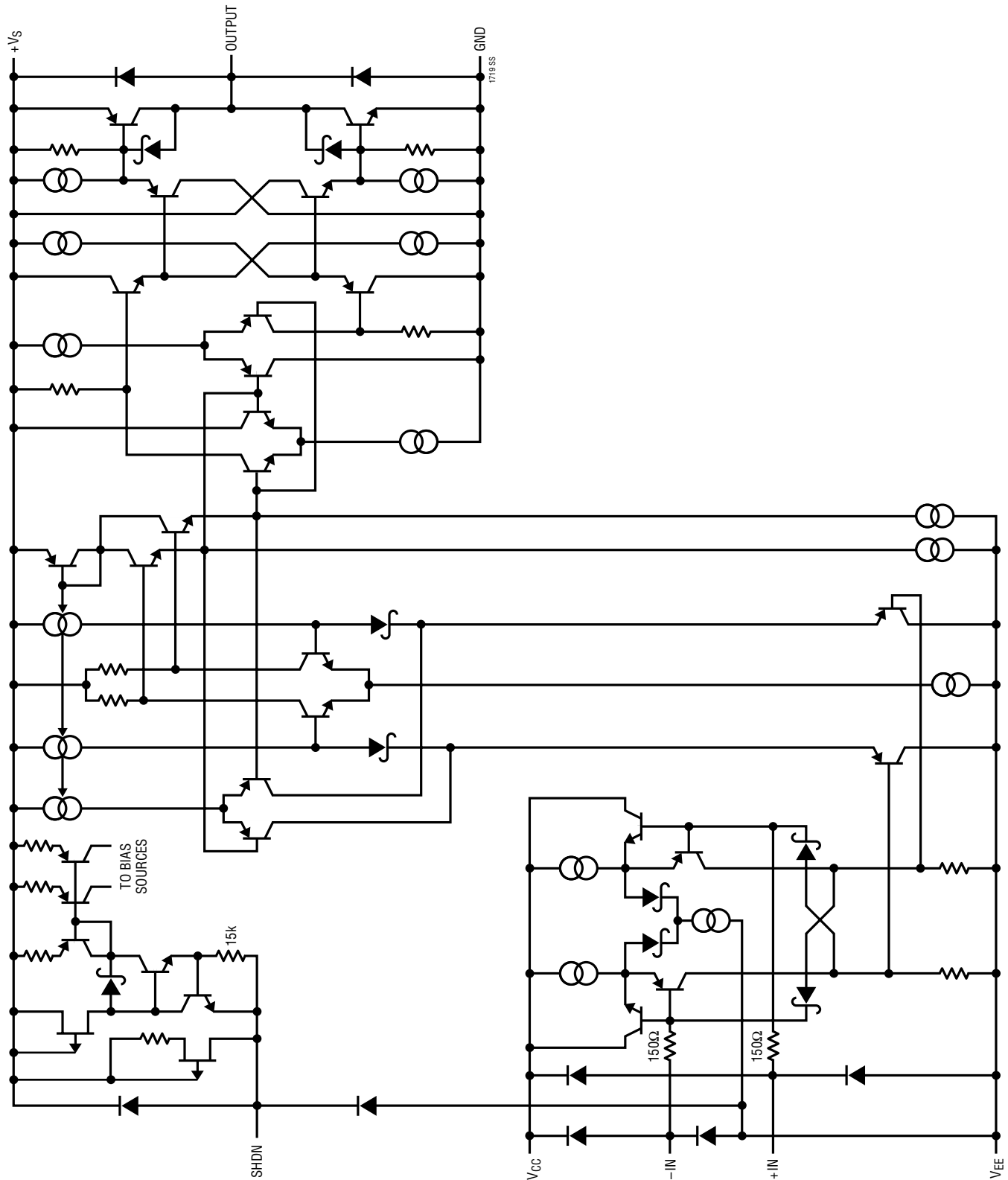
### $\pm V_{TRIP}$ Test Circuit

The input trip points test circuit uses a 1kHz triangle wave to repeatedly trip the comparator being tested. The LT1719 output is used to trigger switched capacitor sampling of the triangle wave, with a sampler for each direction. Because the triangle wave is attenuated 1000:1 and fed to the LT1719's differential input, the sampled voltages are therefore 1000 times the input trip voltages. The hysteresis and offset are computed from the trip points as shown.

### Crystal Oscillator

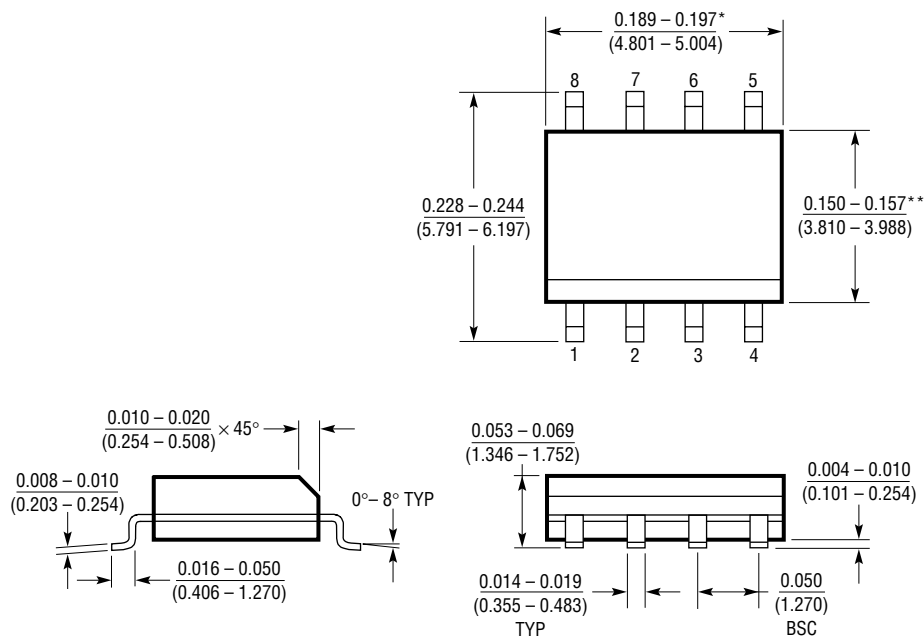
A simple crystal oscillator using an LT1719 is shown on the first page of this data sheet. The 2k-620 $\Omega$  resistor pair set a bias point at the comparator's noninverting input. The 2k-1.8k-0.1 $\mu F$  path sets the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. Although the LT1719 will give the correct logic output when one input is outside the common mode range, additional delays may occur when it is so operated, opening the possibility of spurious operating modes. Therefore, the DC bias voltages at the inputs are set near the center of the LT1719's common mode range and the 220 $\Omega$  resistor attenuates the feedback to the noninverting input. The circuit will operate with any AT-cut crystal from 1MHz to 10MHz over a 2.7V to 6V supply range. As the power is applied, the circuit remains off until the LT1719 bias circuits activate, at a typical  $V_{CC}$  of 2V to 2.2V (25°C), at which point the desired frequency output is generated.

# SIMPLIFIED SCHEMATIC



**PACKAGE DESCRIPTION** Dimensions in inches (millimeters) unless otherwise noted.

**S8 Package**  
**8-Lead Plastic Small Outline (Narrow 0.150)**  
 (LTC DWG # 05-08-1610)



\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE  
 \*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 1298

## TYPICAL APPLICATION

### High Performance Sine Wave to Square Wave Converter

Propagation delay of comparators is typically specified for a 100mV step with some fraction of that for overdrive. But in many signal processing applications, such as in communications, the goal is to convert a sine wave, such as a carrier, to a square wave for use as a timing clock. The desired behavior is for the output timing to be dependent on the input timing only. No phase shift should occur as a function of the input amplitude, which would result in AM to FM conversion.

The circuit of Figure 8a is a simple LT1719-based sine wave to square wave converter. The  $\pm 5V$  supplies on the input allow very large swing inputs, while the 3V logic supply keeps the output swing small to minimize cross talk. Figure 8b shows the time delay vs input amplitude with a 10MHz sine wave. The LT1719 delay changes just 0.65ns over the 26dB amplitude range;  $2.33^\circ$  at 10MHz. The delay is particularly flat yielding excellent AM rejection

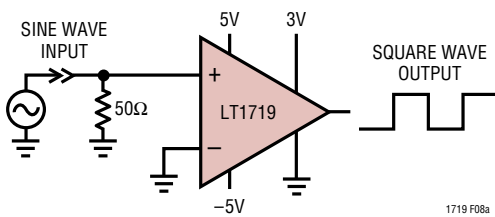


Figure 8a. LT1719-Based Sine Wave to Square Wave Converter

from 0dBm to 15dBm. If a 2:1 transformer is used to drive the input differentially, this exceptionally flat zone spans  $-5\text{dBm}$  to  $10\text{dBm}$ , a common range for RF signal levels.

Similar delay performance is achieved with input frequencies as high as 50MHz. There is, however, some additional encroachment into the central flat zone by both the small amplitude and large amplitude variations.

With small input signals, the hysteresis and dispersion make the LT1719 act like a comparator with a 12mV hysteresis span. In other words, a  $12\text{mV}_{\text{P-P}}$  sine wave at 10MHz will barely toggle the LT1719, with  $90^\circ$  of phase lag or 25ns additional delay.

Above  $5\text{V}_{\text{P-P}}$  at 10MHz, the LT1719 delay starts to decrease due to internal capacitive feed-forward in the input stage. Unlike some comparators, the LT1719 will not falsely anticipate a change in input polarity, but the feed-forward is enough to make a transition propagate through the LT1719 faster once the input polarity does change.

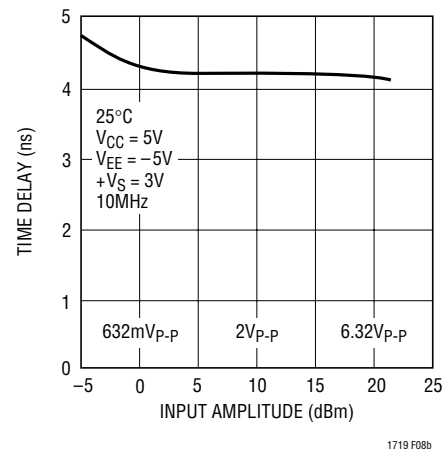


Figure 8b. Time Delay vs Sine Wave Input Amplitude

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1016	UltraFast Precision Comparator	Industry Standard 10ns Comparator
LT1116	12ns Single Supply Ground-Sensing Comparator	Single Supply Version of LT1016
LT1394	7ns, UltraFast, Single Supply Comparator	6mA Single Supply Comparator
LT1671	60ns, Low Power, Single Supply Comparator	450μA Single Supply Comparator
LT1720/LT1721	Dual/Quad 4.5ns, Single Supply 3V/5V Comparator	Dual/Quad Comparator Similar to the LT1719